



PSoC[®] 5LP Registers TRM

(Technical Reference Manual)

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Contents



| | |
|--|-----------|
| Section J: Register Mapping | 67 |
| 1.1 Maneuvering Around the Registers | 67 |
| 1.2 Register Conventions | 67 |
| 1.3 PSoC 5LP Register Map..... | 68 |
| 1.3.1 FLASH_DATA[0..262143] | 111 |
| DATA | |
| 1.3.2 SRAM_CODE64K[0..16383] | 112 |
| Code System Memory Bank | |
| 1.3.3 SRAM_CODE32K[0..8191] | 113 |
| Code System Memory Bank | |
| 1.3.4 SRAM_CODE16K[0..4095] | 114 |
| Code System Memory Bank | |
| 1.3.5 SRAM_CODE[0..4095] | 115 |
| Code System Memory Bank | |
| 1.3.6 SRAM_DATA[0..4095] | 116 |
| Data System Memory Bank | |
| 1.3.7 SRAM_DATA16K[0..4095] | 117 |
| Data System Memory Bank | |
| 1.3.8 SRAM_DATA32K[0..8191] | 118 |
| Data System Memory Bank | |
| 1.3.9 SRAM_DATA64K[0..16383] | 119 |
| Data System Memory Bank | |
| 1.3.10 DMA_SRAM64K[0..16383] | 120 |
| Data System Memory Bank | |
| 1.3.11 DMA_SRAM32K[0..8191] | 121 |
| Data System Memory Bank | |
| 1.3.12 DMA_SRAM16K[0..4095] | 122 |
| Data System Memory Bank | |
| 1.3.13 DMA_SRAM[0..4095] | 123 |
| Data System Memory Bank | |
| 1.3.14 CLKDIST_CR | 124 |
| Configuration Register CR | |
| 1.3.15 CLKDIST_LD | 126 |
| LOAD Register | |
| 1.3.16 CLKDIST_WRK0 | 128 |
| LSB Shadow Divider Value Register | |
| 1.3.17 CLKDIST_WRK1 | 129 |
| MSB Shadow Divider Value Register | |
| 1.3.18 CLKDIST_MSTR0 | 130 |
| Master clock (clk_sync_d) Divider Value Register | |
| 1.3.19 CLKDIST_MSTR1 | 131 |
| Master (clk_sync_d) Configuration Register/CPU Divider Value | |
| 1.3.20 CLKDIST_BCFG0 | 132 |

| | |
|--|-----|
| CLK_BUS LSB Divider Value Register | |
| 1.3.21 CLKDIST_BCFG1 | 133 |
| CLK_BUS MSB Divider Value Register | |
| 1.3.22 CLKDIST_BCFG2 | 134 |
| CLK_BUS Configuration Register | |
| 1.3.23 CLKDIST_UCFG | 136 |
| USB Configuration Register | |
| 1.3.24 CLKDIST_DLY0 | 137 |
| Delay block Configuration Register | |
| 1.3.25 CLKDIST_DLY1 | 138 |
| Delay block Configuration Register | |
| 1.3.26 CLKDIST_DMASK | 140 |
| Digital Clock Mask Register | |
| 1.3.27 CLKDIST_AMASK | 141 |
| Analog Clock Mask Register | |
| 1.3.28 CLKDIST_DCFG[0..7]_CFG0 | 142 |
| LSB Divider Value Register | |
| 1.3.29 CLKDIST_DCFG[0..7]_CFG1 | 143 |
| MSB Divider Value Register | |
| 1.3.30 CLKDIST_DCFG[0..7]_CFG2 | 144 |
| Configuration Register | |
| 1.3.31 CLKDIST_ACFG[0..3]_CFG0 | 146 |
| LSB Divider Value Register | |
| 1.3.32 CLKDIST_ACFG[0..3]_CFG1 | 147 |
| MSB Divider Value Register | |
| 1.3.33 CLKDIST_ACFG[0..3]_CFG2 | 148 |
| Configuration Register | |
| 1.3.34 CLKDIST_ACFG[0..3]_CFG3 | 150 |
| Analog clocks Configuration Register | |
| 1.3.35 FASTCLK_IMO_CR | 151 |
| Internal Main Oscillator Control Register | |
| 1.3.36 FASTCLK_XMHZ_CSR | 153 |
| External 4-25 MHz Crystal Oscillator Status and Control Register | |
| 1.3.37 FASTCLK_XMHZ_TST | 155 |
| External 4-25 MHz Crystal Oscillator Test Register | |
| 1.3.38 FASTCLK_XMHZ_CFG0 | 156 |
| External 4-25 MHz Crystal Oscillator Configuration Register 0 | |
| 1.3.39 FASTCLK_XMHZ_CFG1 | 157 |
| External 4-25 MHz Crystal Oscillator Configuration Register 1 | |
| 1.3.40 FASTCLK_PLL_CFG0 | 159 |
| PLL Configuration Register | |
| 1.3.41 FASTCLK_PLL_CFG1 | 160 |
| PLL Control Register | |
| 1.3.42 FASTCLK_PLL_P | 161 |
| PLL P-Counter Configuration Register | |
| 1.3.43 FASTCLK_PLL_Q | 162 |
| PLL Q-Counter Configuration Register | |
| 1.3.44 FASTCLK_PLL_TST | 163 |
| PLL Test Register | |
| 1.3.45 FASTCLK_PLL_SR | 164 |
| PLL Status Register | |
| 1.3.46 SLOWCLK_ILO_CR0 | 165 |
| Internal Low-speed Oscillator Control Register 0 | |
| 1.3.47 SLOWCLK_ILO_CR1 | 166 |

| | |
|--|-----|
| Internal Low-speed Oscillator Control Register 1 | |
| 1.3.48 SLOWCLK_X32_CR | 167 |
| External 32kHz Crystal Oscillator Control Register | |
| 1.3.49 SLOWCLK_X32_CFG | 169 |
| External 32kHz Crystal Oscillator Configuration Register | |
| 1.3.50 SLOWCLK_X32_TST | 170 |
| External 32kHz Crystal Oscillator Test Register | |
| 1.3.51 BOOST_CR0 | 171 |
| Boost Control 0 | |
| 1.3.52 BOOST_CR1 | 173 |
| Boost Control 1 | |
| 1.3.53 BOOST_CR2 | 174 |
| Boost Control 2 | |
| 1.3.54 BOOST_CR3 | 175 |
| Boost Control 3 | |
| 1.3.55 BOOST_SR | 176 |
| Boost Status | |
| 1.3.56 BOOST_CR4 | 177 |
| Boost Control Register 4 | |
| 1.3.57 BOOST_SR2 | 178 |
| Boost Status Register 2 | |
| 1.3.58 PWRSYS_CR0 | 179 |
| Power System Control Register 0 | |
| 1.3.59 PWRSYS_CR1 | 180 |
| Power System Control Register 1 | |
| 1.3.60 PM_TW_CFG0 | 181 |
| Timewheel Configuration Register 0 | |
| 1.3.61 PM_TW_CFG1 | 182 |
| Timewheel Configuration Register 1 | |
| 1.3.62 PM_TW_CFG2 | 183 |
| Timewheel Configuration Register 2 | |
| 1.3.63 PM_WDT_CFG | 184 |
| Watchdog Timer Configuration Register | |
| 1.3.64 PM_WDT_CR | 186 |
| Watchdog Timer Control Register | |
| 1.3.65 PM_INT_SR | 187 |
| Power Manager Interrupt Status Register | |
| 1.3.66 PM_MODE_CFG0 | 188 |
| Power Mode Configuration Register 0 | |
| 1.3.67 PM_MODE_CFG1 | 189 |
| Power Mode Configuration Register 1 | |
| 1.3.68 PM_MODE_CSR | 190 |
| Power Mode Control/Status Register | |
| 1.3.69 PM_USB_CR0 | 192 |
| USB Power Mode Control Register 0 | |
| 1.3.70 PM_WAKEUP_CFG0 | 193 |
| Power Mode Wakeup Mask Configuration Register 0 | |
| 1.3.71 PM_WAKEUP_CFG1 | 194 |
| Power Mode Wakeup Mask Configuration Register 1 | |
| 1.3.72 PM_WAKEUP_CFG2 | 195 |
| Power Mode Wakeup Mask Configuration Register 2 | |
| 1.3.73 PM_ACT_CFG0 | 196 |
| Active Power Mode Configuration Register 0 | |
| 1.3.74 PM_ACT_CFG1 | 197 |

| | |
|--|-----|
| Active Power Mode Configuration Register 1 | |
| 1.3.75PM_ACT_CFG2 | 198 |
| Active Power Mode Configuration Register 2 | |
| 1.3.76PM_ACT_CFG3 | 199 |
| Active Power Mode Configuration Register 3 | |
| 1.3.77PM_ACT_CFG4 | 200 |
| Active Power Mode Configuration Register 4 | |
| 1.3.78PM_ACT_CFG5 | 201 |
| Active Power Mode Configuration Register 5 | |
| 1.3.79PM_ACT_CFG6 | 202 |
| Active Power Mode Configuration Register 6 | |
| 1.3.80PM_ACT_CFG7 | 203 |
| Active Power Mode Configuration Register 7 | |
| 1.3.81PM_ACT_CFG8 | 204 |
| Active Power Mode Configuration Register 8 | |
| 1.3.82PM_ACT_CFG9 | 205 |
| Active Power Mode Configuration Register 9 | |
| 1.3.83PM_ACT_CFG10 | 206 |
| Active Power Mode Configuration Register 10 | |
| 1.3.84PM_ACT_CFG11 | 207 |
| Active Power Mode Configuration Register 11 | |
| 1.3.85PM_ACT_CFG12 | 208 |
| Active Power Mode Configuration Register 12 | |
| 1.3.86PM_ACT_CFG13 | 209 |
| Active Power Mode Configuration Register 13 | |
| 1.3.87PM_STBY_CFG0 | 210 |
| Standby Power Mode Configuration Register 0 | |
| 1.3.88PM_STBY_CFG1 | 211 |
| Standby Power Mode Configuration Register 1 | |
| 1.3.89PM_STBY_CFG2 | 212 |
| Standby Power Mode Configuration Register 2 | |
| 1.3.90PM_STBY_CFG3 | 213 |
| Standby Power Mode Configuration Register 3 | |
| 1.3.91PM_STBY_CFG4 | 214 |
| Standby Power Mode Configuration Register 4 | |
| 1.3.92PM_STBY_CFG5 | 215 |
| Standby Power Mode Configuration Register 5 | |
| 1.3.93PM_STBY_CFG6 | 216 |
| Standby Power Mode Configuration Register 6 | |
| 1.3.94PM_STBY_CFG7 | 217 |
| Standby Power Mode Configuration Register 7 | |
| 1.3.95PM_STBY_CFG8 | 218 |
| Standby Power Mode Configuration Register 8 | |
| 1.3.96PM_STBY_CFG9 | 219 |
| Standby Power Mode Configuration Register 9 | |
| 1.3.97PM_STBY_CFG10 | 220 |
| Standby Power Mode Configuration Register 10 | |
| 1.3.98PM_STBY_CFG11 | 221 |
| Standby Power Mode Configuration Register 11 | |
| 1.3.99PM_STBY_CFG12 | 222 |
| Standby Power Mode Configuration Register 12 | |
| 1.3.100PM_STBY_CFG13 | 223 |
| Standby Power Mode Configuration Register 13 | |
| 1.3.101PM_AVAIL_CR0 | 224 |

| | |
|---|-----|
| Power Mode Available Subsystem Control Register 0 | |
| 1.3.102PM_AVAIL_CR1 | 225 |
| Power Mode Available Subsystem Control Register 1 | |
| 1.3.103PM_AVAIL_CR2 | 226 |
| Power Mode Available Subsystem Control Register 2 | |
| 1.3.104PM_AVAIL_CR3 | 227 |
| Power Mode Available Subsystem Control Register 3 | |
| 1.3.105PM_AVAIL_CR4 | 228 |
| Power Mode Available Subsystem Control Register 4 | |
| 1.3.106PM_AVAIL_CR5 | 229 |
| Power Mode Available Subsystem Control Register 5 | |
| 1.3.107PM_AVAIL_CR6 | 230 |
| Power Mode Available Subsystem Control Register 6 | |
| 1.3.108PM_AVAIL_SR0 | 231 |
| Power Mode Available Subsystem Status Register 0 | |
| 1.3.109PM_AVAIL_SR1 | 232 |
| Power Mode Available Subsystem Status Register 1 | |
| 1.3.110PM_AVAIL_SR2 | 233 |
| Power Mode Available Subsystem Status Register 2 | |
| 1.3.111PM_AVAIL_SR3 | 234 |
| Power Mode Available Subsystem Status Register 3 | |
| 1.3.112PM_AVAIL_SR4 | 235 |
| Power Mode Available Subsystem Status Register 4 | |
| 1.3.113PM_AVAIL_SR5 | 236 |
| Power Mode Available Subsystem Status Register 5 | |
| 1.3.114PM_AVAIL_SR6 | 237 |
| Power Mode Available Subsystem Status Register 6 | |
| 1.3.115PICU[0..15]_INTTYPE[0..7] | 238 |
| Port Interrupt Control Type Register | |
| 1.3.116PICU[0..15]_INTSTAT | 240 |
| Port Interrupt Control Status Register | |
| 1.3.117PICU[0..15]_SNAP | 241 |
| Port Interrupt Control Snap Shot Register | |
| 1.3.118PICU[0..15]_DISABLE_COR | 242 |
| Disable Status Register Clear on Read Feature | |
| 1.3.119DAC[0..3]_TR | 243 |
| DAC Block Trim Register | |
| 1.3.120NPUMP_DSM_TR0 | 244 |
| Delta Sigma Modulator (DSM) Negative Pump Trim Register 0 | |
| 1.3.121NPUMP_SC_TR0 | 245 |
| Switched Cap Negative Pump Trim Register 0 | |
| 1.3.122NPUMP_OPAMP_TR0 | 246 |
| Analog Linear Output Buffer (OPAMP) Negative Pump Trim Register 0 | |
| 1.3.123SAR[0..1]_TR0 | 247 |
| SAR trim register 0 | |
| 1.3.124OPAMP[0..3]_TR0 | 248 |
| Analog Output Buffer Trim Register 0 | |
| 1.3.125OPAMP[0..3]_TR1 | 249 |
| Analog Output Buffer Trim Register 1 | |
| 1.3.126CMP[0..3]_TR0 | 250 |
| Comparator Trim Register | |
| 1.3.127CMP[0..3]_TR1 | 251 |
| Comparator Trim Register | |
| 1.3.128PWRSYS_HIB_TR0 | 252 |

| | |
|---|-----|
| Hibernate Trim Register 0 | |
| 1.3.129PWRSYS_HIB_TR1 | 253 |
| Hibernate Trim Register 1 | |
| 1.3.130PWRSYS_I2C_TR | 254 |
| I2C Regulator Trim Register 1 | |
| 1.3.131PWRSYS_SLP_TR | 255 |
| Sleep Regulator Trim Register | |
| 1.3.132PWRSYS_BUZZ_TR | 256 |
| Power Mode Buzz Trim Register | |
| 1.3.133PWRSYS_WAKE_TR0 | 257 |
| Power Mode Wakeup Trim Register 0 | |
| 1.3.134PWRSYS_WAKE_TR1 | 258 |
| Power Mode Wakeup Trim Register 1 | |
| 1.3.135PWRSYS_BREF_TR | 259 |
| Boot Reference Trim Register | |
| 1.3.136PWRSYS_BG_TR | 260 |
| Bandgap Trim | |
| 1.3.137PWRSYS_WAKE_TR2 | 261 |
| Power Mode Wakeup Trim Register 2 | |
| 1.3.138PWRSYS_WAKE_TR3 | 263 |
| Power Mode Wakeup Trim Register 3 | |
| 1.3.139ILO_TR0 | 264 |
| Internal Low-speed Oscillator Trim Register | |
| 1.3.140ILO_TR1 | 265 |
| Internal Low-speed Oscillator Coarse Trim Register | |
| 1.3.141X32_TR | 266 |
| 32 kHz Watch Crystal Oscillator Trim Register | |
| 1.3.142IMO_TR0 | 267 |
| Internal Main Oscillator Trim Register 0 | |
| 1.3.143IMO_TR1 | 268 |
| Internal Main Oscillator Trim Register 1 | |
| 1.3.144IMO_GAIN | 269 |
| Internal Main Oscillator Gain Trim Register | |
| 1.3.145IMO_C36M | 270 |
| Internal Main Oscillator 36 MHz clock control register {INTERNAL} | |
| 1.3.146IMO_TR2 | 271 |
| Internal Main Oscillator Trim Register 2 | |
| 1.3.147XMHZ_TR | 272 |
| External 4-25 MHz Crystal Oscillator Trim Register | |
| 1.3.148DLY | 273 |
| Delay block Configuration Register | |
| 1.3.149MLOGIC_WNDG_CFG0 | 274 |
| MLogic Wounding Register 0 | |
| 1.3.150MLOGIC_WNDG_CFG1 | 276 |
| MLogic Wounding Register 1 | |
| 1.3.151MLOGIC_DMPSTR | 277 |
| Dumpster Register | |
| 1.3.152MLOGIC_SEG_CR | 278 |
| Segment Control Register | |
| 1.3.153MLOGIC_SEG_CFG0 | 279 |
| Segment Configuration Register | |
| 1.3.154MLOGIC_DEBUG | 280 |
| MLOGIC Debug Register | |
| 1.3.155MLOGIC_CPU_SCR_CPU_SCR | 281 |

| | |
|---|-----|
| System Status and Control Register | |
| 1.3.156MLOGIC_REV_ID | 282 |
| Silicon Revision ID | |
| 1.3.157RESET_IPOR_CR0 | 283 |
| Imprecise Power On Reset Control Register 0 | |
| 1.3.158RESET_IPOR_CR1 | 284 |
| Imprecise Power On Reset Control Register 1 | |
| 1.3.159RESET_IPOR_CR2 | 285 |
| Imprecise Power On Reset Control Register 2 | |
| 1.3.160RESET_IPOR_CR3 | 286 |
| Imprecise Power On Reset Control Register 3 | |
| 1.3.161RESET_CR0 | 287 |
| LVI Set Point Control Register | |
| 1.3.162RESET_CR1 | 288 |
| Reset System Control Register | |
| 1.3.163RESET_CR2 | 289 |
| Software Reset Control Register | |
| 1.3.164RESET_CR3 | 290 |
| LVD/POR Mode Control Register | |
| 1.3.165RESET_CR4 | 291 |
| Reset Ignore Control Register | |
| 1.3.166RESET_CR5 | 292 |
| Reset Ignore Control Register | |
| 1.3.167RESET_SR0 | 293 |
| Reset and Voltage Detection Status Register 0 | |
| 1.3.168RESET_SR1 | 294 |
| Reset and Voltage Detection Status Register 1 | |
| 1.3.169RESET_SR2 | 295 |
| Reset and Voltage Detection Status Register 2 | |
| 1.3.170RESET_SR3 | 296 |
| Reset and Voltage Detection Status Register 3 | |
| 1.3.171RESET_TR | 297 |
| PRES Trim Register | |
| 1.3.172SPC_FM_EE_CR | 298 |
| FM_EE_CR | |
| 1.3.173SPC_FM_EE_WAKE_CNT | 299 |
| FM_EE_WAKE_CNT | |
| 1.3.174SPC_EE_SCR | 300 |
| EEPROM Status & Control Register | |
| 1.3.175SPC_EE_ERR | 301 |
| EEPROM Error Register | |
| 1.3.176SPC_CPU_DATA | 302 |
| SPC CPU Data Register | |
| 1.3.177SPC_DMA_DATA | 303 |
| SPC DMA Data Register | |
| 1.3.178SPC_SR | 304 |
| SPC Status Register | |
| 1.3.179SPC_CR | 306 |
| SPC Control Register | |
| 1.3.180SPC_DMM_MAP_SRAM[0..127] | 307 |
| SPC Direct Memory Mapping | |
| 1.3.181CACHE_CC_CTL | 308 |
| Cache Control Register | |
| 1.3.182CACHE_ECC_CORR | 310 |

| | |
|---|---------------------------|
| Error Correction detected | |
| 1.3.183 | CACHE_ECC_ERR 312 |
| Error Correction failed | |
| 1.3.184 | CACHE_FLASH_ERR 314 |
| FLASH error | |
| 1.3.185 | CACHE_HITMISS 316 |
| HIT/MISS counters | |
| 1.3.186 | I2C_XCFG 318 |
| I2C Extended Configuration Register | |
| 1.3.187 | I2C_ADR 320 |
| I2C Slave Address Register | |
| 1.3.188 | I2C_CFG 321 |
| I2C Configuration Register | |
| 1.3.189 | I2C_CSR 323 |
| I2C Control and Status Register | |
| 1.3.190 | I2C_D 324 |
| I2C Data Register | |
| 1.3.191 | I2C_MCSR 325 |
| I2C Master Control and Status Register | |
| 1.3.192 | I2C_CLK_DIV1 326 |
| I2C Clock Divide Factor Register-1 | |
| 1.3.193 | I2C_CLK_DIV2 327 |
| I2C Clock Divide Factor Register-2 | |
| 1.3.194 | I2C_TMOUT_CSR 328 |
| I2C TIMEOUT CSR. | |
| 1.3.195 | I2C_TMOUT_SR 329 |
| I2C TIMEOUT SR. | |
| 1.3.196 | I2C_TMOUT_CFG0 330 |
| I2C TIMEOUT Period Configuration | |
| 1.3.197 | I2C_TMOUT_CFG1 331 |
| I2C TIMEOUT Period Configuration | |
| 1.3.198 | DEC_CR 332 |
| Decimator Control Register | |
| 1.3.199 | DEC_SR 335 |
| Decimator Status Register | |
| 1.3.200 | DEC_SHIFT1 337 |
| Decimator Shifter 1 (Input) | |
| 1.3.201 | DEC_SHIFT2 338 |
| Decimator Shifter 2 (Output) | |
| 1.3.202 | DEC_DR2 339 |
| Decimator Decimation Rate (2) | |
| 1.3.203 | DEC_DR2H 340 |
| Decimator Decimation Rate (2) and Overflow Correction | |
| 1.3.204 | DEC_DR1 341 |
| Decimator Decimation Rate (1) of CIC Filter | |
| 1.3.205 | DEC_OCOR 342 |
| Decimator Offset Correction Coefficient (Low Byte) | |
| 1.3.206 | DEC_OCORM 343 |
| Decimator Offset Correction Coefficient (Middle Byte) | |
| 1.3.207 | DEC_OCORH 344 |
| Decimator Offset Correction Coefficient (High Byte) | |
| 1.3.208 | DEC_GCOR 345 |
| Decimator Gain Correction Coefficient (Low Byte) | |
| 1.3.209 | DEC_GCORH 346 |

| | |
|---|-----|
| Decimator Gain Correction Coefficient (High Byte) | |
| 1.3.210DEC_GVAL | 347 |
| Decimator Gain Correction Size Register | |
| 1.3.211DEC_OUTSAMP | 348 |
| Decimator Output Data Sample (Low Byte) | |
| 1.3.212DEC_OUTSAMPM | 349 |
| Decimator Output Data Sample (Middle Byte) | |
| 1.3.213DEC_OUTSAMPH | 350 |
| Decimator Output Data Sample (High Byte) | |
| 1.3.214DEC_OUTSAMPS | 351 |
| Decimator Output Data Sample (Sign Extension) | |
| 1.3.215DEC_COHER | 352 |
| Decimator Coherency Register | |
| 1.3.216TMR[0..3]_CFG0 | 354 |
| Configuration Register CFG0 | |
| 1.3.217TMR[0..3]_CFG1 | 355 |
| Configuration Register CFG1 | |
| 1.3.218TMR[0..3]_CFG2 | 357 |
| Configuration Register CFG2 | |
| 1.3.219TMR[0..3]_SR0 | 358 |
| Status Register SR0 | |
| 1.3.220TMR[0..3]_PER0 | 359 |
| Timer Period Register PER0 | |
| 1.3.221TMR[0..3]_PER1 | 360 |
| Timer Period Register PER1 | |
| 1.3.222TMR[0..3]_CNT_CMP0 | 361 |
| Count/Comparator value CNT/CMP0 | |
| 1.3.223TMR[0..3]_CNT_CMP1 | 362 |
| Count/Comparator value CNT/CMP1 | |
| 1.3.224TMR[0..3]_CAP0 | 363 |
| Capture Value CAP0 | |
| 1.3.225TMR[0..3]_CAP1 | 364 |
| Capture Value CAP1 | |
| 1.3.226TMR[0..3]_RT0 | 365 |
| Configuration Register RT0 | |
| 1.3.227TMR[0..3]_RT1 | 366 |
| Configuration Register RT1 | |
| 1.3.228PRT[0..14]_PC[0..7] | 367 |
| Port Pin Configuration Register | |
| 1.3.229IO_PC_PRT15_PC[0..5] | 369 |
| Port Pin Configuration Register | |
| 1.3.230IO_PC_PRT15_7_6_PC[0..1] | 370 |
| Port Pin Configuration Register | |
| 1.3.231PRT[0..14]_DR_ALIAS | 371 |
| Aliased Port Data Output Register | |
| 1.3.232PRT15_DR_15_ALIAS | 372 |
| Aliased Port Data Output Register | |
| 1.3.233PRT[0..14]_PS_ALIAS | 373 |
| Aliased Port Pin State Register | |
| 1.3.234PRT15_PS15_ALIAS | 374 |
| Aliased Port Pin State Register | |
| 1.3.235PRT[0..11]_DR | 376 |
| Port Data Output Register | |
| 1.3.236PRT[0..11]_PS | 377 |

| | |
|---|-----|
| Port Pin State Register1 | |
| 1.3.237PRT[0..11]_DM[0..2] | 378 |
| Port Drive Mode Register | |
| 1.3.238PRT[0..11]_SLW | 380 |
| Port slew rate control | |
| 1.3.239PRT[0..11]_BYP | 381 |
| Port Bypass enable | |
| 1.3.240PRT[0..11]_BIE | 382 |
| Port Bidirection enable | |
| 1.3.241PRT[0..11]_INP_DIS | 383 |
| Input buffer disable override | |
| 1.3.242PRT[0..11]_CTL | 384 |
| Port wide control signals | |
| 1.3.243PRT[0..11]_PRT | 385 |
| Port wide configuration register | |
| 1.3.244PRT[0..11]_BIT_MASK | 386 |
| Bit-mask for Aliased Register access | |
| 1.3.245PRT[0..11]_AMUX | 387 |
| Port Analog global mux bus enable | |
| 1.3.246PRT[0..11]_AG | 388 |
| Port Analog global enable | |
| 1.3.247PRT[0..11]_LCD_COM_SEG | 389 |
| Port LCD Com seg bits. | |
| 1.3.248PRT[0..11]_LCD_EN | 390 |
| Port LCD enable register. | |
| 1.3.249PRT12_DR | 391 |
| Port Data Output Register | |
| 1.3.250PRT12_PS | 392 |
| Port Pin State Register1 | |
| 1.3.251PRT12_DM[0..2] | 393 |
| Port Drive Mode Register | |
| 1.3.252PRT12_SLW | 395 |
| Port slew rate control | |
| 1.3.253PRT12_BYP | 396 |
| Port Bypass enable | |
| 1.3.254PRT12_BIE | 397 |
| Port Bidirection enable | |
| 1.3.255PRT12_INP_DIS | 398 |
| Input buffer disable override | |
| 1.3.256PRT12_SIO_HYST_EN | 399 |
| SIO Hysteresis enable | |
| 1.3.257PRT12_PRT | 400 |
| Port wide configuration register | |
| 1.3.258PRT12_BIT_MASK | 401 |
| Bit-mask for Aliased Register access | |
| 1.3.259PRT12_SIO_REG_HIFREQ | 402 |
| Regulated pull-up driver DC current setting | |
| 1.3.260PRT12_AG | 403 |
| Port Analog global enable | |
| 1.3.261PRT12_SIO_CFG | 404 |
| SIO Input Output Configuration | |
| 1.3.262PRT12_SIO_DIFF | 405 |
| Differential Input Buffer reference voltage selection | |
| 1.3.263PRT15_DR | 406 |

| | |
|--|-----|
| Port Data Output Register | |
| 1.3.264PRT15_PS | 407 |
| Port Pin State Register1 | |
| 1.3.265PRT15_DM0 | 408 |
| Port Drive Mode Register | |
| 1.3.266PRT15_DM1 | 410 |
| Port Drive Mode Register | |
| 1.3.267PRT15_DM2 | 412 |
| Port Drive Mode Register | |
| 1.3.268PRT15_SLW | 414 |
| Port slew rate control | |
| 1.3.269PRT15_BYP | 415 |
| Port Bypass enable | |
| 1.3.270PRT15_BIE | 416 |
| Port Bidirection enable | |
| 1.3.271PRT15_INP_DIS | 417 |
| Input buffer disable override | |
| 1.3.272PRT15_CTL | 418 |
| Port wide control signals | |
| 1.3.273PRT15_PRT | 419 |
| Port wide configuration register | |
| 1.3.274PRT15_BIT_MASK | 420 |
| Bit-mask for Aliased Register access | |
| 1.3.275PRT15_AMUX | 421 |
| Port Analog global mux bus enable | |
| 1.3.276PRT15_AG | 422 |
| Port Analog global enable | |
| 1.3.277PRT15_LCD_COM_SEG | 423 |
| Port LCD Com seg bits. | |
| 1.3.278PRT15_LCD_EN | 424 |
| Port LCD enable register. | |
| 1.3.279PRT0_OUT_SEL0 | 425 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.280PRT0_OUT_SEL1 | 426 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.281PRT0_OE_SEL0 | 427 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.282PRT0_OE_SEL1 | 428 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.283PRT0_DBL_SYNC_IN | 429 |
| DSI double sync enable register. | |
| 1.3.284PRT0_SYNC_OUT | 430 |
| DSI sync out enable register. | |
| 1.3.285PRT0_CAPS_SEL | 431 |
| Global DSI select register. | |
| 1.3.286PRT1_OUT_SEL0 | 432 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.287PRT1_OUT_SEL1 | 433 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.288PRT1_OE_SEL0 | 434 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.289PRT1_OE_SEL1 | 435 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.290PRT1_DBL_SYNC_IN | 436 |

| | |
|--|-----|
| DSI double sync enable register. | |
| 1.3.291PRT1_SYNC_OUT | 437 |
| DSI sync out enable register. | |
| 1.3.292PRT1_CAPS_SEL | 438 |
| Global DSI select register. | |
| 1.3.293PRT2_OUT_SEL0 | 439 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.294PRT2_OUT_SEL1 | 440 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.295PRT2_OE_SEL0 | 441 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.296PRT2_OE_SEL1 | 442 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.297PRT2_DBL_SYNC_IN | 443 |
| DSI double sync enable register. | |
| 1.3.298PRT2_SYNC_OUT | 444 |
| DSI sync out enable register. | |
| 1.3.299PRT2_CAPS_SEL | 445 |
| Global DSI select register. | |
| 1.3.300PRT3_OUT_SEL0 | 446 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.301PRT3_OUT_SEL1 | 447 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.302PRT3_OE_SEL0 | 448 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.303PRT3_OE_SEL1 | 449 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.304PRT3_DBL_SYNC_IN | 450 |
| DSI double sync enable register. | |
| 1.3.305PRT3_SYNC_OUT | 451 |
| DSI sync out enable register. | |
| 1.3.306PRT3_CAPS_SEL | 452 |
| Global DSI select register. | |
| 1.3.307PRT4_OUT_SEL0 | 453 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.308PRT4_OUT_SEL1 | 454 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.309PRT4_OE_SEL0 | 455 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.310PRT4_OE_SEL1 | 456 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.311PRT4_DBL_SYNC_IN | 457 |
| DSI double sync enable register. | |
| 1.3.312PRT4_SYNC_OUT | 458 |
| DSI sync out enable register. | |
| 1.3.313PRT4_CAPS_SEL | 459 |
| Global DSI select register. | |
| 1.3.314PRT5_OUT_SEL0 | 460 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.315PRT5_OUT_SEL1 | 461 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.316PRT5_OE_SEL0 | 462 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.317PRT5_OE_SEL1 | 463 |

| | |
|--|-----|
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.318PRT5_DBL_SYNC_IN | 464 |
| DSI double sync enable register. | |
| 1.3.319PRT5_SYNC_OUT | 465 |
| DSI sync out enable register. | |
| 1.3.320PRT5_CAPS_SEL | 466 |
| Global DSI select register. | |
| 1.3.321PRT6_OUT_SEL0 | 467 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.322PRT6_OUT_SEL1 | 468 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.323PRT6_OE_SEL0 | 469 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.324PRT6_OE_SEL1 | 470 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.325PRT6_DBL_SYNC_IN | 471 |
| DSI double sync enable register. | |
| 1.3.326PRT6_SYNC_OUT | 472 |
| DSI sync out enable register. | |
| 1.3.327PRT6_CAPS_SEL | 473 |
| Global DSI select register. | |
| 1.3.328PRT12_OUT_SEL0 | 474 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.329PRT12_OUT_SEL1 | 475 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.330PRT12_OE_SEL0 | 476 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.331PRT12_OE_SEL1 | 477 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.332PRT12_DBL_SYNC_IN | 478 |
| DSI double sync enable register. | |
| 1.3.333PRT12_SYNC_OUT | 479 |
| DSI sync out enable register. | |
| 1.3.334PRT15_OUT_SEL0 | 480 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.335PRT15_OUT_SEL1 | 481 |
| Digital System Interconnect Port Pin Output Select Registers. | |
| 1.3.336PRT15_OE_SEL0 | 482 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.337PRT15_OE_SEL1 | 483 |
| Dynamic Drive Strength of Port Output Enable Select registers. | |
| 1.3.338PRT15_DBL_SYNC_IN | 484 |
| DSI double sync enable register. | |
| 1.3.339PRT15_SYNC_OUT | 485 |
| DSI sync out enable register. | |
| 1.3.340PRT15_CAPS_SEL | 486 |
| Global DSI select register. | |
| 1.3.341EMIF_NO_UDB | 487 |
| EMIF UDB/NO_UDB Mode Register | |
| 1.3.342EMIF_RP_WAIT_STATES | 488 |
| External Memory Interface Read Path Wait States Register | |
| 1.3.343EMIF_MEM_DWN | 489 |
| External Memory Power Down Register | |
| 1.3.344EMIF_MEMCLK_DIV | 490 |

| | |
|---|-----|
| External Memory Clock Divider Register | |
| 1.3.345EMIF_CLOCK_EN | 491 |
| EMIF Clock Enable Register | |
| 1.3.346EMIF_EM_TYPE | 492 |
| External Memory Type Register | |
| 1.3.347EMIF_WP_WAIT_STATES | 493 |
| External Memory Interface Write Path Wait States Register | |
| 1.3.348SC[0..3]_CR0 | 494 |
| Switched Capacitor Control Register 0 | |
| 1.3.349SC[0..3]_CR1 | 495 |
| Switched Capacitor Control Register 1 | |
| 1.3.350SC[0..3]_CR2 | 497 |
| Switched Capacitor Control Register 2 | |
| 1.3.351DAC[0..3]_CR0 | 499 |
| DAC Block Control Register 0 | |
| 1.3.352DAC[0..3]_CR1 | 500 |
| DAC Block Control Register 1 | |
| 1.3.353DAC[0..3]_TST | 502 |
| DAC Block Test Register | |
| 1.3.354CMP[0..3]_CR | 503 |
| Comparator Control Register | |
| 1.3.355LUT[0..3]_CR | 505 |
| LUT Config Register | |
| 1.3.356LUT[0..3]_MX | 506 |
| LUT Input Mux Config Register | |
| 1.3.357OPAMP[0..3]_CR | 507 |
| Analog Output Buffer Configuration Register | |
| 1.3.358OPAMP[0..3]_RSVD | 508 |
| OPAMP reserved | |
| 1.3.359LCDDAC_CR0 | 509 |
| LCD Control Register 0 | |
| 1.3.360LCDDAC_CR1 | 511 |
| LCDDAC Control Register 1 | |
| 1.3.361LCDDRV_CR | 512 |
| LCD Control Register | |
| 1.3.362LCDTMR_CFG | 514 |
| LCD Timer Configuration Register | |
| 1.3.363BG_CR0 | 515 |
| Bandgap Precision Reference Control 0 | |
| 1.3.364BG_RSVD | 516 |
| Bandgap Precision Reference Reserved Register | |
| 1.3.365BG_DFT0 | 517 |
| Bandgap Precision Reference DFT Register 0 | |
| 1.3.366BG_DFT1 | 518 |
| Bandgap Precision Reference DFT Register 1 | |
| 1.3.367CAPSL_CFG0 | 520 |
| Capsense Reference Driver Configuration Register | |
| 1.3.368CAPSL_CFG1 | 522 |
| Capsense IO Configuration Register | |
| 1.3.369CAPSR_CFG0 | 523 |
| Capsense Reference Driver Configuration Register | |
| 1.3.370CAPSR_CFG1 | 525 |
| Capsense IO Configuration Register | |
| 1.3.371PUMP_CR0 | 526 |

| | |
|--|-----|
| Pump Configuration Register 0 | |
| 1.3.372PUMP_CR1 | 527 |
| Pump Configuration Register 1 | |
| 1.3.373LPF0_CR0 | 529 |
| Low Pass Filter Control Register | |
| 1.3.374LPF0_RSVD | 531 |
| LPF Reserved | |
| 1.3.375LPF1_CR0 | 532 |
| Low Pass Filter Control Register | |
| 1.3.376LPF1_RSVD | 534 |
| LPF Reserved | |
| 1.3.377ANAIF_CFG_MISC_CR0 | 535 |
| MISC Control Register 0 | |
| 1.3.378DSM[0..0]_CR0 | 536 |
| Delta Sigma Modulator Control Register 0 | |
| 1.3.379DSM[0..0]_CR1 | 537 |
| Delta Sigma Modulator Control Register 1 | |
| 1.3.380DSM[0..0]_CR2 | 538 |
| Delta Sigma Modulator Control Register 2 | |
| 1.3.381DSM[0..0]_CR3 | 540 |
| Delta Sigma Modulator Control Register 3 | |
| 1.3.382DSM[0..0]_CR4 | 542 |
| Delta Sigma Modulator Control Register 4 | |
| 1.3.383DSM[0..0]_CR5 | 543 |
| Delta Sigma Modulator Control Register 5 | |
| 1.3.384DSM[0..0]_CR6 | 544 |
| Delta Sigma Modulator Control Register 6 | |
| 1.3.385DSM[0..0]_CR7 | 545 |
| Delta Sigma Modulator Control Register 7 | |
| 1.3.386DSM[0..0]_CR8 | 547 |
| Delta Sigma Modulator Control Register 8 | |
| 1.3.387DSM[0..0]_CR9 | 549 |
| Delta Sigma Modulator Control Register 9 | |
| 1.3.388DSM[0..0]_CR10 | 551 |
| Delta Sigma Modulator Control Register 10 | |
| 1.3.389DSM[0..0]_CR11 | 553 |
| Delta Sigma Modulator Control Register 11 | |
| 1.3.390DSM[0..0]_CR12 | 555 |
| Delta Sigma Modulator Control Register 12 | |
| 1.3.391DSM[0..0]_CR13 | 557 |
| Delta Sigma Modulator Control Register 13 | |
| 1.3.392DSM[0..0]_CR14 | 558 |
| Delta Sigma Modulator Control Register 14 | |
| 1.3.393DSM[0..0]_CR15 | 560 |
| Delta Sigma Modulator Control Register 15 | |
| 1.3.394DSM[0..0]_CR16 | 561 |
| Delta Sigma Modulator Control Register 0 | |
| 1.3.395DSM[0..0]_CR17 | 562 |
| Delta Sigma Modulator Control Register | |
| 1.3.396DSM[0..0]_REF0 | 564 |
| Delta Sigma Modulator Reference Register 0 | |
| 1.3.397DSM[0..0]_REF1 | 565 |
| Delta Sigma Modulator Reference Register 1 | |
| 1.3.398DSM[0..0]_REF2 | 566 |

| | |
|---|-----|
| Delta Sigma Modulator Reference Register 2 | |
| 1.3.399DSM[0..0]_REF3 | 567 |
| Delta Sigma Modulator Reference Register 1 | |
| 1.3.400DSM[0..0]_DEM0 | 568 |
| Delta Sigma Modulator Dynamic Element Matching Register 0 | |
| 1.3.401DSM[0..0]_DEM1 | 570 |
| Delta Sigma Modulator Dynamic Element Matching Register 1 | |
| 1.3.402DSM[0..0]_TST0 | 571 |
| Delta Sigma Modulator Test Register 0 | |
| 1.3.403DSM[0..0]_TST1 | 573 |
| Delta Sigma Modulator Test Register 1 | |
| 1.3.404DSM[0..0]_BUF0 | 574 |
| Delta Sigma Modulator Buffer Register 0 | |
| 1.3.405DSM[0..0]_BUF1 | 575 |
| Delta Sigma Modulator Buffer Register 1 | |
| 1.3.406DSM[0..0]_BUF2 | 576 |
| Delta Sigma Modulator Buffer Register 2 | |
| 1.3.407DSM[0..0]_BUF3 | 577 |
| Delta Sigma Modulator Buffer Register 2 | |
| 1.3.408DSM[0..0]_MISC | 578 |
| Delta Sigma Modulator Miscellaneous register | |
| 1.3.409DSM[0..0]_RSVD1 | 579 |
| Delta Sigma Modulator RSVD 1 | |
| 1.3.410SAR[0..1]_CSR0 | 580 |
| SAR status and control register 0 | |
| 1.3.411SAR[0..1]_CSR1 | 582 |
| SAR status and control register 1 | |
| 1.3.412SAR[0..1]_CSR2 | 584 |
| SAR status and control register 2 | |
| 1.3.413SAR[0..1]_CSR3 | 585 |
| SAR status and control register 3 | |
| 1.3.414SAR[0..1]_CSR4 | 587 |
| SAR status and control register 4 | |
| 1.3.415SAR[0..1]_CSR5 | 589 |
| SAR status and control register 5 | |
| 1.3.416SAR[0..1]_CSR6 | 591 |
| SAR status and control register 6 | |
| 1.3.417SC0_SW0 | 592 |
| Switched Capacitor Analog Routing Register 0 | |
| 1.3.418SC0_SW2 | 593 |
| Switched Capacitor Analog Routing Register 2 | |
| 1.3.419SC0_SW3 | 594 |
| Switched Capacitor Analog Routing Register 3 | |
| 1.3.420SC0_SW4 | 595 |
| Switched Capacitor Analog Routing Register 4 | |
| 1.3.421SC0_SW6 | 596 |
| Switched Capacitor Analog Routing Register 6 | |
| 1.3.422SC0_SW7 | 597 |
| Switched Capacitor Analog Routing Register 7 | |
| 1.3.423SC0_SW8 | 598 |
| Switched Capacitor Analog Routing Register 8 | |
| 1.3.424SC0_SW10 | 599 |
| Switched Capacitor Analog Routing Register 10 | |
| 1.3.425SC0_CLK | 600 |

| | |
|---|-----|
| Switched Capacitor Clock Selection Register | |
| 1.3.426SC0_BST | 602 |
| Switched Capacitor Boost Clock Selection Register | |
| 1.3.427SC1_SW0 | 603 |
| Switched Capacitor Analog Routing Register 0 | |
| 1.3.428SC1_SW2 | 604 |
| Switched Capacitor Analog Routing Register 2 | |
| 1.3.429SC1_SW3 | 605 |
| Switched Capacitor Analog Routing Register 3 | |
| 1.3.430SC1_SW4 | 606 |
| Switched Capacitor Analog Routing Register 4 | |
| 1.3.431SC1_SW6 | 607 |
| Switched Capacitor Analog Routing Register 6 | |
| 1.3.432SC1_SW7 | 608 |
| Switched Capacitor Analog Routing Register 7 | |
| 1.3.433SC1_SW8 | 609 |
| Switched Capacitor Analog Routing Register 8 | |
| 1.3.434SC1_SW10 | 610 |
| Switched Capacitor Analog Routing Register 10 | |
| 1.3.435SC1_CLK | 611 |
| Switched Capacitor Clock Selection Register | |
| 1.3.436SC1_BST | 613 |
| Switched Capacitor Boost Clock Selection Register | |
| 1.3.437SC2_SW0 | 614 |
| Switched Capacitor Analog Routing Register 0 | |
| 1.3.438SC2_SW2 | 615 |
| Switched Capacitor Analog Routing Register 2 | |
| 1.3.439SC2_SW3 | 616 |
| Switched Capacitor Analog Routing Register 3 | |
| 1.3.440SC2_SW4 | 617 |
| Switched Capacitor Analog Routing Register 4 | |
| 1.3.441SC2_SW6 | 618 |
| Switched Capacitor Analog Routing Register 6 | |
| 1.3.442SC2_SW7 | 619 |
| Switched Capacitor Analog Routing Register 7 | |
| 1.3.443SC2_SW8 | 620 |
| Switched Capacitor Analog Routing Register 8 | |
| 1.3.444SC2_SW10 | 621 |
| Switched Capacitor Analog Routing Register 10 | |
| 1.3.445SC2_CLK | 622 |
| Switched Capacitor Clock Selection Register | |
| 1.3.446SC2_BST | 624 |
| Switched Capacitor Boost Clock Selection Register | |
| 1.3.447SC3_SW0 | 625 |
| Switched Capacitor Analog Routing Register 0 | |
| 1.3.448SC3_SW2 | 626 |
| Switched Capacitor Analog Routing Register 2 | |
| 1.3.449SC3_SW3 | 627 |
| Switched Capacitor Analog Routing Register 3 | |
| 1.3.450SC3_SW4 | 628 |
| Switched Capacitor Analog Routing Register 4 | |
| 1.3.451SC3_SW6 | 629 |
| Switched Capacitor Analog Routing Register 6 | |
| 1.3.452SC3_SW7 | 630 |

| | |
|---|-----|
| Switched Capacitor Analog Routing Register 7 | |
| 1.3.453SC3_SW8 | 631 |
| Switched Capacitor Analog Routing Register 8 | |
| 1.3.454SC3_SW10 | 632 |
| Switched Capacitor Analog Routing Register 10 | |
| 1.3.455SC3_CLK | 633 |
| Switched Capacitor Clock Selection Register | |
| 1.3.456SC3_BST | 635 |
| Switched Capacitor Boost Clock Selection Register | |
| 1.3.457DAC0_SW0 | 636 |
| DAC Analog Routing Register 0 | |
| 1.3.458DAC0_SW2 | 637 |
| DAC Analog Routing Register 2 | |
| 1.3.459DAC0_SW3 | 638 |
| DAC Analog Routing Register 3 | |
| 1.3.460DAC0_SW4 | 639 |
| DAC Analog Routing Register 4 | |
| 1.3.461DAC0_STROBE | 640 |
| DAC Strobe Register | |
| 1.3.462DAC1_SW0 | 641 |
| DAC Analog Routing Register 0 | |
| 1.3.463DAC1_SW2 | 642 |
| DAC Analog Routing Register 2 | |
| 1.3.464DAC1_SW3 | 643 |
| DAC Analog Routing Register 3 | |
| 1.3.465DAC1_SW4 | 644 |
| DAC Analog Routing Register 4 | |
| 1.3.466DAC1_STROBE | 645 |
| DAC Strobe Register | |
| 1.3.467DAC2_SW0 | 646 |
| DAC Analog Routing Register 0 | |
| 1.3.468DAC2_SW2 | 647 |
| DAC Analog Routing Register 2 | |
| 1.3.469DAC2_SW3 | 648 |
| DAC Analog Routing Register 3 | |
| 1.3.470DAC2_SW4 | 649 |
| DAC Analog Routing Register 4 | |
| 1.3.471DAC2_STROBE | 650 |
| DAC Strobe Register | |
| 1.3.472DAC3_SW0 | 651 |
| DAC Analog Routing Register 0 | |
| 1.3.473DAC3_SW2 | 652 |
| DAC Analog Routing Register 2 | |
| 1.3.474DAC3_SW3 | 653 |
| DAC Analog Routing Register 3 | |
| 1.3.475DAC3_SW4 | 654 |
| DAC Analog Routing Register 4 | |
| 1.3.476DAC3_STROBE | 655 |
| DAC Strobe Register | |
| 1.3.477CMP0_SW0 | 656 |
| Comparator Analog Routing Register 0 | |
| 1.3.478CMP0_SW2 | 657 |
| Comparator Analog Routing Register 2 | |
| 1.3.479CMP0_SW3 | 658 |

| | |
|---|-----|
| Comparator Analog Routing Register 3 | |
| 1.3.480CMP0_SW4 | 659 |
| Comparator Analog Routing Register 4 | |
| 1.3.481CMP0_SW6 | 660 |
| Comparator Analog Routing Register 6 | |
| 1.3.482CMP0_CLK | 661 |
| Comparator Clock Control Register | |
| 1.3.483CMP1_SW0 | 662 |
| Comparator Analog Routing Register 0 | |
| 1.3.484CMP1_SW2 | 663 |
| Comparator Analog Routing Register 2 | |
| 1.3.485CMP1_SW3 | 664 |
| Comparator Analog Routing Register 3 | |
| 1.3.486CMP1_SW4 | 665 |
| Comparator Analog Routing Register 4 | |
| 1.3.487CMP1_SW6 | 666 |
| Comparator Analog Routing Register 6 | |
| 1.3.488CMP1_CLK | 667 |
| Comparator Clock Control Register | |
| 1.3.489CMP2_SW0 | 668 |
| Comparator Analog Routing Register 0 | |
| 1.3.490CMP2_SW2 | 669 |
| Comparator Analog Routing Register 2 | |
| 1.3.491CMP2_SW3 | 670 |
| Comparator Analog Routing Register 3 | |
| 1.3.492CMP2_SW4 | 671 |
| Comparator Analog Routing Register 4 | |
| 1.3.493CMP2_SW6 | 672 |
| Comparator Analog Routing Register 6 | |
| 1.3.494CMP2_CLK | 673 |
| Comparator Clock Control Register | |
| 1.3.495CMP3_SW0 | 674 |
| Comparator Analog Routing Register 0 | |
| 1.3.496CMP3_SW2 | 675 |
| Comparator Analog Routing Register 2 | |
| 1.3.497CMP3_SW3 | 676 |
| Comparator Analog Routing Register 3 | |
| 1.3.498CMP3_SW4 | 677 |
| Comparator Analog Routing Register 4 | |
| 1.3.499CMP3_SW6 | 678 |
| Comparator Analog Routing Register 6 | |
| 1.3.500CMP3_CLK | 679 |
| Comparator Clock Control Register | |
| 1.3.501DSM0_SW0 | 680 |
| Delta Sigma Modulator Analog Routing Register 0 | |
| 1.3.502DSM0_SW2 | 681 |
| Delta Sigma Modulator Analog Routing Register 2 | |
| 1.3.503DSM0_SW3 | 682 |
| Delta Sigma Modulator Analog Routing Register 3 | |
| 1.3.504DSM0_SW4 | 683 |
| Delta Sigma Modulator Analog Routing Register 4 | |
| 1.3.505DSM0_SW6 | 684 |
| Delta Sigma Modulator Analog Routing Register 6 | |
| 1.3.506DSM0_CLK | 685 |

| | |
|--|-----|
| Delta Sigma Modulator Clock Selection Register | |
| 1.3.507SAR0_SW0 | 686 |
| SAR Analog Routing Register 0 | |
| 1.3.508SAR0_SW2 | 687 |
| SAR Analog Routing Register 2 | |
| 1.3.509SAR0_SW3 | 688 |
| SAR Analog Routing Register 3 | |
| 1.3.510SAR0_SW4 | 689 |
| SAR Analog Routing Register 4 | |
| 1.3.511SAR0_SW6 | 690 |
| SAR Analog Routing Register 6 | |
| 1.3.512SAR0_CLK | 691 |
| SAR Clock Selection Register | |
| 1.3.513SAR1_SW0 | 693 |
| SAR Analog Routing Register 0 | |
| 1.3.514SAR1_SW2 | 694 |
| SAR Analog Routing Register 2 | |
| 1.3.515SAR1_SW3 | 695 |
| SAR Analog Routing Register 3 | |
| 1.3.516SAR1_SW4 | 696 |
| SAR Analog Routing Register 4 | |
| 1.3.517SAR1_SW6 | 697 |
| SAR Analog Routing Register 6 | |
| 1.3.518SAR1_CLK | 698 |
| SAR Clock Selection Register | |
| 1.3.519OPAMP0_MX | 700 |
| Analog Buffer Input Selection Register | |
| 1.3.520OPAMP0_SW | 702 |
| Analog Buffer Routing Switch Register | |
| 1.3.521OPAMP1_MX | 703 |
| Analog Buffer Input Selection Register | |
| 1.3.522OPAMP1_SW | 705 |
| Analog Buffer Routing Switch Register | |
| 1.3.523OPAMP2_MX | 706 |
| Analog Buffer Input Selection Register | |
| 1.3.524OPAMP2_SW | 708 |
| Analog Buffer Routing Switch Register | |
| 1.3.525OPAMP3_MX | 709 |
| Analog Buffer Input Selection Register | |
| 1.3.526OPAMP3_SW | 711 |
| Analog Buffer Routing Switch Register | |
| 1.3.527LCDDAC_SW0 | 712 |
| LCDDAC Switch Register 0 | |
| 1.3.528LCDDAC_SW1 | 713 |
| LCDDAC Switch Register 1 | |
| 1.3.529LCDDAC_SW2 | 714 |
| LCDDAC Switch Register 2 | |
| 1.3.530LCDDAC_SW3 | 715 |
| LCDDAC Switch Register 3 | |
| 1.3.531LCDDAC_SW4 | 716 |
| LCDDAC Switch Register 3 | |
| 1.3.532SC_MISC | 717 |
| Switched Cap Miscellaneous Control Register | |
| 1.3.533BUS_SW0 | 718 |

| | |
|---|-----|
| Bus Switch Register 0 | |
| 1.3.534BUS_SW2 | 720 |
| Bus Switch Register 2 | |
| 1.3.535BUS_SW3 | 721 |
| Bus Switch Register 3 | |
| 1.3.536DFT_CR0 | 722 |
| DFT Control Register 0 | |
| 1.3.537DFT_CR1 | 723 |
| DFT Control Register 1 | |
| 1.3.538DFT_CR2 | 724 |
| DFT Control Register 2 | |
| 1.3.539DFT_CR3 | 726 |
| DFT Control Register 3 | |
| 1.3.540DFT_CR4 | 728 |
| DFT Control Register 4 | |
| 1.3.541DFT_CR5 | 729 |
| DFT Control Register 5 | |
| 1.3.542DAC[0..3]_D | 730 |
| DAC Data Register | |
| 1.3.543DSM[0..0]_OUT0 | 731 |
| DSM Output Register 0 | |
| 1.3.544DSM[0..0]_OUT1 | 732 |
| DSM Output Register 1 | |
| 1.3.545LUT_SR | 734 |
| LUT Status Register | |
| 1.3.546LUT_WRK1 | 735 |
| Reserved | |
| 1.3.547LUT_MSK | 736 |
| LUT Interrupt ReQuest (IRQ) Mask Register | |
| 1.3.548LUT_CLK | 737 |
| LUT CLK Register | |
| 1.3.549LUT_CPTR | 738 |
| LUT Capture Mode Register | |
| 1.3.550CMP_WRK | 739 |
| Comparator output working register | |
| 1.3.551CMP_TST | 740 |
| Comparator Test Register | |
| 1.3.552SC_SR | 741 |
| Switched Capacitor Status Register | |
| 1.3.553SC_WRK1 | 742 |
| Reserved | |
| 1.3.554SC_MSK | 743 |
| SC IRQ Mask Register | |
| 1.3.555SC_CMPINV | 744 |
| SC comparator inversion | |
| 1.3.556SC_CPTR | 745 |
| SC Capture Mode Register | |
| 1.3.557SAR[0..1]_WRK0 | 746 |
| SAR working register 0 | |
| 1.3.558SAR[0..1]_WRK1 | 747 |
| SAR register 1 | |
| 1.3.559ANAIF_WRK_SARS_SOF | 748 |
| SAR Global Start-of-frame register | |
| 1.3.560USB_EP0_DR[0..7] | 749 |

| | |
|--|-----|
| Control End point EP0 Data Register | |
| 1.3.561USB_CR0 | 750 |
| USB control 0 Register | |
| 1.3.562USB_CR1 | 751 |
| USB control 1 Register | |
| 1.3.563USB_SIE_EP_INT_EN | 752 |
| USB SIE Data Endpoints Interrupt Enable Register | |
| 1.3.564USB_SIE_EP_INT_SR | 753 |
| SIE Data Endpoint Interrupt Status | |
| 1.3.565USB_SIE_EP1_CNT0 | 754 |
| Non-control endpoint count register | |
| 1.3.566USB_SIE_EP1_CNT1 | 755 |
| Non-control endpoint count register | |
| 1.3.567USB_SIE_EP1_CR0 | 756 |
| 1.3.568USB_USBIO_CR0 | 757 |
| USBIO Control 0 Register | |
| 1.3.569USB_USBIO_CR2 | 758 |
| USBIO control 2 Register | |
| 1.3.570USB_USBIO_CR1 | 759 |
| USBIO control 1 Register | |
| 1.3.571USB_DYN_RECONFIG | 760 |
| USB Dynamic reconfiguration register | |
| 1.3.572USB_SOF0 | 761 |
| Start Of Frame Register | |
| 1.3.573USB_SOF1 | 762 |
| Start Of Frame Register | |
| 1.3.574USB_SIE_EP2_CNT0 | 763 |
| Non-control endpoint count register | |
| 1.3.575USB_SIE_EP2_CNT1 | 764 |
| Non-control endpoint count register | |
| 1.3.576USB_SIE_EP2_CR0 | 765 |
| 1.3.577USB_OSCLK_DR0 | 766 |
| Oscillator lock data register 0 | |
| 1.3.578USB_OSCLK_DR1 | 767 |
| Oscillator lock data register 1 | |
| 1.3.579USB_EP0_CR | 768 |
| Endpoint0 control Register | |
| 1.3.580USB_EP0_CNT | 769 |
| Endpoint0 count Register | |
| 1.3.581USB_SIE_EP3_CNT0 | 770 |
| Non-control endpoint count register | |
| 1.3.582USB_SIE_EP3_CNT1 | 771 |
| Non-control endpoint count register | |
| 1.3.583USB_SIE_EP3_CR0 | 772 |
| 1.3.584USB_SIE_EP4_CNT0 | 773 |
| Non-control endpoint count register | |
| 1.3.585USB_SIE_EP4_CNT1 | 774 |
| Non-control endpoint count register | |
| 1.3.586USB_SIE_EP4_CR0 | 775 |
| 1.3.587USB_SIE_EP5_CNT0 | 776 |
| Non-control endpoint count register | |
| 1.3.588USB_SIE_EP5_CNT1 | 777 |
| Non-control endpoint count register | |
| 1.3.589USB_SIE_EP5_CR0 | 778 |

| | | | |
|---------|--------------------|---|-----|
| 1.3.590 | USB_SIE_EP6_CNT0 | Non-control endpoint count register | 779 |
| 1.3.591 | USB_SIE_EP6_CNT1 | Non-control endpoint count register | 780 |
| 1.3.592 | USB_SIE_EP6_CR0 | | 781 |
| 1.3.593 | USB_SIE_EP7_CNT0 | Non-control endpoint count register | 782 |
| 1.3.594 | USB_SIE_EP7_CNT1 | Non-control endpoint count register | 783 |
| 1.3.595 | USB_SIE_EP7_CR0 | | 784 |
| 1.3.596 | USB_SIE_EP8_CNT0 | Non-control endpoint count register | 785 |
| 1.3.597 | USB_SIE_EP8_CNT1 | Non-control endpoint count register | 786 |
| 1.3.598 | USB_SIE_EP8_CR0 | | 787 |
| 1.3.599 | USB_ARB_EP1_CFG | Endpoint Configuration Register | 788 |
| 1.3.600 | USB_ARB_EP1_INT_EN | Endpoint Interrupt Enable Register | 789 |
| 1.3.601 | USB_ARB_EP1_SR | Endpoint Status Register | 790 |
| 1.3.602 | USB_ARB_RW1_WA | Endpoint Write Address value | 791 |
| 1.3.603 | USB_ARB_RW1_WA_MSB | Endpoint Write Address value | 792 |
| 1.3.604 | USB_ARB_RW1_RA | Endpoint Read Address value | 793 |
| 1.3.605 | USB_ARB_RW1_RA_MSB | Endpoint Read Address value | 794 |
| 1.3.606 | USB_ARB_RW1_DR | Endpoint Data Register | 795 |
| 1.3.607 | USB_BUF_SIZE | Dedicated Endpoint Buffer Size Register | 796 |
| 1.3.608 | USB_EP_ACTIVE | Endpoint Active Indication Register | 797 |
| 1.3.609 | USB_EP_TYPE | Endpoint Type (IN/OUT) Indication | 798 |
| 1.3.610 | USB_ARB_EP2_CFG | Endpoint Configuration Register | 799 |
| 1.3.611 | USB_ARB_EP2_INT_EN | Endpoint Interrupt Enable Register | 800 |
| 1.3.612 | USB_ARB_EP2_SR | Endpoint Status Register | 801 |
| 1.3.613 | USB_ARB_RW2_WA | Endpoint Write Address value | 802 |
| 1.3.614 | USB_ARB_RW2_WA_MSB | Endpoint Write Address value | 803 |
| 1.3.615 | USB_ARB_RW2_RA | Endpoint Read Address value | 804 |
| 1.3.616 | USB_ARB_RW2_RA_MSB | Endpoint Read Address value | 805 |
| 1.3.617 | USB_ARB_RW2_DR | Endpoint Data Register | 806 |
| 1.3.618 | USB_ARB_CFG | | 807 |

| | |
|-------------------------------------|-----|
| Arbiter Configuration Register | |
| 1.3.619USB_USB_CLK_EN | 808 |
| USB Block Clock Enable Register | |
| 1.3.620USB_ARB_INT_EN | 809 |
| Arbiter Interrupt Enable | |
| 1.3.621USB_ARB_INT_SR | 810 |
| Arbiter Interrupt Status | |
| 1.3.622USB_ARB_EP3_CFG | 811 |
| Endpoint Configuration Register | |
| 1.3.623USB_ARB_EP3_INT_EN | 812 |
| Endpoint Interrupt Enable Register | |
| 1.3.624USB_ARB_EP3_SR | 813 |
| Endpoint Status Register | |
| 1.3.625USB_ARB_RW3_WA | 814 |
| Endpoint Write Address value | |
| 1.3.626USB_ARB_RW3_WA_MSB | 815 |
| Endpoint Write Address value | |
| 1.3.627USB_ARB_RW3_RA | 816 |
| Endpoint Read Address value | |
| 1.3.628USB_ARB_RW3_RA_MSB | 817 |
| Endpoint Read Address value | |
| 1.3.629USB_ARB_RW3_DR | 818 |
| Endpoint Data Register | |
| 1.3.630USB_CWA | 819 |
| Common Area Write Address | |
| 1.3.631USB_CWA_MSB | 820 |
| Common Area Write Address | |
| 1.3.632USB_ARB_EP4_CFG | 821 |
| Endpoint Configuration Register | |
| 1.3.633USB_ARB_EP4_INT_EN | 822 |
| Endpoint Interrupt Enable Register | |
| 1.3.634USB_ARB_EP4_SR | 823 |
| Endpoint Status Register | |
| 1.3.635USB_ARB_RW4_WA | 824 |
| Endpoint Write Address value | |
| 1.3.636USB_ARB_RW4_WA_MSB | 825 |
| Endpoint Write Address value | |
| 1.3.637USB_ARB_RW4_RA | 826 |
| Endpoint Read Address value | |
| 1.3.638USB_ARB_RW4_RA_MSB | 827 |
| Endpoint Read Address value | |
| 1.3.639USB_ARB_RW4_DR | 828 |
| Endpoint Data Register | |
| 1.3.640USB_DMA_THRES | 829 |
| DMA Burst / Threshold Configuration | |
| 1.3.641USB_DMA_THRES_MSB | 830 |
| DMA Burst / Threshold Configuration | |
| 1.3.642USB_ARB_EP5_CFG | 831 |
| Endpoint Configuration Register | |
| 1.3.643USB_ARB_EP5_INT_EN | 832 |
| Endpoint Interrupt Enable Register | |
| 1.3.644USB_ARB_EP5_SR | 833 |
| Endpoint Status Register | |
| 1.3.645USB_ARB_RW5_WA | 834 |

| | |
|------------------------------------|-----|
| Endpoint Write Address value | |
| 1.3.646USB_ARB_RW5_WA_MSB | 835 |
| Endpoint Write Address value | |
| 1.3.647USB_ARB_RW5_RA | 836 |
| Endpoint Read Address value | |
| 1.3.648USB_ARB_RW5_RA_MSB | 837 |
| Endpoint Read Address value | |
| 1.3.649USB_ARB_RW5_DR | 838 |
| Endpoint Data Register | |
| 1.3.650USB_BUS_RST_CNT | 839 |
| Bus Reset Count Register | |
| 1.3.651USB_ARB_EP6_CFG | 840 |
| Endpoint Configuration Register | |
| 1.3.652USB_ARB_EP6_INT_EN | 841 |
| Endpoint Interrupt Enable Register | |
| 1.3.653USB_ARB_EP6_SR | 842 |
| Endpoint Status Register | |
| 1.3.654USB_ARB_RW6_WA | 843 |
| Endpoint Write Address value | |
| 1.3.655USB_ARB_RW6_WA_MSB | 844 |
| Endpoint Write Address value | |
| 1.3.656USB_ARB_RW6_RA | 845 |
| Endpoint Read Address value | |
| 1.3.657USB_ARB_RW6_RA_MSB | 846 |
| Endpoint Read Address value | |
| 1.3.658USB_ARB_RW6_DR | 847 |
| Endpoint Data Register | |
| 1.3.659USB_ARB_EP7_CFG | 848 |
| Endpoint Configuration Register | |
| 1.3.660USB_ARB_EP7_INT_EN | 849 |
| Endpoint Interrupt Enable Register | |
| 1.3.661USB_ARB_EP7_SR | 850 |
| Endpoint Status Register | |
| 1.3.662USB_ARB_RW7_WA | 851 |
| Endpoint Write Address value | |
| 1.3.663USB_ARB_RW7_WA_MSB | 852 |
| Endpoint Write Address value | |
| 1.3.664USB_ARB_RW7_RA | 853 |
| Endpoint Read Address value | |
| 1.3.665USB_ARB_RW7_RA_MSB | 854 |
| Endpoint Read Address value | |
| 1.3.666USB_ARB_RW7_DR | 855 |
| Endpoint Data Register | |
| 1.3.667USB_ARB_EP8_CFG | 856 |
| Endpoint Configuration Register | |
| 1.3.668USB_ARB_EP8_INT_EN | 857 |
| Endpoint Interrupt Enable Register | |
| 1.3.669USB_ARB_EP8_SR | 858 |
| Endpoint Status Register | |
| 1.3.670USB_ARB_RW8_WA | 859 |
| Endpoint Write Address value | |
| 1.3.671USB_ARB_RW8_WA_MSB | 860 |
| Endpoint Write Address value | |
| 1.3.672USB_ARB_RW8_RA | 861 |

| | |
|-----------------------------------|-----|
| Endpoint Read Address value | |
| 1.3.673USB_ARB_RW8_RA_MSB | 862 |
| Endpoint Read Address value | |
| 1.3.674USB_ARB_RW8_DR | 863 |
| Endpoint Data Register | |
| 1.3.675USB_MEM_DATA[0..511] | 864 |
| DATA | |
| 1.3.676B[0..3]_UDB00_A0 | 865 |
| UDB00_A0 | |
| 1.3.677B[0..3]_UDB01_A0 | 866 |
| UDB01_A0 | |
| 1.3.678B[0..3]_UDB02_A0 | 867 |
| UDB02_A0 | |
| 1.3.679B[0..3]_UDB03_A0 | 868 |
| UDB03_A0 | |
| 1.3.680B[0..3]_UDB04_A0 | 869 |
| UDB04_A0 | |
| 1.3.681B[0..3]_UDB05_A0 | 870 |
| UDB05_A0 | |
| 1.3.682B[0..3]_UDB06_A0 | 871 |
| UDB06_A0 | |
| 1.3.683B[0..3]_UDB07_A0 | 872 |
| UDB07_A0 | |
| 1.3.684B[0..3]_UDB08_A0 | 873 |
| UDB08_A0 | |
| 1.3.685B[0..3]_UDB09_A0 | 874 |
| UDB09_A0 | |
| 1.3.686B[0..3]_UDB10_A0 | 875 |
| UDB10_A0 | |
| 1.3.687B[0..3]_UDB11_A0 | 876 |
| UDB11_A0 | |
| 1.3.688B[0..3]_UDB12_A0 | 877 |
| UDB12_A0 | |
| 1.3.689B[0..3]_UDB13_A0 | 878 |
| UDB13_A0 | |
| 1.3.690B[0..3]_UDB14_A0 | 879 |
| UDB14_A0 | |
| 1.3.691B[0..3]_UDB15_A0 | 880 |
| UDB15_A0 | |
| 1.3.692B[0..3]_UDB00_A1 | 881 |
| UDB00_A1 | |
| 1.3.693B[0..3]_UDB01_A1 | 882 |
| UDB01_A1 | |
| 1.3.694B[0..3]_UDB02_A1 | 883 |
| UDB02_A1 | |
| 1.3.695B[0..3]_UDB03_A1 | 884 |
| UDB03_A1 | |
| 1.3.696B[0..3]_UDB04_A1 | 885 |
| UDB04_A1 | |
| 1.3.697B[0..3]_UDB05_A1 | 886 |
| UDB05_A1 | |
| 1.3.698B[0..3]_UDB06_A1 | 887 |
| UDB06_A1 | |
| 1.3.699B[0..3]_UDB07_A1 | 888 |

| | |
|-------------------------|-----|
| UDB07_A1 | |
| 1.3.700B[0..3]_UDB08_A1 | 889 |
| UDB08_A1 | |
| 1.3.701B[0..3]_UDB09_A1 | 890 |
| UDB09_A1 | |
| 1.3.702B[0..3]_UDB10_A1 | 891 |
| UDB10_A1 | |
| 1.3.703B[0..3]_UDB11_A1 | 892 |
| UDB11_A1 | |
| 1.3.704B[0..3]_UDB12_A1 | 893 |
| UDB12_A1 | |
| 1.3.705B[0..3]_UDB13_A1 | 894 |
| UDB13_A1 | |
| 1.3.706B[0..3]_UDB14_A1 | 895 |
| UDB14_A1 | |
| 1.3.707B[0..3]_UDB15_A1 | 896 |
| UDB15_A1 | |
| 1.3.708B[0..3]_UDB00_D0 | 897 |
| UDB00_D0 | |
| 1.3.709B[0..3]_UDB01_D0 | 898 |
| UDB01_D0 | |
| 1.3.710B[0..3]_UDB02_D0 | 899 |
| UDB02_D0 | |
| 1.3.711B[0..3]_UDB03_D0 | 900 |
| UDB03_D0 | |
| 1.3.712B[0..3]_UDB04_D0 | 901 |
| UDB04_D0 | |
| 1.3.713B[0..3]_UDB05_D0 | 902 |
| UDB05_D0 | |
| 1.3.714B[0..3]_UDB06_D0 | 903 |
| UDB06_D0 | |
| 1.3.715B[0..3]_UDB07_D0 | 904 |
| UDB07_D0 | |
| 1.3.716B[0..3]_UDB08_D0 | 905 |
| UDB08_D0 | |
| 1.3.717B[0..3]_UDB09_D0 | 906 |
| UDB09_D0 | |
| 1.3.718B[0..3]_UDB10_D0 | 907 |
| UDB10_D0 | |
| 1.3.719B[0..3]_UDB11_D0 | 908 |
| UDB11_D0 | |
| 1.3.720B[0..3]_UDB12_D0 | 909 |
| UDB12_D0 | |
| 1.3.721B[0..3]_UDB13_D0 | 910 |
| UDB13_D0 | |
| 1.3.722B[0..3]_UDB14_D0 | 911 |
| UDB14_D0 | |
| 1.3.723B[0..3]_UDB15_D0 | 912 |
| UDB15_D0 | |
| 1.3.724B[0..3]_UDB00_D1 | 913 |
| UDB00_D1 | |
| 1.3.725B[0..3]_UDB01_D1 | 914 |
| UDB01_D1 | |
| 1.3.726B[0..3]_UDB02_D1 | 915 |

| | |
|-------------------------|-----|
| UDB02_D1 | |
| 1.3.727B[0..3]_UDB03_D1 | 916 |
| UDB03_D1 | |
| 1.3.728B[0..3]_UDB04_D1 | 917 |
| UDB04_D1 | |
| 1.3.729B[0..3]_UDB05_D1 | 918 |
| UDB05_D1 | |
| 1.3.730B[0..3]_UDB06_D1 | 919 |
| UDB06_D1 | |
| 1.3.731B[0..3]_UDB07_D1 | 920 |
| UDB07_D1 | |
| 1.3.732B[0..3]_UDB08_D1 | 921 |
| UDB08_D1 | |
| 1.3.733B[0..3]_UDB09_D1 | 922 |
| UDB09_D1 | |
| 1.3.734B[0..3]_UDB10_D1 | 923 |
| UDB10_D1 | |
| 1.3.735B[0..3]_UDB11_D1 | 924 |
| UDB11_D1 | |
| 1.3.736B[0..3]_UDB12_D1 | 925 |
| UDB12_D1 | |
| 1.3.737B[0..3]_UDB13_D1 | 926 |
| UDB13_D1 | |
| 1.3.738B[0..3]_UDB14_D1 | 927 |
| UDB14_D1 | |
| 1.3.739B[0..3]_UDB15_D1 | 928 |
| UDB15_D1 | |
| 1.3.740B[0..3]_UDB00_F0 | 929 |
| UDB00_F0 | |
| 1.3.741B[0..3]_UDB01_F0 | 930 |
| UDB01_F0 | |
| 1.3.742B[0..3]_UDB02_F0 | 931 |
| UDB02_F0 | |
| 1.3.743B[0..3]_UDB03_F0 | 932 |
| UDB03_F0 | |
| 1.3.744B[0..3]_UDB04_F0 | 933 |
| UDB04_F0 | |
| 1.3.745B[0..3]_UDB05_F0 | 934 |
| UDB05_F0 | |
| 1.3.746B[0..3]_UDB06_F0 | 935 |
| UDB06_F0 | |
| 1.3.747B[0..3]_UDB07_F0 | 936 |
| UDB07_F0 | |
| 1.3.748B[0..3]_UDB08_F0 | 937 |
| UDB08_F0 | |
| 1.3.749B[0..3]_UDB09_F0 | 938 |
| UDB09_F0 | |
| 1.3.750B[0..3]_UDB10_F0 | 939 |
| UDB10_F0 | |
| 1.3.751B[0..3]_UDB11_F0 | 940 |
| UDB11_F0 | |
| 1.3.752B[0..3]_UDB12_F0 | 941 |
| UDB12_F0 | |
| 1.3.753B[0..3]_UDB13_F0 | 942 |

| | |
|-------------------------------|-----|
| UDB13_F0 | |
| 1.3.754B[0..3]_UDB14_F0 | 943 |
| UDB14_F0 | |
| 1.3.755B[0..3]_UDB15_F0 | 944 |
| UDB15_F0 | |
| 1.3.756B[0..3]_UDB00_F1 | 945 |
| UDB00_F1 | |
| 1.3.757B[0..3]_UDB01_F1 | 946 |
| UDB01_F1 | |
| 1.3.758B[0..3]_UDB02_F1 | 947 |
| UDB02_F1 | |
| 1.3.759B[0..3]_UDB03_F1 | 948 |
| UDB03_F1 | |
| 1.3.760B[0..3]_UDB04_F1 | 949 |
| UDB04_F1 | |
| 1.3.761B[0..3]_UDB05_F1 | 950 |
| UDB05_F1 | |
| 1.3.762B[0..3]_UDB06_F1 | 951 |
| UDB06_F1 | |
| 1.3.763B[0..3]_UDB07_F1 | 952 |
| UDB07_F1 | |
| 1.3.764B[0..3]_UDB08_F1 | 953 |
| UDB08_F1 | |
| 1.3.765B[0..3]_UDB09_F1 | 954 |
| UDB09_F1 | |
| 1.3.766B[0..3]_UDB10_F1 | 955 |
| UDB10_F1 | |
| 1.3.767B[0..3]_UDB11_F1 | 956 |
| UDB11_F1 | |
| 1.3.768B[0..3]_UDB12_F1 | 957 |
| UDB12_F1 | |
| 1.3.769B[0..3]_UDB13_F1 | 958 |
| UDB13_F1 | |
| 1.3.770B[0..3]_UDB14_F1 | 959 |
| UDB14_F1 | |
| 1.3.771B[0..3]_UDB15_F1 | 960 |
| UDB15_F1 | |
| 1.3.772B[0..3]_UDB00_ST | 961 |
| UDB00_ST | |
| 1.3.773B[0..3]_UDB01_ST | 962 |
| UDB01_ST | |
| 1.3.774B[0..3]_UDB02_ST | 963 |
| UDB02_ST | |
| 1.3.775B[0..3]_UDB03_ST | 964 |
| UDB03_ST | |
| 1.3.776B[0..3]_UDB04_ST | 965 |
| UDB04_ST | |
| 1.3.777B[0..3]_UDB05_ST | 966 |
| UDB05_ST | |
| 1.3.778B[0..3]_UDB06_ST | 967 |
| UDB06_ST | |
| 1.3.779B[0..3]_UDB07_ST | 968 |
| UDB07_ST | |
| 1.3.780B[0..3]_UDB08_ST | 969 |

| | |
|--------------------------|-----|
| UDB08_ST | |
| 1.3.781B[0..3]_UDB09_ST | 970 |
| UDB09_ST | |
| 1.3.782B[0..3]_UDB10_ST | 971 |
| UDB10_ST | |
| 1.3.783B[0..3]_UDB11_ST | 972 |
| UDB11_ST | |
| 1.3.784B[0..3]_UDB12_ST | 973 |
| UDB12_ST | |
| 1.3.785B[0..3]_UDB13_ST | 974 |
| UDB13_ST | |
| 1.3.786B[0..3]_UDB14_ST | 975 |
| UDB14_ST | |
| 1.3.787B[0..3]_UDB15_ST | 976 |
| UDB15_ST | |
| 1.3.788B[0..3]_UDB00_CTL | 977 |
| UDB00_CTL | |
| 1.3.789B[0..3]_UDB01_CTL | 978 |
| UDB01_CTL | |
| 1.3.790B[0..3]_UDB02_CTL | 979 |
| UDB02_CTL | |
| 1.3.791B[0..3]_UDB03_CTL | 980 |
| UDB03_CTL | |
| 1.3.792B[0..3]_UDB04_CTL | 981 |
| UDB04_CTL | |
| 1.3.793B[0..3]_UDB05_CTL | 982 |
| UDB05_CTL | |
| 1.3.794B[0..3]_UDB06_CTL | 983 |
| UDB06_CTL | |
| 1.3.795B[0..3]_UDB07_CTL | 984 |
| UDB07_CTL | |
| 1.3.796B[0..3]_UDB08_CTL | 985 |
| UDB08_CTL | |
| 1.3.797B[0..3]_UDB09_CTL | 986 |
| UDB09_CTL | |
| 1.3.798B[0..3]_UDB10_CTL | 987 |
| UDB10_CTL | |
| 1.3.799B[0..3]_UDB11_CTL | 988 |
| UDB11_CTL | |
| 1.3.800B[0..3]_UDB12_CTL | 989 |
| UDB12_CTL | |
| 1.3.801B[0..3]_UDB13_CTL | 990 |
| UDB13_CTL | |
| 1.3.802B[0..3]_UDB14_CTL | 991 |
| UDB14_CTL | |
| 1.3.803B[0..3]_UDB15_CTL | 992 |
| UDB15_CTL | |
| 1.3.804B[0..3]_UDB00_MSK | 993 |
| UDB00_MSK | |
| 1.3.805B[0..3]_UDB01_MSK | 994 |
| UDB01_MSK | |
| 1.3.806B[0..3]_UDB02_MSK | 995 |
| UDB02_MSK | |
| 1.3.807B[0..3]_UDB03_MSK | 996 |

| | |
|---------------------------|------|
| UDB03_MSK | |
| 1.3.808B[0..3]_UDB04_MSK | 997 |
| UDB04_MSK | |
| 1.3.809B[0..3]_UDB05_MSK | 998 |
| UDB05_MSK | |
| 1.3.810B[0..3]_UDB06_MSK | 999 |
| UDB06_MSK | |
| 1.3.811B[0..3]_UDB07_MSK | 1000 |
| UDB07_MSK | |
| 1.3.812B[0..3]_UDB08_MSK | 1001 |
| UDB08_MSK | |
| 1.3.813B[0..3]_UDB09_MSK | 1002 |
| UDB09_MSK | |
| 1.3.814B[0..3]_UDB10_MSK | 1003 |
| UDB10_MSK | |
| 1.3.815B[0..3]_UDB11_MSK | 1004 |
| UDB11_MSK | |
| 1.3.816B[0..3]_UDB12_MSK | 1005 |
| UDB12_MSK | |
| 1.3.817B[0..3]_UDB13_MSK | 1006 |
| UDB13_MSK | |
| 1.3.818B[0..3]_UDB14_MSK | 1007 |
| UDB14_MSK | |
| 1.3.819B[0..3]_UDB15_MSK | 1008 |
| UDB15_MSK | |
| 1.3.820B[0..3]_UDB00_ACTL | 1009 |
| UDB00_ACTL | |
| 1.3.821B[0..3]_UDB01_ACTL | 1011 |
| UDB01_ACTL | |
| 1.3.822B[0..3]_UDB02_ACTL | 1013 |
| UDB02_ACTL | |
| 1.3.823B[0..3]_UDB03_ACTL | 1015 |
| UDB03_ACTL | |
| 1.3.824B[0..3]_UDB04_ACTL | 1017 |
| UDB04_ACTL | |
| 1.3.825B[0..3]_UDB05_ACTL | 1019 |
| UDB05_ACTL | |
| 1.3.826B[0..3]_UDB06_ACTL | 1021 |
| UDB06_ACTL | |
| 1.3.827B[0..3]_UDB07_ACTL | 1023 |
| UDB07_ACTL | |
| 1.3.828B[0..3]_UDB08_ACTL | 1025 |
| UDB08_ACTL | |
| 1.3.829B[0..3]_UDB09_ACTL | 1027 |
| UDB09_ACTL | |
| 1.3.830B[0..3]_UDB10_ACTL | 1029 |
| UDB10_ACTL | |
| 1.3.831B[0..3]_UDB11_ACTL | 1031 |
| UDB11_ACTL | |
| 1.3.832B[0..3]_UDB12_ACTL | 1033 |
| UDB12_ACTL | |
| 1.3.833B[0..3]_UDB13_ACTL | 1035 |
| UDB13_ACTL | |
| 1.3.834B[0..3]_UDB14_ACTL | 1037 |

| | |
|----------------------------------|------|
| UDB14_ACTL | |
| 1.3.835B[0..3]_UDB15_ACTL | 1039 |
| UDB15_ACTL | |
| 1.3.836B[0..3]_UDB00_MC | 1041 |
| UDB00_MC | |
| 1.3.837B[0..3]_UDB01_MC | 1042 |
| UDB01_MC | |
| 1.3.838B[0..3]_UDB02_MC | 1043 |
| UDB02_MC | |
| 1.3.839B[0..3]_UDB03_MC | 1044 |
| UDB03_MC | |
| 1.3.840B[0..3]_UDB04_MC | 1045 |
| UDB04_MC | |
| 1.3.841B[0..3]_UDB05_MC | 1046 |
| UDB05_MC | |
| 1.3.842B[0..3]_UDB06_MC | 1047 |
| UDB06_MC | |
| 1.3.843B[0..3]_UDB07_MC | 1048 |
| UDB07_MC | |
| 1.3.844B[0..3]_UDB08_MC | 1049 |
| UDB08_MC | |
| 1.3.845B[0..3]_UDB09_MC | 1050 |
| UDB09_MC | |
| 1.3.846B[0..3]_UDB10_MC | 1051 |
| UDB10_MC | |
| 1.3.847B[0..3]_UDB11_MC | 1052 |
| UDB11_MC | |
| 1.3.848B[0..3]_UDB12_MC | 1053 |
| UDB12_MC | |
| 1.3.849B[0..3]_UDB13_MC | 1054 |
| UDB13_MC | |
| 1.3.850B[0..3]_UDB14_MC | 1055 |
| UDB14_MC | |
| 1.3.851B[0..3]_UDB15_MC | 1056 |
| UDB15_MC | |
| 1.3.852B[0..3]_UDB00_01_A0 | 1057 |
| UDB00_01_A0 | |
| 1.3.853B[0..3]_UDB01_02_A0 | 1058 |
| UDB01_02_A0 | |
| 1.3.854B[0..3]_UDB02_03_A0 | 1059 |
| UDB02_03_A0 | |
| 1.3.855B[0..3]_UDB03_04_A0 | 1060 |
| UDB03_04_A0 | |
| 1.3.856B[0..3]_UDB04_05_A0 | 1061 |
| UDB04_05_A0 | |
| 1.3.857B[0..3]_UDB05_06_A0 | 1062 |
| UDB05_06_A0 | |
| 1.3.858B[0..3]_UDB06_07_A0 | 1063 |
| UDB06_07_A0 | |
| 1.3.859B[0..3]_UDB07_08_A0 | 1064 |
| UDB07_08_A0 | |
| 1.3.860B[0..3]_UDB08_09_A0 | 1065 |
| UDB08_09_A0 | |
| 1.3.861B[0..3]_UDB09_10_A0 | 1066 |

| | |
|----------------------------------|------|
| UDB09_10_A0 | |
| 1.3.862B[0..3]_UDB10_11_A0 | 1067 |
| UDB10_11_A0 | |
| 1.3.863B[0..3]_UDB11_12_A0 | 1068 |
| UDB11_12_A0 | |
| 1.3.864B[0..3]_UDB12_13_A0 | 1069 |
| UDB12_13_A0 | |
| 1.3.865B[0..3]_UDB13_14_A0 | 1070 |
| UDB13_14_A0 | |
| 1.3.866B[0..3]_UDB14_15_A0 | 1071 |
| UDB14_15_A0 | |
| 1.3.867B[0..3]_UDB00_01_A1 | 1072 |
| UDB00_01_A1 | |
| 1.3.868B[0..3]_UDB01_02_A1 | 1073 |
| UDB01_02_A1 | |
| 1.3.869B[0..3]_UDB02_03_A1 | 1074 |
| UDB02_03_A1 | |
| 1.3.870B[0..3]_UDB03_04_A1 | 1075 |
| UDB03_04_A1 | |
| 1.3.871B[0..3]_UDB04_05_A1 | 1076 |
| UDB04_05_A1 | |
| 1.3.872B[0..3]_UDB05_06_A1 | 1077 |
| UDB05_06_A1 | |
| 1.3.873B[0..3]_UDB06_07_A1 | 1078 |
| UDB06_07_A1 | |
| 1.3.874B[0..3]_UDB07_08_A1 | 1079 |
| UDB07_08_A1 | |
| 1.3.875B[0..3]_UDB08_09_A1 | 1080 |
| UDB08_09_A1 | |
| 1.3.876B[0..3]_UDB09_10_A1 | 1081 |
| UDB09_10_A1 | |
| 1.3.877B[0..3]_UDB10_11_A1 | 1082 |
| UDB10_11_A1 | |
| 1.3.878B[0..3]_UDB11_12_A1 | 1083 |
| UDB11_12_A1 | |
| 1.3.879B[0..3]_UDB12_13_A1 | 1084 |
| UDB12_13_A1 | |
| 1.3.880B[0..3]_UDB13_14_A1 | 1085 |
| UDB13_14_A1 | |
| 1.3.881B[0..3]_UDB14_15_A1 | 1086 |
| UDB14_15_A1 | |
| 1.3.882B[0..3]_UDB00_01_D0 | 1087 |
| UDB00_01_D0 | |
| 1.3.883B[0..3]_UDB01_02_D0 | 1088 |
| UDB01_02_D0 | |
| 1.3.884B[0..3]_UDB02_03_D0 | 1089 |
| UDB02_03_D0 | |
| 1.3.885B[0..3]_UDB03_04_D0 | 1090 |
| UDB03_04_D0 | |
| 1.3.886B[0..3]_UDB04_05_D0 | 1091 |
| UDB04_05_D0 | |
| 1.3.887B[0..3]_UDB05_06_D0 | 1092 |
| UDB05_06_D0 | |
| 1.3.888B[0..3]_UDB06_07_D0 | 1093 |

| | |
|----------------------------------|------|
| UDB06_07_D0 | |
| 1.3.889B[0..3]_UDB07_08_D0 | 1094 |
| UDB07_08_D0 | |
| 1.3.890B[0..3]_UDB08_09_D0 | 1095 |
| UDB08_09_D0 | |
| 1.3.891B[0..3]_UDB09_10_D0 | 1096 |
| UDB09_10_D0 | |
| 1.3.892B[0..3]_UDB10_11_D0 | 1097 |
| UDB10_11_D0 | |
| 1.3.893B[0..3]_UDB11_12_D0 | 1098 |
| UDB11_12_D0 | |
| 1.3.894B[0..3]_UDB12_13_D0 | 1099 |
| UDB12_13_D0 | |
| 1.3.895B[0..3]_UDB13_14_D0 | 1100 |
| UDB13_14_D0 | |
| 1.3.896B[0..3]_UDB14_15_D0 | 1101 |
| UDB14_15_D0 | |
| 1.3.897B[0..3]_UDB00_01_D1 | 1102 |
| UDB00_01_D1 | |
| 1.3.898B[0..3]_UDB01_02_D1 | 1103 |
| UDB01_02_D1 | |
| 1.3.899B[0..3]_UDB02_03_D1 | 1104 |
| UDB02_03_D1 | |
| 1.3.900B[0..3]_UDB03_04_D1 | 1105 |
| UDB03_04_D1 | |
| 1.3.901B[0..3]_UDB04_05_D1 | 1106 |
| UDB04_05_D1 | |
| 1.3.902B[0..3]_UDB05_06_D1 | 1107 |
| UDB05_06_D1 | |
| 1.3.903B[0..3]_UDB06_07_D1 | 1108 |
| UDB06_07_D1 | |
| 1.3.904B[0..3]_UDB07_08_D1 | 1109 |
| UDB07_08_D1 | |
| 1.3.905B[0..3]_UDB08_09_D1 | 1110 |
| UDB08_09_D1 | |
| 1.3.906B[0..3]_UDB09_10_D1 | 1111 |
| UDB09_10_D1 | |
| 1.3.907B[0..3]_UDB10_11_D1 | 1112 |
| UDB10_11_D1 | |
| 1.3.908B[0..3]_UDB11_12_D1 | 1113 |
| UDB11_12_D1 | |
| 1.3.909B[0..3]_UDB12_13_D1 | 1114 |
| UDB12_13_D1 | |
| 1.3.910B[0..3]_UDB13_14_D1 | 1115 |
| UDB13_14_D1 | |
| 1.3.911B[0..3]_UDB14_15_D1 | 1116 |
| UDB14_15_D1 | |
| 1.3.912B[0..3]_UDB00_01_F0 | 1117 |
| UDB00_01_F0 | |
| 1.3.913B[0..3]_UDB01_02_F0 | 1118 |
| UDB01_02_F0 | |
| 1.3.914B[0..3]_UDB02_03_F0 | 1119 |
| UDB02_03_F0 | |
| 1.3.915B[0..3]_UDB03_04_F0 | 1120 |

| | |
|----------------------------|------|
| UDB03_04_F0 | |
| 1.3.916B[0..3]_UDB04_05_F0 | 1121 |
| UDB04_05_F0 | |
| 1.3.917B[0..3]_UDB05_06_F0 | 1122 |
| UDB05_06_F0 | |
| 1.3.918B[0..3]_UDB06_07_F0 | 1123 |
| UDB06_07_F0 | |
| 1.3.919B[0..3]_UDB07_08_F0 | 1124 |
| UDB07_08_F0 | |
| 1.3.920B[0..3]_UDB08_09_F0 | 1125 |
| UDB08_09_F0 | |
| 1.3.921B[0..3]_UDB09_10_F0 | 1126 |
| UDB09_10_F0 | |
| 1.3.922B[0..3]_UDB10_11_F0 | 1127 |
| UDB10_11_F0 | |
| 1.3.923B[0..3]_UDB11_12_F0 | 1128 |
| UDB11_12_F0 | |
| 1.3.924B[0..3]_UDB12_13_F0 | 1129 |
| UDB12_13_F0 | |
| 1.3.925B[0..3]_UDB13_14_F0 | 1130 |
| UDB13_14_F0 | |
| 1.3.926B[0..3]_UDB14_15_F0 | 1131 |
| UDB14_15_F0 | |
| 1.3.927B[0..3]_UDB00_01_F1 | 1132 |
| UDB00_01_F1 | |
| 1.3.928B[0..3]_UDB01_02_F1 | 1133 |
| UDB01_02_F1 | |
| 1.3.929B[0..3]_UDB02_03_F1 | 1134 |
| UDB02_03_F1 | |
| 1.3.930B[0..3]_UDB03_04_F1 | 1135 |
| UDB03_04_F1 | |
| 1.3.931B[0..3]_UDB04_05_F1 | 1136 |
| UDB04_05_F1 | |
| 1.3.932B[0..3]_UDB05_06_F1 | 1137 |
| UDB05_06_F1 | |
| 1.3.933B[0..3]_UDB06_07_F1 | 1138 |
| UDB06_07_F1 | |
| 1.3.934B[0..3]_UDB07_08_F1 | 1139 |
| UDB07_08_F1 | |
| 1.3.935B[0..3]_UDB08_09_F1 | 1140 |
| UDB08_09_F1 | |
| 1.3.936B[0..3]_UDB09_10_F1 | 1141 |
| UDB09_10_F1 | |
| 1.3.937B[0..3]_UDB10_11_F1 | 1142 |
| UDB10_11_F1 | |
| 1.3.938B[0..3]_UDB11_12_F1 | 1143 |
| UDB11_12_F1 | |
| 1.3.939B[0..3]_UDB12_13_F1 | 1144 |
| UDB12_13_F1 | |
| 1.3.940B[0..3]_UDB13_14_F1 | 1145 |
| UDB13_14_F1 | |
| 1.3.941B[0..3]_UDB14_15_F1 | 1146 |
| UDB14_15_F1 | |
| 1.3.942B[0..3]_UDB00_01_ST | 1147 |

| | |
|-----------------------------------|------|
| UDB00_01_ST | |
| 1.3.943B[0..3]_UDB01_02_ST | 1148 |
| UDB01_02_ST | |
| 1.3.944B[0..3]_UDB02_03_ST | 1149 |
| UDB02_03_ST | |
| 1.3.945B[0..3]_UDB03_04_ST | 1150 |
| UDB03_04_ST | |
| 1.3.946B[0..3]_UDB04_05_ST | 1151 |
| UDB04_05_ST | |
| 1.3.947B[0..3]_UDB05_06_ST | 1152 |
| UDB05_06_ST | |
| 1.3.948B[0..3]_UDB06_07_ST | 1153 |
| UDB06_07_ST | |
| 1.3.949B[0..3]_UDB07_08_ST | 1154 |
| UDB07_08_ST | |
| 1.3.950B[0..3]_UDB08_09_ST | 1155 |
| UDB08_09_ST | |
| 1.3.951B[0..3]_UDB09_10_ST | 1156 |
| UDB09_10_ST | |
| 1.3.952B[0..3]_UDB10_11_ST | 1157 |
| UDB10_11_ST | |
| 1.3.953B[0..3]_UDB11_12_ST | 1158 |
| UDB11_12_ST | |
| 1.3.954B[0..3]_UDB12_13_ST | 1159 |
| UDB12_13_ST | |
| 1.3.955B[0..3]_UDB13_14_ST | 1160 |
| UDB13_14_ST | |
| 1.3.956B[0..3]_UDB14_15_ST | 1161 |
| UDB14_15_ST | |
| 1.3.957B[0..3]_UDB00_01_CTL | 1162 |
| UDB00_01_CTL | |
| 1.3.958B[0..3]_UDB01_02_CTL | 1163 |
| UDB01_02_CTL | |
| 1.3.959B[0..3]_UDB02_03_CTL | 1164 |
| UDB02_03_CTL | |
| 1.3.960B[0..3]_UDB03_04_CTL | 1165 |
| UDB03_04_CTL | |
| 1.3.961B[0..3]_UDB04_05_CTL | 1166 |
| UDB04_05_CTL | |
| 1.3.962B[0..3]_UDB05_06_CTL | 1167 |
| UDB05_06_CTL | |
| 1.3.963B[0..3]_UDB06_07_CTL | 1168 |
| UDB06_07_CTL | |
| 1.3.964B[0..3]_UDB07_08_CTL | 1169 |
| UDB07_08_CTL | |
| 1.3.965B[0..3]_UDB08_09_CTL | 1170 |
| UDB08_09_CTL | |
| 1.3.966B[0..3]_UDB09_10_CTL | 1171 |
| UDB09_10_CTL | |
| 1.3.967B[0..3]_UDB10_11_CTL | 1172 |
| UDB10_11_CTL | |
| 1.3.968B[0..3]_UDB11_12_CTL | 1173 |
| UDB11_12_CTL | |
| 1.3.969B[0..3]_UDB12_13_CTL | 1174 |

| | |
|------------------------------------|------|
| UDB12_13_CTL | |
| 1.3.970B[0..3]_UDB13_14_CTL | 1175 |
| UDB13_14_CTL | |
| 1.3.971B[0..3]_UDB14_15_CTL | 1176 |
| UDB14_15_CTL | |
| 1.3.972B[0..3]_UDB00_01_MSK | 1177 |
| UDB00_01_MSK | |
| 1.3.973B[0..3]_UDB01_02_MSK | 1178 |
| UDB01_02_MSK | |
| 1.3.974B[0..3]_UDB02_03_MSK | 1179 |
| UDB02_03_MSK | |
| 1.3.975B[0..3]_UDB03_04_MSK | 1180 |
| UDB03_04_MSK | |
| 1.3.976B[0..3]_UDB04_05_MSK | 1181 |
| UDB04_05_MSK | |
| 1.3.977B[0..3]_UDB05_06_MSK | 1182 |
| UDB05_06_MSK | |
| 1.3.978B[0..3]_UDB06_07_MSK | 1183 |
| UDB06_07_MSK | |
| 1.3.979B[0..3]_UDB07_08_MSK | 1184 |
| UDB07_08_MSK | |
| 1.3.980B[0..3]_UDB08_09_MSK | 1185 |
| UDB08_09_MSK | |
| 1.3.981B[0..3]_UDB09_10_MSK | 1186 |
| UDB09_10_MSK | |
| 1.3.982B[0..3]_UDB10_11_MSK | 1187 |
| UDB10_11_MSK | |
| 1.3.983B[0..3]_UDB11_12_MSK | 1188 |
| UDB11_12_MSK | |
| 1.3.984B[0..3]_UDB12_13_MSK | 1189 |
| UDB12_13_MSK | |
| 1.3.985B[0..3]_UDB13_14_MSK | 1190 |
| UDB13_14_MSK | |
| 1.3.986B[0..3]_UDB14_15_MSK | 1191 |
| UDB14_15_MSK | |
| 1.3.987B[0..3]_UDB00_01_ACTL | 1192 |
| UDB00_01_ACTL | |
| 1.3.988B[0..3]_UDB01_02_ACTL | 1194 |
| UDB01_02_ACTL | |
| 1.3.989B[0..3]_UDB02_03_ACTL | 1196 |
| UDB02_03_ACTL | |
| 1.3.990B[0..3]_UDB03_04_ACTL | 1198 |
| UDB03_04_ACTL | |
| 1.3.991B[0..3]_UDB04_05_ACTL | 1200 |
| UDB04_05_ACTL | |
| 1.3.992B[0..3]_UDB05_06_ACTL | 1202 |
| UDB05_06_ACTL | |
| 1.3.993B[0..3]_UDB06_07_ACTL | 1204 |
| UDB06_07_ACTL | |
| 1.3.994B[0..3]_UDB07_08_ACTL | 1206 |
| UDB07_08_ACTL | |
| 1.3.995B[0..3]_UDB08_09_ACTL | 1208 |
| UDB08_09_ACTL | |
| 1.3.996B[0..3]_UDB09_10_ACTL | 1210 |

| | |
|-------------------------------------|------|
| UDB09_10_ACTL | |
| 1.3.997B[0..3]_UDB10_11_ACTL | 1212 |
| UDB10_11_ACTL | |
| 1.3.998B[0..3]_UDB11_12_ACTL | 1214 |
| UDB11_12_ACTL | |
| 1.3.999B[0..3]_UDB12_13_ACTL | 1216 |
| UDB12_13_ACTL | |
| 1.3.1000B[0..3]_UDB13_14_ACTL | 1218 |
| UDB13_14_ACTL | |
| 1.3.1001B[0..3]_UDB14_15_ACTL | 1220 |
| UDB14_15_ACTL | |
| 1.3.1002B[0..3]_UDB00_01_MC | 1222 |
| UDB00_01_MC | |
| 1.3.1003B[0..3]_UDB01_02_MC | 1223 |
| UDB01_02_MC | |
| 1.3.1004B[0..3]_UDB02_03_MC | 1224 |
| UDB02_03_MC | |
| 1.3.1005B[0..3]_UDB03_04_MC | 1225 |
| UDB03_04_MC | |
| 1.3.1006B[0..3]_UDB04_05_MC | 1226 |
| UDB04_05_MC | |
| 1.3.1007B[0..3]_UDB05_06_MC | 1227 |
| UDB05_06_MC | |
| 1.3.1008B[0..3]_UDB06_07_MC | 1228 |
| UDB06_07_MC | |
| 1.3.1009B[0..3]_UDB07_08_MC | 1229 |
| UDB07_08_MC | |
| 1.3.1010B[0..3]_UDB08_09_MC | 1230 |
| UDB08_09_MC | |
| 1.3.1011B[0..3]_UDB09_10_MC | 1231 |
| UDB09_10_MC | |
| 1.3.1012B[0..3]_UDB10_11_MC | 1232 |
| UDB10_11_MC | |
| 1.3.1013B[0..3]_UDB11_12_MC | 1233 |
| UDB11_12_MC | |
| 1.3.1014B[0..3]_UDB12_13_MC | 1234 |
| UDB12_13_MC | |
| 1.3.1015B[0..3]_UDB13_14_MC | 1235 |
| UDB13_14_MC | |
| 1.3.1016B[0..3]_UDB14_15_MC | 1236 |
| UDB14_15_MC | |
| 1.3.1017B[0..3]_UDB00_A0_A1 | 1237 |
| UDB00_A0_A1 | |
| 1.3.1018B[0..3]_UDB01_A0_A1 | 1238 |
| UDB01_A0_A1 | |
| 1.3.1019B[0..3]_UDB02_A0_A1 | 1239 |
| UDB02_A0_A1 | |
| 1.3.1020B[0..3]_UDB03_A0_A1 | 1240 |
| UDB03_A0_A1 | |
| 1.3.1021B[0..3]_UDB04_A0_A1 | 1241 |
| UDB04_A0_A1 | |
| 1.3.1022B[0..3]_UDB05_A0_A1 | 1242 |
| UDB05_A0_A1 | |
| 1.3.1023B[0..3]_UDB06_A0_A1 | 1243 |

| | |
|-----------------------------|------|
| UDB06_A0_A1 | |
| 1.3.1024B[0..3]_UDB07_A0_A1 | 1244 |
| UDB07_A0_A1 | |
| 1.3.1025B[0..3]_UDB08_A0_A1 | 1245 |
| UDB08_A0_A1 | |
| 1.3.1026B[0..3]_UDB09_A0_A1 | 1246 |
| UDB09_A0_A1 | |
| 1.3.1027B[0..3]_UDB10_A0_A1 | 1247 |
| UDB10_A0_A1 | |
| 1.3.1028B[0..3]_UDB11_A0_A1 | 1248 |
| UDB11_A0_A1 | |
| 1.3.1029B[0..3]_UDB12_A0_A1 | 1249 |
| UDB12_A0_A1 | |
| 1.3.1030B[0..3]_UDB13_A0_A1 | 1250 |
| UDB13_A0_A1 | |
| 1.3.1031B[0..3]_UDB14_A0_A1 | 1251 |
| UDB14_A0_A1 | |
| 1.3.1032B[0..3]_UDB15_A0_A1 | 1252 |
| UDB15_A0_A1 | |
| 1.3.1033B[0..3]_UDB00_D0_D1 | 1253 |
| UDB00_D0_D1 | |
| 1.3.1034B[0..3]_UDB01_D0_D1 | 1254 |
| UDB01_D0_D1 | |
| 1.3.1035B[0..3]_UDB02_D0_D1 | 1255 |
| UDB02_D0_D1 | |
| 1.3.1036B[0..3]_UDB03_D0_D1 | 1256 |
| UDB03_D0_D1 | |
| 1.3.1037B[0..3]_UDB04_D0_D1 | 1257 |
| UDB04_D0_D1 | |
| 1.3.1038B[0..3]_UDB05_D0_D1 | 1258 |
| UDB05_D0_D1 | |
| 1.3.1039B[0..3]_UDB06_D0_D1 | 1259 |
| UDB06_D0_D1 | |
| 1.3.1040B[0..3]_UDB07_D0_D1 | 1260 |
| UDB07_D0_D1 | |
| 1.3.1041B[0..3]_UDB08_D0_D1 | 1261 |
| UDB08_D0_D1 | |
| 1.3.1042B[0..3]_UDB09_D0_D1 | 1262 |
| UDB09_D0_D1 | |
| 1.3.1043B[0..3]_UDB10_D0_D1 | 1263 |
| UDB10_D0_D1 | |
| 1.3.1044B[0..3]_UDB11_D0_D1 | 1264 |
| UDB11_D0_D1 | |
| 1.3.1045B[0..3]_UDB12_D0_D1 | 1265 |
| UDB12_D0_D1 | |
| 1.3.1046B[0..3]_UDB13_D0_D1 | 1266 |
| UDB13_D0_D1 | |
| 1.3.1047B[0..3]_UDB14_D0_D1 | 1267 |
| UDB14_D0_D1 | |
| 1.3.1048B[0..3]_UDB15_D0_D1 | 1268 |
| UDB15_D0_D1 | |
| 1.3.1049B[0..3]_UDB00_F0_F1 | 1269 |
| UDB00_F0_F1 | |
| 1.3.1050B[0..3]_UDB01_F0_F1 | 1270 |

| | |
|------------------------------|------|
| UDB01_F0_F1 | |
| 1.3.1051B[0..3]_UDB02_F0_F1 | 1271 |
| UDB02_F0_F1 | |
| 1.3.1052B[0..3]_UDB03_F0_F1 | 1272 |
| UDB03_F0_F1 | |
| 1.3.1053B[0..3]_UDB04_F0_F1 | 1273 |
| UDB04_F0_F1 | |
| 1.3.1054B[0..3]_UDB05_F0_F1 | 1274 |
| UDB05_F0_F1 | |
| 1.3.1055B[0..3]_UDB06_F0_F1 | 1275 |
| UDB06_F0_F1 | |
| 1.3.1056B[0..3]_UDB07_F0_F1 | 1276 |
| UDB07_F0_F1 | |
| 1.3.1057B[0..3]_UDB08_F0_F1 | 1277 |
| UDB08_F0_F1 | |
| 1.3.1058B[0..3]_UDB09_F0_F1 | 1278 |
| UDB09_F0_F1 | |
| 1.3.1059B[0..3]_UDB10_F0_F1 | 1279 |
| UDB10_F0_F1 | |
| 1.3.1060B[0..3]_UDB11_F0_F1 | 1280 |
| UDB11_F0_F1 | |
| 1.3.1061B[0..3]_UDB12_F0_F1 | 1281 |
| UDB12_F0_F1 | |
| 1.3.1062B[0..3]_UDB13_F0_F1 | 1282 |
| UDB13_F0_F1 | |
| 1.3.1063B[0..3]_UDB14_F0_F1 | 1283 |
| UDB14_F0_F1 | |
| 1.3.1064B[0..3]_UDB15_F0_F1 | 1284 |
| UDB15_F0_F1 | |
| 1.3.1065B[0..3]_UDB00_ST_CTL | 1285 |
| UDB00_ST_CTL | |
| 1.3.1066B[0..3]_UDB01_ST_CTL | 1286 |
| UDB01_ST_CTL | |
| 1.3.1067B[0..3]_UDB02_ST_CTL | 1287 |
| UDB02_ST_CTL | |
| 1.3.1068B[0..3]_UDB03_ST_CTL | 1288 |
| UDB03_ST_CTL | |
| 1.3.1069B[0..3]_UDB04_ST_CTL | 1289 |
| UDB04_ST_CTL | |
| 1.3.1070B[0..3]_UDB05_ST_CTL | 1290 |
| UDB05_ST_CTL | |
| 1.3.1071B[0..3]_UDB06_ST_CTL | 1291 |
| UDB06_ST_CTL | |
| 1.3.1072B[0..3]_UDB07_ST_CTL | 1292 |
| UDB07_ST_CTL | |
| 1.3.1073B[0..3]_UDB08_ST_CTL | 1293 |
| UDB08_ST_CTL | |
| 1.3.1074B[0..3]_UDB09_ST_CTL | 1294 |
| UDB09_ST_CTL | |
| 1.3.1075B[0..3]_UDB10_ST_CTL | 1295 |
| UDB10_ST_CTL | |
| 1.3.1076B[0..3]_UDB11_ST_CTL | 1296 |
| UDB11_ST_CTL | |
| 1.3.1077B[0..3]_UDB12_ST_CTL | 1297 |

| | |
|--------------------------------------|------|
| UDB12_ST_CTL | |
| 1.3.1078B[0..3]_UDB13_ST_CTL | 1298 |
| UDB13_ST_CTL | |
| 1.3.1079B[0..3]_UDB14_ST_CTL | 1299 |
| UDB14_ST_CTL | |
| 1.3.1080B[0..3]_UDB15_ST_CTL | 1300 |
| UDB15_ST_CTL | |
| 1.3.1081B[0..3]_UDB00_MSK_ACTL | 1301 |
| UDB00_MSK_ACTL | |
| 1.3.1082B[0..3]_UDB01_MSK_ACTL | 1303 |
| UDB01_MSK_ACTL | |
| 1.3.1083B[0..3]_UDB02_MSK_ACTL | 1305 |
| UDB02_MSK_ACTL | |
| 1.3.1084B[0..3]_UDB03_MSK_ACTL | 1307 |
| UDB03_MSK_ACTL | |
| 1.3.1085B[0..3]_UDB04_MSK_ACTL | 1309 |
| UDB04_MSK_ACTL | |
| 1.3.1086B[0..3]_UDB05_MSK_ACTL | 1311 |
| UDB05_MSK_ACTL | |
| 1.3.1087B[0..3]_UDB06_MSK_ACTL | 1313 |
| UDB06_MSK_ACTL | |
| 1.3.1088B[0..3]_UDB07_MSK_ACTL | 1315 |
| UDB07_MSK_ACTL | |
| 1.3.1089B[0..3]_UDB08_MSK_ACTL | 1317 |
| UDB08_MSK_ACTL | |
| 1.3.1090B[0..3]_UDB09_MSK_ACTL | 1319 |
| UDB09_MSK_ACTL | |
| 1.3.1091B[0..3]_UDB10_MSK_ACTL | 1321 |
| UDB10_MSK_ACTL | |
| 1.3.1092B[0..3]_UDB11_MSK_ACTL | 1323 |
| UDB11_MSK_ACTL | |
| 1.3.1093B[0..3]_UDB12_MSK_ACTL | 1325 |
| UDB12_MSK_ACTL | |
| 1.3.1094B[0..3]_UDB13_MSK_ACTL | 1327 |
| UDB13_MSK_ACTL | |
| 1.3.1095B[0..3]_UDB14_MSK_ACTL | 1329 |
| UDB14_MSK_ACTL | |
| 1.3.1096B[0..3]_UDB15_MSK_ACTL | 1331 |
| UDB15_MSK_ACTL | |
| 1.3.1097B[0..3]_UDB00_MC_00 | 1333 |
| UDB00_MC_00 | |
| 1.3.1098B[0..3]_UDB01_MC_00 | 1334 |
| UDB01_MC_00 | |
| 1.3.1099B[0..3]_UDB02_MC_00 | 1335 |
| UDB02_MC_00 | |
| 1.3.1100B[0..3]_UDB03_MC_00 | 1336 |
| UDB03_MC_00 | |
| 1.3.1101B[0..3]_UDB04_MC_00 | 1337 |
| UDB04_MC_00 | |
| 1.3.1102B[0..3]_UDB05_MC_00 | 1338 |
| UDB05_MC_00 | |
| 1.3.1103B[0..3]_UDB06_MC_00 | 1339 |
| UDB06_MC_00 | |
| 1.3.1104B[0..3]_UDB07_MC_00 | 1340 |

| | |
|---|------|
| UDB07_MC_00 | |
| 1.3.1105B[0..3]_UDB08_MC_00 | 1341 |
| UDB08_MC_00 | |
| 1.3.1106B[0..3]_UDB09_MC_00 | 1342 |
| UDB09_MC_00 | |
| 1.3.1107B[0..3]_UDB10_MC_00 | 1343 |
| UDB10_MC_00 | |
| 1.3.1108B[0..3]_UDB11_MC_00 | 1344 |
| UDB11_MC_00 | |
| 1.3.1109B[0..3]_UDB12_MC_00 | 1345 |
| UDB12_MC_00 | |
| 1.3.1110B[0..3]_UDB13_MC_00 | 1346 |
| UDB13_MC_00 | |
| 1.3.1111B[0..3]_UDB14_MC_00 | 1347 |
| UDB14_MC_00 | |
| 1.3.1112B[0..3]_UDB15_MC_00 | 1348 |
| UDB15_MC_00 | |
| 1.3.1113PHUB_CFG | 1349 |
| PHUB Configuration | |
| 1.3.1114PHUB_ERR | 1351 |
| PHUB Error Detection | |
| 1.3.1115PHUB_ERR_ADR | 1352 |
| PHUB Error Address | |
| 1.3.1116PHUB_CH[0..23]_BASIC_CFG | 1353 |
| Channel Basic Configuration Register | |
| 1.3.1117PHUB_CH[0..23]_ACTION | 1355 |
| Channel Action | |
| 1.3.1118PHUB_CH[0..23]_BASIC_STATUS | 1357 |
| Channel Basic Status Register | |
| 1.3.1119PHUB_CFGMEM[0..23]_CFG0 | 1360 |
| PHUB Channel Configuration Register 0 | |
| 1.3.1120PHUB_CFGMEM[0..23]_CFG1 | 1363 |
| PHUB Channel Configuration Register 1 | |
| 1.3.1121PHUB_TDMEM[0..127]_ORIG_TD0 | 1365 |
| PHUB Original Transaction Descriptor 0 | |
| 1.3.1122PHUB_TDMEM[0..127]_ORIG_TD1 | 1371 |
| PHUB Original Transaction Descriptor 0 | |
| 1.3.1123EE_DATA[0..2047] | 1376 |
| EEPROM Memory | |
| 1.3.1124CAN[0..0]_CSR_INT_SR | 1377 |
| INT_SR | |
| 1.3.1125CAN[0..0]_CSR_INT_EN | 1379 |
| INT_EN | |
| 1.3.1126CAN[0..0]_CSR_BUF_SR | 1381 |
| BUF_SR | |
| 1.3.1127CAN[0..0]_CSR_ERR_SR | 1383 |
| ERR_SR | |
| 1.3.1128CAN[0..0]_CSR_CMD | 1384 |
| CMD | |
| 1.3.1129CAN[0..0]_CSR_CFG | 1385 |
| CFG | |
| 1.3.1130CAN[0..0]_TX[0..7]_CMD | 1387 |
| TXCMD | |
| 1.3.1131CAN[0..0]_TX[0..7]_ID | 1389 |

| | |
|---|------|
| TXID | |
| 1.3.1132CAN[0..0]_TX[0..7]_DH | 1390 |
| TXDH | |
| 1.3.1133CAN[0..0]_TX[0..7]_DL | 1391 |
| TXDL | |
| 1.3.1134CAN[0..0]_RX[0..15]_CMD | 1392 |
| RXCMD | |
| 1.3.1135CAN[0..0]_RX[0..15]_ID | 1394 |
| RXID | |
| 1.3.1136CAN[0..0]_RX[0..15]_DH | 1395 |
| RXDH | |
| 1.3.1137CAN[0..0]_RX[0..15]_DL | 1396 |
| RXDL | |
| 1.3.1138CAN[0..0]_RX[0..15]_AMR | 1397 |
| RXAMR | |
| 1.3.1139CAN[0..0]_RX[0..15]_ACR | 1398 |
| RXACR | |
| 1.3.1140CAN[0..0]_RX[0..15]_AMRD | 1399 |
| RXAMRD | |
| 1.3.1141CAN[0..0]_RX[0..15]_ACRD | 1400 |
| RXACRD | |
| 1.3.1142DFB[0..0]_DPA_SRAM_DATA[0..127] | 1401 |
| Data RAM A | |
| 1.3.1143DFB[0..0]_DPB_SRAM_DATA[0..127] | 1402 |
| DFB Data RAM B | |
| 1.3.1144DFB[0..0]_CSA_SRAM_DATA[0..63] | 1403 |
| DFB Control Store A | |
| 1.3.1145DFB[0..0]_CSB_SRAM_DATA[0..63] | 1404 |
| DFB Control Store B | |
| 1.3.1146DFB[0..0]_FSM_SRAM_DATA[0..63] | 1405 |
| DFB Code Store B | |
| 1.3.1147DFB[0..0]_ACU_SRAM_DATA[0..15] | 1406 |
| DFB Address Store | |
| 1.3.1148DFB[0..0]_CR | 1407 |
| DFB Command Register | |
| 1.3.1149DFB[0..0]_SR | 1408 |
| DFB Status Register | |
| 1.3.1150DFB[0..0]_RAM_EN | 1411 |
| DFB RAM Enable Register | |
| 1.3.1151DFB[0..0]_RAM_DIR | 1413 |
| DFB RAM Direction Register | |
| 1.3.1152DFB[0..0]_SEMA | 1415 |
| DFB Semaphore Register | |
| 1.3.1153DFB[0..0]_DSI_CTRL | 1416 |
| DFB Global Control Register | |
| 1.3.1154DFB[0..0]_INT_CTRL | 1417 |
| DFB Interrupt Control Register | |
| 1.3.1155DFB[0..0]_DMA_CTRL | 1418 |
| DFB DMAREQ Control Register | |
| 1.3.1156DFB[0..0]_STAGEA | 1419 |
| DFB Low Byte Staging Register A | |
| 1.3.1157DFB[0..0]_STAGEAM | 1420 |
| DFB Middle Byte Staging Register A | |
| 1.3.1158DFB[0..0]_STAGEAH | 1421 |

| | |
|--|------|
| DFB High Byte Staging Register A | |
| 1.3.1159DFB[0..0]_STAGEB | 1422 |
| DFB Low Byte Staging Register B | |
| 1.3.1160DFB[0..0]_STAGEBM | 1423 |
| DFB Middle Byte Staging Register B | |
| 1.3.1161DFB[0..0]_STAGEBH | 1424 |
| DFB High Byte Staging Register B | |
| 1.3.1162DFB[0..0]_HOLDA | 1425 |
| DFB Low Byte Holding Register A | |
| 1.3.1163DFB[0..0]_HOLDAM | 1426 |
| DFB Middle Byte Holding Register A | |
| 1.3.1164DFB[0..0]_HOLDAH | 1427 |
| DFB High Byte Holding Register A | |
| 1.3.1165DFB[0..0]_HOLDAS | 1428 |
| DFB Holding Register A Sign Extension | |
| 1.3.1166DFB[0..0]_HOLDB | 1429 |
| DFB Low Byte Holding Register B | |
| 1.3.1167DFB[0..0]_HOLDBM | 1430 |
| DFB Middle Byte Holding Register B | |
| 1.3.1168DFB[0..0]_HOLDBH | 1431 |
| DFB High Byte Holding Register B | |
| 1.3.1169DFB[0..0]_HOLDBS | 1432 |
| DFB Holding Register B Sign Extension | |
| 1.3.1170DFB[0..0]_COHER | 1433 |
| DFB Coherency Register | |
| 1.3.1171DFB[0..0]_DALIGN | 1435 |
| DFB Data Alignment Register | |
| 1.3.1172B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] | 1436 |
| PLD_IT | |
| 1.3.1173B[0..3]_P[0..7]_U[0..1]_PLD_ORT[0..3] | 1446 |
| PLD_ORT | |
| 1.3.1174B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST | 1450 |
| MC_CFG_CEN_CONST | |
| 1.3.1175B[0..3]_P[0..7]_U[0..1]_MC_CFG_XORFB | 1453 |
| MC_CFG_XORFB | |
| 1.3.1176B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET | 1455 |
| MC_CFG_SET_RESET | |
| 1.3.1177B[0..3]_P[0..7]_U[0..1]_MC_CFG_BYPASS | 1458 |
| MC_CFG_BYPASS | |
| 1.3.1178B[0..3]_P[0..7]_U[0..1]_CFG0 | 1460 |
| CFG0 | |
| 1.3.1179B[0..3]_P[0..7]_U[0..1]_CFG1 | 1461 |
| CFG1 | |
| 1.3.1180B[0..3]_P[0..7]_U[0..1]_CFG2 | 1462 |
| CFG2 | |
| 1.3.1181B[0..3]_P[0..7]_U[0..1]_CFG3 | 1464 |
| CFG3 | |
| 1.3.1182B[0..3]_P[0..7]_U[0..1]_CFG4 | 1466 |
| CFG4 | |
| 1.3.1183B[0..3]_P[0..7]_U[0..1]_CFG5 | 1467 |
| CFG5 | |
| 1.3.1184B[0..3]_P[0..7]_U[0..1]_CFG6 | 1469 |
| CFG6 | |
| 1.3.1185B[0..3]_P[0..7]_U[0..1]_CFG7 | 1471 |

| | |
|--|------|
| CFG7 | |
| 1.3.1186B[0..3]_P[0..7]_U[0..1]_CFG8 | 1473 |
| CFG8 | |
| 1.3.1187B[0..3]_P[0..7]_U[0..1]_CFG9 | 1474 |
| CFG9 | |
| 1.3.1188B[0..3]_P[0..7]_U[0..1]_CFG10 | 1475 |
| CFG10 | |
| 1.3.1189B[0..3]_P[0..7]_U[0..1]_CFG11 | 1476 |
| CFG11 | |
| 1.3.1190B[0..3]_P[0..7]_U[0..1]_CFG12 | 1477 |
| CFG12 | |
| 1.3.1191B[0..3]_P[0..7]_U[0..1]_CFG13 | 1479 |
| CFG13 | |
| 1.3.1192B[0..3]_P[0..7]_U[0..1]_CFG14 | 1481 |
| CFG14 | |
| 1.3.1193B[0..3]_P[0..7]_U[0..1]_CFG15 | 1483 |
| CFG15 | |
| 1.3.1194B[0..3]_P[0..7]_U[0..1]_CFG16 | 1485 |
| CFG16 | |
| 1.3.1195B[0..3]_P[0..7]_U[0..1]_CFG17 | 1488 |
| CFG17 | |
| 1.3.1196B[0..3]_P[0..7]_U[0..1]_CFG18 | 1490 |
| CFG18 | |
| 1.3.1197B[0..3]_P[0..7]_U[0..1]_CFG19 | 1491 |
| CFG19 | |
| 1.3.1198B[0..3]_P[0..7]_U[0..1]_CFG20 | 1492 |
| CFG20 | |
| 1.3.1199B[0..3]_P[0..7]_U[0..1]_CFG21 | 1493 |
| CFG21 | |
| 1.3.1200B[0..3]_P[0..7]_U[0..1]_CFG22 | 1494 |
| CFG22 | |
| 1.3.1201B[0..3]_P[0..7]_U[0..1]_CFG23 | 1496 |
| CFG23 | |
| 1.3.1202B[0..3]_P[0..7]_U[0..1]_CFG24 | 1498 |
| CFG24 | |
| 1.3.1203B[0..3]_P[0..7]_U[0..1]_CFG25 | 1500 |
| CFG25 | |
| 1.3.1204B[0..3]_P[0..7]_U[0..1]_CFG26 | 1502 |
| CFG26 | |
| 1.3.1205B[0..3]_P[0..7]_U[0..1]_CFG27 | 1504 |
| CFG27 | |
| 1.3.1206B[0..3]_P[0..7]_U[0..1]_CFG28 | 1506 |
| CFG28 | |
| 1.3.1207B[0..3]_P[0..7]_U[0..1]_CFG29 | 1508 |
| CFG29 | |
| 1.3.1208B[0..3]_P[0..7]_U[0..1]_CFG30 | 1510 |
| CFG30 | |
| 1.3.1209B[0..3]_P[0..7]_U[0..1]_CFG31 | 1512 |
| CFG31 | |
| 1.3.1210B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] | 1514 |
| DCFG | |
| 1.3.1211B[0..3]_P[0..7]_ROUTE_HC[0..127] | 1519 |
| HC | |
| 1.3.1212B[0..3]_P[0..7]_ROUTE_HV_L[0..15] | 1541 |

| | |
|---|------|
| HV_L | |
| 1.3.1213B[0..3]_P[0..7]_ROUTE_HS[0..23] | 1547 |
| HS | |
| 1.3.1214B[0..3]_P[0..7]_ROUTE_HV_R[0..15] | 1552 |
| HV_R | |
| 1.3.1215B[0..3]_P[0..7]_ROUTE_PLD0IN0 | 1558 |
| PLD0IN0 | |
| 1.3.1216B[0..3]_P[0..7]_ROUTE_PLD0IN1 | 1559 |
| PLD0IN1 | |
| 1.3.1217B[0..3]_P[0..7]_ROUTE_PLD0IN2 | 1560 |
| PLD0IN2 | |
| 1.3.1218B[0..3]_P[0..7]_ROUTE_PLD1IN0 | 1561 |
| PLD1IN0 | |
| 1.3.1219B[0..3]_P[0..7]_ROUTE_PLD1IN1 | 1562 |
| PLD1IN1 | |
| 1.3.1220B[0..3]_P[0..7]_ROUTE_PLD1IN2 | 1563 |
| PLD1IN2 | |
| 1.3.1221B[0..3]_P[0..7]_ROUTE_DPIN0 | 1564 |
| DPIN0 | |
| 1.3.1222B[0..3]_P[0..7]_ROUTE_DPIN1 | 1565 |
| DPIN1 | |
| 1.3.1223B[0..3]_P[0..7]_ROUTE_SCIN | 1566 |
| SCIN | |
| 1.3.1224B[0..3]_P[0..7]_ROUTE_SCI0IN | 1567 |
| SCIOIN | |
| 1.3.1225B[0..3]_P[0..7]_ROUTE_RCIN | 1568 |
| RCIN | |
| 1.3.1226B[0..3]_P[0..7]_ROUTE_VS0 | 1569 |
| VS0 | |
| 1.3.1227B[0..3]_P[0..7]_ROUTE_VS1 | 1570 |
| VS1 | |
| 1.3.1228B[0..3]_P[0..7]_ROUTE_VS2 | 1571 |
| VS2 | |
| 1.3.1229B[0..3]_P[0..7]_ROUTE_VS3 | 1572 |
| VS3 | |
| 1.3.1230B[0..3]_P[0..7]_ROUTE_VS4 | 1573 |
| VS4 | |
| 1.3.1231B[0..3]_P[0..7]_ROUTE_VS5 | 1574 |
| VS5 | |
| 1.3.1232B[0..3]_P[0..7]_ROUTE_VS6 | 1575 |
| VS6 | |
| 1.3.1233B[0..3]_P[0..7]_ROUTE_VS7 | 1576 |
| VS7 | |
| 1.3.1234DSI[0..15]_HC[0..127] | 1577 |
| HC | |
| 1.3.1235DSI[0..15]_HV_L[0..15] | 1599 |
| HV_L | |
| 1.3.1236DSI[0..15]_HS[0..23] | 1603 |
| HS | |
| 1.3.1237DSI[0..15]_HV_R[0..15] | 1608 |
| HV_R | |
| 1.3.1238DSI[0..15]_DSIINP0 | 1612 |
| DSIINP0 | |
| 1.3.1239DSI[0..15]_DSIINP1 | 1613 |

| | |
|-------------------------------|------|
| DSIINP1 | |
| 1.3.1240DSI[0..15]_DSIINP2 | 1614 |
| DSIINP2 | |
| 1.3.1241DSI[0..15]_DSIINP3 | 1615 |
| DSIINP3 | |
| 1.3.1242DSI[0..15]_DSIINP4 | 1616 |
| DSIINP4 | |
| 1.3.1243DSI[0..15]_DSIINP5 | 1617 |
| DSIINP5 | |
| 1.3.1244DSI[0..15]_DSIOUTP0 | 1618 |
| DSIOUTP0 | |
| 1.3.1245DSI[0..15]_DSIOUTP1 | 1619 |
| DSIOUTP1 | |
| 1.3.1246DSI[0..15]_DSIOUTP2 | 1620 |
| DSIOUTP2 | |
| 1.3.1247DSI[0..15]_DSIOUTP3 | 1621 |
| DSIOUTP3 | |
| 1.3.1248DSI[0..15]_DSIOUTT0 | 1622 |
| DSIOUTT0 | |
| 1.3.1249DSI[0..15]_DSIOUTT1 | 1623 |
| DSIOUTT1 | |
| 1.3.1250DSI[0..15]_DSIOUTT2 | 1624 |
| DSIOUTT2 | |
| 1.3.1251DSI[0..15]_DSIOUTT3 | 1625 |
| DSIOUTT3 | |
| 1.3.1252DSI[0..15]_DSIOUTT4 | 1626 |
| DSIOUTT4 | |
| 1.3.1253DSI[0..15]_DSIOUTT5 | 1627 |
| DSIOUTT5 | |
| 1.3.1254DSI[0..15]_VS0 | 1628 |
| VS0 | |
| 1.3.1255DSI[0..15]_VS1 | 1629 |
| VS1 | |
| 1.3.1256DSI[0..15]_VS2 | 1630 |
| VS2 | |
| 1.3.1257DSI[0..15]_VS3 | 1631 |
| VS3 | |
| 1.3.1258DSI[0..15]_VS4 | 1632 |
| VS4 | |
| 1.3.1259DSI[0..15]_VS5 | 1633 |
| VS5 | |
| 1.3.1260DSI[0..15]_VS6 | 1634 |
| VS6 | |
| 1.3.1261DSI[0..15]_VS7 | 1635 |
| VS7 | |
| 1.3.1262BCTL[0..3]_MDCLK_EN | 1636 |
| MDCLK_EN | |
| 1.3.1263BCTL[0..3]_MBCLK_EN | 1637 |
| MBCLK_EN | |
| 1.3.1264BCTL[0..3]_WAIT_CFG | 1639 |
| WAIT_CFG | |
| 1.3.1265BCTL[0..3]_BANK_CTL | 1641 |
| BANK_CTL | |
| 1.3.1266BCTL[0..3]_UDB_TEST_0 | 1643 |

| | |
|--------------------------------|------|
| UDB_TEST_0 | |
| 1.3.1267BCTL[0..3]_UDB_TEST_1 | 1644 |
| UDB_TEST_1 | |
| 1.3.1268BCTL[0..3]_UDB_TEST_2 | 1645 |
| UDB_TEST_2 | |
| 1.3.1269BCTL[0..3]_UDB_TEST_3 | 1646 |
| UDB_TEST_3 | |
| 1.3.1270BCTL[0..3]_DCLK_EN0 | 1648 |
| DCLK_EN | |
| 1.3.1271BCTL[0..3]_BCLK_EN0 | 1649 |
| BCLK_EN | |
| 1.3.1272BCTL[0..3]_DCLK_EN1 | 1652 |
| DCLK_EN | |
| 1.3.1273BCTL[0..3]_BCLK_EN1 | 1653 |
| BCLK_EN | |
| 1.3.1274BCTL[0..3]_DCLK_EN2 | 1656 |
| DCLK_EN | |
| 1.3.1275BCTL[0..3]_BCLK_EN2 | 1657 |
| BCLK_EN | |
| 1.3.1276BCTL[0..3]_DCLK_EN3 | 1660 |
| DCLK_EN | |
| 1.3.1277BCTL[0..3]_BCLK_EN3 | 1661 |
| BCLK_EN | |
| 1.3.1278IDMUX_IRQ_CTL[0..7] | 1664 |
| Control Register IRQ_CTL | |
| 1.3.1279IDMUX_DRQ_CTL[0..5] | 1665 |
| Configuration Register DRQ_CTL | |
| 1.3.1280CACHERAM_DATA[0..255] | 1666 |
| Cache SRAM | |
| 1.3.1281SFR_GPIO0 | 1667 |
| GPIO0 Register | |
| 1.3.1282SFR_GPIRD0 | 1668 |
| GPIRD0 Register | |
| 1.3.1283SFR_GPIO0_SEL | 1669 |
| GPIO0_SEL Register | |
| 1.3.1284SFR_GPIO1 | 1670 |
| GPIO1 Register | |
| 1.3.1285SFR_GPIRD1 | 1671 |
| GPIRD1 Register | |
| 1.3.1286SFR_GPIO2 | 1672 |
| GPIO2 Register | |
| 1.3.1287SFR_GPIRD2 | 1673 |
| GPIRD2 Register | |
| 1.3.1288SFR_GPIO2_SEL | 1674 |
| GPIO2_SEL Register | |
| 1.3.1289SFR_GPIO1_SEL | 1675 |
| GPIO1_SEL Register | |
| 1.3.1290SFR_GPIO3 | 1676 |
| GPIO3 Register | |
| 1.3.1291SFR_GPIRD3 | 1677 |
| GPIRD3 Register | |
| 1.3.1292SFR_GPIO3_SEL | 1678 |
| GPIO3_SEL Register | |
| 1.3.1293SFR_GPIO4 | 1679 |

| | |
|-------------------------|------|
| GPIO4 Register | |
| 1.3.1294SFR_GPIRD4 | 1680 |
| GPIRD4 Register | |
| 1.3.1295SFR_GPIO4_SEL | 1681 |
| GPIO4_SEL Register | |
| 1.3.1296SFR_GPIO5 | 1682 |
| GPIO5 Register | |
| 1.3.1297SFR_GPIRD5 | 1683 |
| GPIRD5 Register | |
| 1.3.1298SFR_GPIO5_SEL | 1684 |
| GPIO5_SEL Register | |
| 1.3.1299SFR_GPIO6 | 1685 |
| GPIO6 Register | |
| 1.3.1300SFR_GPIRD6 | 1686 |
| GPIRD6 Register | |
| 1.3.1301SFR_GPIO6_SEL | 1687 |
| GPIO6_SEL Register | |
| 1.3.1302SFR_GPIO12 | 1688 |
| GPIO12 Register | |
| 1.3.1303SFR_GPIRD12 | 1689 |
| GPIRD12 Register | |
| 1.3.1304SFR_GPIO12_SEL | 1690 |
| GPIO12_SEL Register | |
| 1.3.1305SFR_GPIO15 | 1691 |
| GPIO15 Register | |
| 1.3.1306SFR_GPIRD15 | 1692 |
| GPIRD15 Register | |
| 1.3.1307SFR_GPIO15_SEL | 1693 |
| GPIO15_SEL Register | |
| 1.3.1308TC_TST_CR1 | 1694 |
| Test Control Register 1 | |
| 1.3.1309TC_TST_CR2 | 1695 |
| Test Control Register 2 | |
| 1.3.1310TC_TST_CR3 | 1697 |
| Test Control Register 3 | |
| 1.3.1311TC_TST_CR4 | 1698 |
| Test Control Register 4 | |
| 1.3.1312TC_TST_CR5 | 1699 |
| Test Control Register 5 | |
| 1.3.1313TC_TST_CR6 | 1700 |
| Test Control Register 6 | |
| 1.3.1314TC_TST_KEY | 1701 |
| Test Key Register | |
| 1.3.1315TC_PM_CTRL | 1702 |
| Power Mode Control | |
| 1.3.1316P3BA_Y_START | 1703 |
| Y_START | |
| 1.3.1317P3BA_YROLL | 1704 |
| YROLL | |
| 1.3.1318P3BA_YCFG | 1705 |
| YCFG | |
| 1.3.1319P3BA_X_START1 | 1706 |
| X_START1 | |
| 1.3.1320P3BA_X_START2 | 1707 |

| | |
|---------------------------|------|
| X_START2 | |
| 1.3.1321P3BA_XROLL1 | 1708 |
| XROLL1 | |
| 1.3.1322P3BA_XROLL2 | 1709 |
| XROLL2 | |
| 1.3.1323P3BA_XINC | 1710 |
| XINC | |
| 1.3.1324P3BA_XCFG | 1711 |
| XCFG | |
| 1.3.1325P3BA_OFFSETADDR1 | 1712 |
| OFFSETADDR1 | |
| 1.3.1326P3BA_OFFSETADDR2 | 1713 |
| OFFSETADDR2 | |
| 1.3.1327P3BA_OFFSETADDR3 | 1714 |
| OFFSETADDR3 | |
| 1.3.1328P3BA_ABSADDR1 | 1715 |
| ABSADDR1 | |
| 1.3.1329P3BA_ABSADDR2 | 1716 |
| ABSADDR2 | |
| 1.3.1330P3BA_ABSADDR3 | 1717 |
| ABSADDR3 | |
| 1.3.1331P3BA_ABSADDR4 | 1718 |
| ABSADDR4 | |
| 1.3.1332P3BA_DATCFG1 | 1719 |
| DATCFG1 | |
| 1.3.1333P3BA_DATCFG2 | 1720 |
| DATCFG2 | |
| 1.3.1334P3BA_CMP_RSLT1 | 1721 |
| CMP_RSLT1 | |
| 1.3.1335P3BA_CMP_RSLT2 | 1722 |
| CMP_RSLT2 | |
| 1.3.1336P3BA_CMP_RSLT3 | 1723 |
| CMP_RSLT3 | |
| 1.3.1337P3BA_CMP_RSLT4 | 1724 |
| CMP_RSLT4 | |
| 1.3.1338P3BA_DATA_REG1 | 1725 |
| DATA_REG1 | |
| 1.3.1339P3BA_DATA_REG2 | 1726 |
| DATA_REG2 | |
| 1.3.1340P3BA_DATA_REG3 | 1727 |
| DATA_REG3 | |
| 1.3.1341P3BA_DATA_REG4 | 1728 |
| DATA_REG4 | |
| 1.3.1342P3BA_EXP_DATA1 | 1729 |
| EXP_DATA1 | |
| 1.3.1343P3BA_EXP_DATA2 | 1730 |
| EXP_DATA2 | |
| 1.3.1344P3BA_EXP_DATA3 | 1731 |
| EXP_DATA3 | |
| 1.3.1345P3BA_EXP_DATA4 | 1732 |
| EXP_DATA4 | |
| 1.3.1346P3BA_MSTR_HRDATA1 | 1733 |
| MSTR_HRDATA1 | |
| 1.3.1347P3BA_MSTR_HRDATA2 | 1734 |

| | |
|--------------------------------------|------|
| MSTR_HRDATA2 | |
| 1.3.1348P3BA_MSTR_HRDATA3 | 1735 |
| MSTR_HRDATA3 | |
| 1.3.1349P3BA_MSTR_HRDATA4 | 1736 |
| MSTR_HRDATA4 | |
| 1.3.1350P3BA_BIST_EN | 1737 |
| BIST_EN | |
| 1.3.1351P3BA_PHUB_MASTER_SSR | 1738 |
| PHUB_MASTER_SSR | |
| 1.3.1352P3BA_SEQCFG1 | 1739 |
| SEQCFG1 | |
| 1.3.1353P3BA_SEQCFG2 | 1740 |
| SEQCFG2 | |
| 1.3.1354P3BA_Y_CURR | 1741 |
| Y_CURR | |
| 1.3.1355P3BA_X_CURR1 | 1742 |
| X_CURR1 | |
| 1.3.1356P3BA_X_CURR2 | 1743 |
| X_CURR2 | |
| 1.3.1357PANTHER_STCALIB_CFG | 1744 |
| SYSTICK Calibration register | |
| 1.3.1358PANTHER_WAITPIPE | 1745 |
| Wait State Pipline | |
| 1.3.1359PANTHER_TRACE_CFG | 1747 |
| Debug Trace Configuration | |
| 1.3.1360PANTHER_DBG_CFG | 1748 |
| Embedded Trace Overflow Stall | |
| 1.3.1361PANTHER_CM3_LCKRST_STAT | 1749 |
| Status Register | |
| 1.3.1362PANTHER_DEVICE_ID | 1750 |
| Device Identification | |
| 1.3.1363FLSECC_DATA[0..32767] | 1751 |
| DATA | |
| 1.3.1364FLSHID_RSVD[0..127] | 1752 |
| RSVD | |
| 1.3.1365FLSHID_CUST_MDATA[0..127] | 1753 |
| Customer Meta Data | |
| 1.3.1366FLSHID_CUST_TABLES_Y_LOC | 1754 |
| Y location | |
| 1.3.1367FLSHID_CUST_TABLES_X_LOC | 1755 |
| X location | |
| 1.3.1368FLSHID_CUST_TABLES_WAFER_NUM | 1756 |
| Wafer Number | |
| 1.3.1369FLSHID_CUST_TABLES_LOT_LSB | 1757 |
| Lot Number LSB | |
| 1.3.1370FLSHID_CUST_TABLES_LOT_MSB | 1758 |
| Lot Number MSB | |
| 1.3.1371FLSHID_CUST_TABLES_WRK_WK | 1759 |
| Work Week | |
| 1.3.1372FLSHID_CUST_TABLES_FAB_YR | 1760 |
| Fab/Yr | |
| 1.3.1373FLSHID_CUST_TABLES_MINOR | 1761 |
| Minor Part Number | |
| 1.3.1374FLSHID_CUST_TABLES_IMO_3MHZ | 1762 |

| | |
|--|------|
| IMO Trim - 3 MHz | |
| 1.3.1375FLSHID_CUST_TABLES_IMO_6MHZ | 1763 |
| IMO Trim - 6 MHz | |
| 1.3.1376FLSHID_CUST_TABLES_IMO_12MHZ | 1764 |
| IMO Trim - 12 MHz | |
| 1.3.1377FLSHID_CUST_TABLES_IMO_24MHZ | 1765 |
| IMO Trim - 24 MHz | |
| 1.3.1378FLSHID_CUST_TABLES_IMO_67MHZ | 1766 |
| IMO Trim - 67 MHz | |
| 1.3.1379FLSHID_CUST_TABLES_IMO_80MHZ | 1767 |
| IMO Trim - 80 MHz | |
| 1.3.1380FLSHID_CUST_TABLES_IMO_92MHZ | 1768 |
| IMO Trim - 92 MHz | |
| 1.3.1381FLSHID_CUST_TABLES_IMO_USB | 1769 |
| IMO Trim - USB Mode | |
| 1.3.1382FLSHID_CUST_TABLES_CMP0_TR0_HS | 1770 |
| CMP0_TR0 High Speed | |
| 1.3.1383FLSHID_CUST_TABLES_CMP1_TR0_HS | 1771 |
| CMP1_TR0 High Speed | |
| 1.3.1384FLSHID_CUST_TABLES_CMP2_TR0_HS | 1772 |
| CMP2_TR0 High Speed | |
| 1.3.1385FLSHID_CUST_TABLES_CMP3_TR0_HS | 1773 |
| CMP3_TR0 High Speed | |
| 1.3.1386FLSHID_CUST_TABLES_CMP0_TR1_HS | 1774 |
| CMP0_TR1 High Speed | |
| 1.3.1387FLSHID_CUST_TABLES_CMP1_TR1_HS | 1775 |
| CMP1_TR1 High Speed | |
| 1.3.1388FLSHID_CUST_TABLES_CMP2_TR1_HS | 1776 |
| CMP2_TR1 High Speed | |
| 1.3.1389FLSHID_CUST_TABLES_CMP3_TR1_HS | 1777 |
| CMP3_TR1 High Speed | |
| 1.3.1390FLSHID_CUST_TABLES_DEC_M1 | 1778 |
| Decimator Trim - Mode 1 | |
| 1.3.1391FLSHID_CUST_TABLES_DEC_M2 | 1779 |
| Decimator Trim - mode 2 | |
| 1.3.1392FLSHID_CUST_TABLES_DEC_M3 | 1780 |
| Decimator Trim - mode 3 | |
| 1.3.1393FLSHID_CUST_TABLES_DEC_M4 | 1781 |
| Decimator Trim - mode 4 | |
| 1.3.1394FLSHID_CUST_TABLES_DEC_M5 | 1782 |
| Decimator Trim - mode 5 | |
| 1.3.1395FLSHID_CUST_TABLES_DEC_M6 | 1783 |
| Decimator Trim - mode 6 | |
| 1.3.1396FLSHID_CUST_TABLES_DEC_M7 | 1784 |
| Decimator Trim - Mode 7 | |
| 1.3.1397FLSHID_CUST_TABLES_DEC_M8 | 1785 |
| Decimator Trim - Mode 8 | |
| 1.3.1398FLSHID_CUST_TABLES_DAC0_M1 | 1786 |
| DAC0_TR Trim - Mode 1 | |
| 1.3.1399FLSHID_CUST_TABLES_DAC0_M2 | 1787 |
| DAC0_TR Trim - mode 2 | |
| 1.3.1400FLSHID_CUST_TABLES_DAC0_M3 | 1788 |
| DAC0_TR Trim - mode 3 | |
| 1.3.1401FLSHID_CUST_TABLES_DAC0_M4 | 1789 |

| | |
|------------------------------------|------|
| DAC0_TR Trim - mode 4 | |
| 1.3.1402FLSHID_CUST_TABLES_DAC0_M5 | 1790 |
| DAC0_TR Trim - mode 5 | |
| 1.3.1403FLSHID_CUST_TABLES_DAC0_M6 | 1791 |
| DAC0_TR Trim - mode 6 | |
| 1.3.1404FLSHID_CUST_TABLES_DAC0_M7 | 1792 |
| DAC0_TR Trim - mode 7 | |
| 1.3.1405FLSHID_CUST_TABLES_DAC0_M8 | 1793 |
| DAC0_TR Trim - mode 8 | |
| 1.3.1406FLSHID_CUST_TABLES_DAC2_M1 | 1794 |
| DAC2_TR Trim - Mode 1 | |
| 1.3.1407FLSHID_CUST_TABLES_DAC2_M2 | 1795 |
| DAC2_TR Trim - mode 2 | |
| 1.3.1408FLSHID_CUST_TABLES_DAC2_M3 | 1796 |
| DAC2_TR Trim - mode 3 | |
| 1.3.1409FLSHID_CUST_TABLES_DAC2_M4 | 1797 |
| DAC2_TR Trim - mode 4 | |
| 1.3.1410FLSHID_CUST_TABLES_DAC2_M5 | 1798 |
| DAC2_TR Trim - mode 5 | |
| 1.3.1411FLSHID_CUST_TABLES_DAC2_M6 | 1799 |
| DAC2_TR Trim - mode 6 | |
| 1.3.1412FLSHID_CUST_TABLES_DAC2_M7 | 1800 |
| DAC2_TR Trim - mode 7 | |
| 1.3.1413FLSHID_CUST_TABLES_DAC2_M8 | 1801 |
| DAC2_TR Trim - mode 8 | |
| 1.3.1414FLSHID_CUST_TABLES_DAC1_M1 | 1802 |
| DAC1_TR Trim - Mode 1 | |
| 1.3.1415FLSHID_CUST_TABLES_DAC1_M2 | 1803 |
| DAC1_TR Trim - mode 2 | |
| 1.3.1416FLSHID_CUST_TABLES_DAC1_M3 | 1804 |
| DAC1_TR Trim - mode 3 | |
| 1.3.1417FLSHID_CUST_TABLES_DAC1_M4 | 1805 |
| DAC1_TR Trim - mode 4 | |
| 1.3.1418FLSHID_CUST_TABLES_DAC1_M5 | 1806 |
| DAC1_TR Trim - mode 5 | |
| 1.3.1419FLSHID_CUST_TABLES_DAC1_M6 | 1807 |
| DAC1_TR Trim - mode 6 | |
| 1.3.1420FLSHID_CUST_TABLES_DAC1_M7 | 1808 |
| DAC1_TR Trim - mode 7 | |
| 1.3.1421FLSHID_CUST_TABLES_DAC1_M8 | 1809 |
| DAC1_TR Trim - mode 8 | |
| 1.3.1422FLSHID_CUST_TABLES_DAC3_M1 | 1810 |
| DAC3_TR Trim - Mode 1 | |
| 1.3.1423FLSHID_CUST_TABLES_DAC3_M2 | 1811 |
| DAC3_TR Trim - mode 2 | |
| 1.3.1424FLSHID_CUST_TABLES_DAC3_M3 | 1812 |
| DAC3_TR Trim - mode 3 | |
| 1.3.1425FLSHID_CUST_TABLES_DAC3_M4 | 1813 |
| DAC3_TR Trim - mode 4 | |
| 1.3.1426FLSHID_CUST_TABLES_DAC3_M5 | 1814 |
| DAC3_TR Trim - mode 5 | |
| 1.3.1427FLSHID_CUST_TABLES_DAC3_M6 | 1815 |
| DAC3_TR Trim - mode 6 | |
| 1.3.1428FLSHID_CUST_TABLES_DAC3_M7 | 1816 |

| | |
|---|------|
| DAC3_TR Trim - mode 7 | |
| 1.3.1429FLSHID_CUST_TABLES_DAC3_M8 | 1817 |
| DAC3_TR Trim - mode 8 | |
| 1.3.1430FLSHID_PETE_DATA[0..31] | 1818 |
| PE/TE Data | |
| 1.3.1431FLSHID_SPC_PARAMS[0..31] | 1819 |
| SPC Parameters | |
| 1.3.1432FLSHID_MFG_CFG_WNDG_CFG0 | 1820 |
| MLOGIC_WNDG_CFG0 Trim | |
| 1.3.1433FLSHID_MFG_CFG_WNDG_CFG1 | 1821 |
| MLOGIC_WNDG_CFG1 Trim | |
| 1.3.1434FLSHID_MFG_CFG_PWRSYS_BG_TR | 1822 |
| PWRSYS_BG_TR Trim | |
| 1.3.1435FLSHID_MFG_CFG_RESET_TR | 1823 |
| RESET_TR Trim | |
| 1.3.1436FLSHID_MFG_CFG_IMO_TR1 | 1824 |
| IMO_TR1 Trim | |
| 1.3.1437FLSHID_MFG_CFG_IMO_GAIN | 1825 |
| IMO_GAIN Trim | |
| 1.3.1438FLSHID_MFG_CFG_IMO_TR2 | 1826 |
| IMO_TR2 Trim | |
| 1.3.1439FLSHID_MFG_CFG_IMO_C36M | 1827 |
| IMO_C36M Trim | |
| 1.3.1440FLSHID_MFG_CFG_PWRSYS_BREF_TR | 1828 |
| PWRSYS_BREF_TR Trim | |
| 1.3.1441FLSHID_MFG_CFG_PWRSYS_BUZZ_TR | 1829 |
| PWRSYS_BUZZ_TR Trim | |
| 1.3.1442FLSHID_MFG_CFG_PWRSYS_I2C_TR | 1830 |
| PWRSYS_I2C_TR Trim | |
| 1.3.1443FLSHID_MFG_CFG_PWRSYS_HIB_TR0 | 1831 |
| PWRSYS_HIB_TR0 Trim | |
| 1.3.1444FLSHID_MFG_CFG_PWRSYS_HIB_TR1 | 1832 |
| PWRSYS_HIB_TR1 Trim | |
| 1.3.1445FLSHID_MFG_CFG_PWRSYS_SLP_TR | 1833 |
| PWRSYS_SLP_TR Trim | |
| 1.3.1446FLSHID_MFG_CFG_ILO_TR0 | 1834 |
| ILO_TR0 Trim | |
| 1.3.1447FLSHID_MFG_CFG_ILO_TR1 | 1835 |
| ILO_TR1 Trim | |
| 1.3.1448FLSHID_MFG_CFG_X32_TR | 1836 |
| X32_TR Trim | |
| 1.3.1449FLSHID_MFG_CFG_XMHZ_TR | 1837 |
| XMHZ_TR Trim | |
| 1.3.1450FLSHID_MFG_CFG_OPAMP0_TR0 | 1838 |
| OPAMP0_TR0 Trim | |
| 1.3.1451FLSHID_MFG_CFG_OPAMP1_TR0 | 1839 |
| OPAMP1_TR0 Trim | |
| 1.3.1452FLSHID_MFG_CFG_OPAMP2_TR0 | 1840 |
| OPAMP2_TR0 Trim | |
| 1.3.1453FLSHID_MFG_CFG_OPAMP3_TR0 | 1841 |
| OPAMP3_TR0 Trim | |
| 1.3.1454FLSHID_MFG_CFG_CMP0_TR0 | 1842 |
| CMP0_TR0 Trim | |
| 1.3.1455FLSHID_MFG_CFG_CMP1_TR0 | 1843 |

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| CMP1_TR0 Trim | |
| 1.3.1456FLSHID_MFG_CFG_CMP2_TR0 | 1844 |
| CMP2_TR0 Trim | |
| 1.3.1457FLSHID_MFG_CFG_CMP3_TR0 | 1845 |
| CMP3_TR0 Trim | |
| 1.3.1458FLSHID_MFG_CFG_CMP0_TR1 | 1846 |
| CMP0_TR1 Trim | |
| 1.3.1459FLSHID_MFG_CFG_CMP1_TR1 | 1847 |
| CMP1_TR1 Trim | |
| 1.3.1460FLSHID_MFG_CFG_CMP2_TR1 | 1848 |
| CMP2_TR1 Trim | |
| 1.3.1461FLSHID_MFG_CFG_CMP3_TR1 | 1849 |
| CMP3_TR1 Trim | |
| 1.3.1462FLSHID_MFG_CFG_IPOR_CR0 | 1850 |
| IPOR_CR0 Trim | |
| 1.3.1463FLSHID_MFG_CFG_IPOR_CR1 | 1851 |
| IPOR_CR1 Trim | |
| 1.3.1464FLSHID_MFG_CFG_IPOR_CR2 | 1852 |
| IPOR_CR2 Trim | |
| 1.3.1465FLSHID_MFG_CFG_IPOR_CR3 | 1853 |
| IPOR_CR3 Trim | |
| 1.3.1466FLSHID_MFG_CFG_DLY | 1854 |
| DLY Trim | |
| 1.3.1467FLSHID_MFG_CFG_RESERVED[0..3] | 1855 |
| Reserved | |
| 1.3.1468FLSHID_MFG_CFG_BG_XOVER_INL_TRIM | 1856 |
| Bandgap Crossover Trim | |
| 1.3.1469FLSHID_MFG_CFG_RSVD[0..15] | 1857 |
| Reserved | |
| 1.3.1470FLSHID_MFG_CFG_PWRSYS_WAKE_TR0 | 1858 |
| PWRSYS_WAKE_TR0 Trim | |
| 1.3.1471FLSHID_MFG_CFG_PWRSYS_WAKE_TR1 | 1859 |
| PWRSYS_WAKE_TR1 Trim | |
| 1.3.1472FLSHID_MFG_CFG_PWRSYS_WAKE_TR2 | 1860 |
| PWRSYS_WAKE_TR2 Trim | |
| 1.3.1473FLSHID_MFG_CFG_PWRSYS_WAKE_TR3 | 1861 |
| PWRSYS_WAKE_TR3 Trim | |
| 1.3.1474FLSHID_MFG_CFG_RSVD_2[0..2] | 1862 |
| Reserved | |
| 1.3.1475FLSHID_MFG_CFG_CHKSM | 1863 |
| Boot Checksum | |
| 1.3.1476EXTMEM_DATA[0..8388607] | 1864 |
| DATA | |
| 1.3.1477ITM_TRACE_EN | 1865 |
| ITM Trace Enable Register | |
| 1.3.1478ITM_TRACE_PRIVILEGE | 1866 |
| ITM Trace Privilege Register | |
| 1.3.1479ITM_TRACE_CTRL | 1867 |
| ITM Trace Control Register | |
| 1.3.1480ITM_LOCK_ACCESS | 1869 |
| ITM Lock Access Register | |
| 1.3.1481ITM_LOCK_STATUS | 1870 |
| ITM Lock Status Register | |
| 1.3.1482ITM_PID4 | 1871 |

| | |
|---|------|
| ITM Peripheral Identification Register 4 | |
| 1.3.1483ITM_PID5 | 1872 |
| ITM Peripheral Identification Register 5 | |
| 1.3.1484ITM_PID6 | 1873 |
| ITM Peripheral Identification Register 6 | |
| 1.3.1485ITM_PID7 | 1874 |
| ITM Peripheral Identification Register 7 | |
| 1.3.1486ITM_PID0 | 1875 |
| ITM Peripheral Identification Register 0 | |
| 1.3.1487ITM_PID1 | 1876 |
| ITM Peripheral Identification Register 1 | |
| 1.3.1488ITM_PID2 | 1877 |
| ITM Peripheral Identification Register 2 | |
| 1.3.1489ITM_PID3 | 1878 |
| ITM Peripheral Identification Register 3 | |
| 1.3.1490ITM_CID0 | 1879 |
| ITM Component Identification Register 0 | |
| 1.3.1491ITM_CID1 | 1880 |
| ITM Component Identification Register 1 | |
| 1.3.1492ITM_CID2 | 1881 |
| ITM Component Identification Register 2 | |
| 1.3.1493ITM_CID3 | 1882 |
| ITM Component Identification Register 3 | |
| 1.3.1494DWT_CTRL | 1883 |
| DWT Control Register | |
| 1.3.1495DWT_CYCLE_COUNT | 1886 |
| DWT Current PC Sampler Cycle Count Register | |
| 1.3.1496DWT_CPI_COUNT | 1887 |
| DWT CPI Count Register | |
| 1.3.1497DWT_EXC_OVHD_COUNT | 1888 |
| DWT Exception Overhead Count Register | |
| 1.3.1498DWT_SLEEP_COUNT | 1889 |
| DWT Sleep Count Register | |
| 1.3.1499DWT_LSU_COUNT | 1890 |
| DWT LSU Count Register | |
| 1.3.1500DWT_FOLD_COUNT | 1891 |
| DWT Fold Count Register | |
| 1.3.1501DWT_PC_SAMPLE | 1892 |
| DWT Program Counter Sample Register | |
| 1.3.1502DWT_COMP_0 | 1893 |
| DWT Comparator Registers | |
| 1.3.1503DWT_MASK_0 | 1894 |
| DWT Mask Registers | |
| 1.3.1504DWT_FUNCTION_0 | 1895 |
| DWT Function registers | |
| 1.3.1505DWT_COMP_1 | 1897 |
| DWT Comparator Registers | |
| 1.3.1506DWT_MASK_1 | 1898 |
| DWT Mask Registers | |
| 1.3.1507DWT_FUNCTION_1 | 1899 |
| DWT Function registers | |
| 1.3.1508DWT_COMP_2 | 1901 |
| DWT Comparator Registers | |
| 1.3.1509DWT_MASK_2 | 1902 |

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| DWT Mask Registers | |
| 1.3.1510DWT_FUNCTION_2 | 1903 |
| DWT Function registers | |
| 1.3.1511DWT_COMP_3 | 1904 |
| DWT Comparator Registers | |
| 1.3.1512DWT_MASK_3 | 1905 |
| DWT Mask Registers | |
| 1.3.1513DWT_FUNCTION_3 | 1906 |
| DWT Function registers | |
| 1.3.1514FPB_CTRL | 1907 |
| Flash Patch Control Register | |
| 1.3.1515FPB_REMAP | 1909 |
| Flash Patch Remap Register | |
| 1.3.1516FPB_FP_COMP_0 | 1910 |
| Flash Patch Comparator Registers | |
| 1.3.1517FPB_FP_COMP_1 | 1912 |
| Flash Patch Comparator Registers | |
| 1.3.1518FPB_FP_COMP_2 | 1914 |
| Flash Patch Comparator Registers | |
| 1.3.1519FPB_FP_COMP_3 | 1916 |
| Flash Patch Comparator Registers | |
| 1.3.1520FPB_FP_COMP_4 | 1918 |
| Flash Patch Comparator Registers | |
| 1.3.1521FPB_FP_COMP_5 | 1920 |
| Flash Patch Comparator Registers | |
| 1.3.1522FPB_FP_COMP_6 | 1922 |
| Flash Patch Comparator Registers | |
| 1.3.1523FPB_FP_COMP_7 | 1924 |
| Flash Patch Comparator Registers | |
| 1.3.1524FPB_PID4 | 1926 |
| FPB Peripheral Identification Register 4 | |
| 1.3.1525FPB_PID5 | 1927 |
| FPB Peripheral Identification Register 5 | |
| 1.3.1526FPB_PID6 | 1928 |
| FPB Peripheral Identification Register 6 | |
| 1.3.1527FPB_PID7 | 1929 |
| FPB Peripheral Identification Register 7 | |
| 1.3.1528FPB_PID0 | 1930 |
| FPB Peripheral Identification Register 0 | |
| 1.3.1529FPB_PID1 | 1931 |
| FPB Peripheral Identification Register 1 | |
| 1.3.1530FPB_PID2 | 1932 |
| FPB Peripheral Identification Register 2 | |
| 1.3.1531FPB_PID3 | 1933 |
| FPB Peripheral Identification Register 3 | |
| 1.3.1532FPB_CID0 | 1934 |
| FPB Component Identification Register 0 | |
| 1.3.1533FPB_CID1 | 1935 |
| FPB Component Identification Register 1 | |
| 1.3.1534FPB_CID2 | 1936 |
| FPB Component Identification Register 2 | |
| 1.3.1535FPB_CID3 | 1937 |
| FPB Component Identification Register 3 | |
| 1.3.1536NVIC_INT_CTL_TYPE | 1938 |

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|-------------------------------------|------|
| Interrupt Controller Type Register | |
| 1.3.1537NVIC_SYSTICK_CTL | 1939 |
| SYSTICK Control and Status register | |
| 1.3.1538NVIC_SYSTICK_RELOAD | 1940 |
| SYSTICK Reload value | |
| 1.3.1539NVIC_SYSTICK_CURRENT | 1941 |
| SYSTICK Counter | |
| 1.3.1540NVIC_SYSTICK_CAL | 1942 |
| SYSTICK Calibration register | |
| 1.3.1541NVIC_SETENA0 | 1943 |
| Interrupt Enable Set 0-31 | |
| 1.3.1542NVIC_CLRENA0 | 1944 |
| Interrupt Enable Clear 0-31 | |
| 1.3.1543NVIC_SETPEND0 | 1945 |
| Interrupt Pending Set 0-31 | |
| 1.3.1544NVIC_CLRPEND0 | 1946 |
| Interrupt Pending Clear 0-31 | |
| 1.3.1545NVIC_ACTIVE0 | 1947 |
| Active Interrupts 0-31 | |
| 1.3.1546NVIC_PRI_0 | 1948 |
| Interrupt Priority 0-31 | |
| 1.3.1547NVIC_PRI_1 | 1949 |
| Interrupt Priority 0-31 | |
| 1.3.1548NVIC_PRI_2 | 1950 |
| Interrupt Priority 0-31 | |
| 1.3.1549NVIC_PRI_3 | 1951 |
| Interrupt Priority 0-31 | |
| 1.3.1550NVIC_PRI_4 | 1952 |
| Interrupt Priority 0-31 | |
| 1.3.1551NVIC_PRI_5 | 1953 |
| Interrupt Priority 0-31 | |
| 1.3.1552NVIC_PRI_6 | 1954 |
| Interrupt Priority 0-31 | |
| 1.3.1553NVIC_PRI_7 | 1955 |
| Interrupt Priority 0-31 | |
| 1.3.1554NVIC_PRI_8 | 1956 |
| Interrupt Priority 0-31 | |
| 1.3.1555NVIC_PRI_9 | 1957 |
| Interrupt Priority 0-31 | |
| 1.3.1556NVIC_PRI_10 | 1958 |
| Interrupt Priority 0-31 | |
| 1.3.1557NVIC_PRI_11 | 1959 |
| Interrupt Priority 0-31 | |
| 1.3.1558NVIC_PRI_12 | 1960 |
| Interrupt Priority 0-31 | |
| 1.3.1559NVIC_PRI_13 | 1961 |
| Interrupt Priority 0-31 | |
| 1.3.1560NVIC_PRI_14 | 1962 |
| Interrupt Priority 0-31 | |
| 1.3.1561NVIC_PRI_15 | 1963 |
| Interrupt Priority 0-31 | |
| 1.3.1562NVIC_PRI_16 | 1964 |
| Interrupt Priority 0-31 | |
| 1.3.1563NVIC_PRI_17 | 1965 |

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| Interrupt Priority 0-31 | |
| 1.3.1564NVIC_PRI_18 | 1966 |
| Interrupt Priority 0-31 | |
| 1.3.1565NVIC_PRI_19 | 1967 |
| Interrupt Priority 0-31 | |
| 1.3.1566NVIC_PRI_20 | 1968 |
| Interrupt Priority 0-31 | |
| 1.3.1567NVIC_PRI_21 | 1969 |
| Interrupt Priority 0-31 | |
| 1.3.1568NVIC_PRI_22 | 1970 |
| Interrupt Priority 0-31 | |
| 1.3.1569NVIC_PRI_23 | 1971 |
| Interrupt Priority 0-31 | |
| 1.3.1570NVIC_PRI_24 | 1972 |
| Interrupt Priority 0-31 | |
| 1.3.1571NVIC_PRI_25 | 1973 |
| Interrupt Priority 0-31 | |
| 1.3.1572NVIC_PRI_26 | 1974 |
| Interrupt Priority 0-31 | |
| 1.3.1573NVIC_PRI_27 | 1975 |
| Interrupt Priority 0-31 | |
| 1.3.1574NVIC_PRI_28 | 1976 |
| Interrupt Priority 0-31 | |
| 1.3.1575NVIC_PRI_29 | 1977 |
| Interrupt Priority 0-31 | |
| 1.3.1576NVIC_PRI_30 | 1978 |
| Interrupt Priority 0-31 | |
| 1.3.1577NVIC_PRI_31 | 1979 |
| Interrupt Priority 0-31 | |
| 1.3.1578NVIC_CPUID_BASE | 1980 |
| CPU ID Base Register | |
| 1.3.1579NVIC_INTR_CTRL_STATE | 1981 |
| Interrupt Control State Register | |
| 1.3.1580NVIC_VECT_OFFSET | 1983 |
| Interrupt Vector Table Offset | |
| 1.3.1581NVIC_APPLN_INTR | 1984 |
| Application Interrupt and Reset Control Register | |
| 1.3.1582NVIC_SYSTEM_CONTROL | 1986 |
| System Control Register | |
| 1.3.1583NVIC_CFG_CONTROL | 1987 |
| Configuration Control Register | |
| 1.3.1584NVIC_SYS_PRIO_HANDLER_4_7 | 1989 |
| System Handler Priority Registers | |
| 1.3.1585NVIC_SYS_PRIO_HANDLER_8_11 | 1990 |
| System Handler Priority Registers | |
| 1.3.1586NVIC_SYS_PRIO_HANDLER_12_15 | 1991 |
| System Handler Priority Registers | |
| 1.3.1587NVIC_SYS_HANDLER_CSR | 1992 |
| System Handler Control and State Register | |
| 1.3.1588NVIC_MEMMAN_FAULT_STATUS | 1994 |
| Memory Manage Fault Status Registers. | |
| 1.3.1589NVIC_BUS_FAULT_STATUS | 1995 |
| Bus Fault Status Register | |
| 1.3.1590NVIC_USAGE_FAULT_STATUS | 1996 |

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| Usage Fault Status Register | |
| 1.3.1591NVIC_HARD_FAULT_STATUS | 1997 |
| Hard Fault Status Register | |
| 1.3.1592NVIC_DEBUG_FAULT_STATUS | 1998 |
| Debug Fault Status Register | |
| 1.3.1593NVIC_MEMMAN_FAULT_ADD | 2000 |
| Memory Manage Fault Address Register | |
| 1.3.1594NVIC_BUS_FAULT_ADD | 2001 |
| Bus Fault Address Register | |
| 1.3.1595CORE_DBG_DBG_HLT_CS | 2002 |
| Debug Halting Control and Status register | |
| 1.3.1596CORE_DBG_DBG_REG_SEL | 2004 |
| Debug Core Register Selector Register | |
| 1.3.1597CORE_DBG_DBG_REG_DATA | 2006 |
| Debug Core Register Data Register | |
| 1.3.1598CORE_DBG_EXC_MON_CTL | 2007 |
| Debug Exception and Monitor Control register | |
| 1.3.1599TPIU_SUPPORTED_SYNC_PRT_SZ | 2009 |
| Supported Sync Port Sizes Register | |
| 1.3.1600TPIU_CURRENT_SYNC_PRT_SZ | 2010 |
| Current Sync Port Size Register | |
| 1.3.1601TPIU_ASYNC_CLK_PRESCALER | 2011 |
| Async Clock Prescaler Register | |
| 1.3.1602TPIU_PROTOCOL | 2012 |
| Selected Pin Protocol Register | |
| 1.3.1603TPIU_FORM_FLUSH_STAT | 2013 |
| Formatter and Flush Status Register | |
| 1.3.1604TPIU_FORM_FLUSH_CTRL | 2014 |
| Formatter and Flush Control Register | |
| 1.3.1605TPIU_TRIGGER | 2015 |
| Integration test of the TRIGGER input. | |
| 1.3.1606TPIU_ITETMDATA | 2016 |
| Integration ETM Data | |
| 1.3.1607TPIU_ITATBCTR2 | 2017 |
| Integration Test Registers | |
| 1.3.1608TPIU_ITATBCTR0 | 2018 |
| Integration Test Registers | |
| 1.3.1609TPIU_ITITMDATA | 2019 |
| Integration ITM Data | |
| 1.3.1610TPIU_ITCTRL | 2020 |
| Integration Mode Control | |
| 1.3.1611TPIU_DEVID | 2021 |
| TPIU Provided Function Register | |
| 1.3.1612TPIU_DEVTYPE | 2023 |
| TPIU Device Type Identifier Register | |
| 1.3.1613TPIU_PID4 | 2024 |
| TPIU Peripheral Identification Register 4 | |
| 1.3.1614TPIU_PID5 | 2025 |
| TPIU Peripheral Identification Register 5 | |
| 1.3.1615TPIU_PID6 | 2026 |
| TPIU Peripheral Identification Register 6 | |
| 1.3.1616TPIU_PID7 | 2027 |
| TPIU Peripheral Identification Register 7 | |
| 1.3.1617TPIU_PID0 | 2028 |

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| TPIU Peripheral Identification Register 0 | |
| 1.3.1618TPIU_PID1 | 2029 |
| TPIU Peripheral Identification Register 1 | |
| 1.3.1619TPIU_PID2 | 2030 |
| TPIU Peripheral Identification Register 2 | |
| 1.3.1620TPIU_PID3 | 2031 |
| TPIU Peripheral Identification Register 3 | |
| 1.3.1621TPIU_CID0 | 2032 |
| TPIU Component Identification Register 0 | |
| 1.3.1622TPIU_CID1 | 2033 |
| TPIU Component Identification Register 1 | |
| 1.3.1623TPIU_CID2 | 2034 |
| TPIU Component Identification Register 2 | |
| 1.3.1624TPIU_CID3 | 2035 |
| TPIU Component Identification Register 3 | |
| 1.3.1625ETM_CTL | 2036 |
| ETM Control register | |
| 1.3.1626ETM_CFG_CODE | 2038 |
| ETM Configuration code register | |
| 1.3.1627ETM_TRIG_EVENT | 2040 |
| Trigger Event Register | |
| 1.3.1628ETM_STATUS | 2041 |
| ETM Status Register | |
| 1.3.1629ETM_SYS_CFG | 2042 |
| System Configuration Register | |
| 1.3.1630ETM_TRACE_ENB_EVENT | 2044 |
| Trace Enable Event Register | |
| 1.3.1631ETM_TRACE_EN_CTRL1 | 2045 |
| TraceEnable Control 1 Register | |
| 1.3.1632ETM_FIFOFULL_LEVEL | 2046 |
| FIFOFULL Level Register | |
| 1.3.1633ETM_SYNC_FREQ | 2047 |
| Synchronization Frequency Register | |
| 1.3.1634ETM_ETM_ID | 2048 |
| ETM ID Register | |
| 1.3.1635ETM_CFG_CODE_EXT | 2050 |
| Configuration Code Extension Register | |
| 1.3.1636ETM_TR_SS_EMBICE_CTRL | 2052 |
| Trace Start/Stop EmbeddedICE Control Register | |
| 1.3.1637ETM_CS_TRACE_ID | 2053 |
| CoreSight Trace ID Register | |
| 1.3.1638ETM_OS_LOCK_ACCESS | 2054 |
| OS Lock Access Register | |
| 1.3.1639ETM_OS_LOCK_STATUS | 2055 |
| OS Lock Status Register | |
| 1.3.1640ETM_PDSR | 2056 |
| Device Power-Down Status Register | |
| 1.3.1641ETM_ITMISCIN | 2057 |
| Integration Test Miscellaneous Inputs | |
| 1.3.1642ETM_ITTRIGOUT | 2058 |
| Integration Test Trigger Out | |
| 1.3.1643ETM_ITATBCTR2 | 2059 |
| ETM Integration Test ATB Control 2 | |
| 1.3.1644ETM_ITATBCTR0 | 2060 |

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| ETM Integration Test ATB Control 0 | |
| 1.3.1645ETM_INT_MODE_CTRL | 2061 |
| Integration Mode Control Register | |
| 1.3.1646ETM_CLM_TAG_SET | 2062 |
| Claim Tag Set Register | |
| 1.3.1647ETM_CLM_TAG_CLR | 2063 |
| Claim Tag Clear Register | |
| 1.3.1648ETM_LOCK_ACCESS | 2064 |
| Lock Access Register | |
| 1.3.1649ETM_LOCK_STATUS | 2065 |
| Lock Status Register | |
| 1.3.1650ETM_AUTH_STATUS | 2066 |
| Authentication Status Register | |
| 1.3.1651ETM_DEV_TYPE | 2067 |
| Device Type Register | |
| 1.3.1652ETM_PID4 | 2068 |
| ETM Peripheral Identification Register 4 | |
| 1.3.1653ETM_PID5 | 2069 |
| ETM Peripheral Identification Register 5 | |
| 1.3.1654ETM_PID6 | 2070 |
| ETM Peripheral Identification Register 6 | |
| 1.3.1655ETM_PID7 | 2071 |
| ETM Peripheral Identification Register 7 | |
| 1.3.1656ETM_PID0 | 2072 |
| ETM Peripheral Identification Register 0 | |
| 1.3.1657ETM_PID1 | 2073 |
| ETM Peripheral Identification Register 1 | |
| 1.3.1658ETM_PID2 | 2074 |
| ETM Peripheral Identification Register 2 | |
| 1.3.1659ETM_PID3 | 2075 |
| ETM Peripheral Identification Register 3 | |
| 1.3.1660ETM_CID0 | 2076 |
| ETM Component Identification Register 0 | |
| 1.3.1661ETM_CID1 | 2077 |
| ETM Component Identification Register 1 | |
| 1.3.1662ETM_CID2 | 2078 |
| ETM Component Identification Register 2 | |
| 1.3.1663ETM_CID3 | 2079 |
| ETM Component Identification Register 3 | |
| 1.3.1664ROM_TABLE_NVIC | 2080 |
| NVIC | |
| 1.3.1665ROM_TABLE_DWT | 2081 |
| DWT | |
| 1.3.1666ROM_TABLE_FPB | 2082 |
| FPB | |
| 1.3.1667ROM_TABLE_ITM | 2083 |
| ITM | |
| 1.3.1668ROM_TABLE_TPIU | 2084 |
| TPIU | |
| 1.3.1669ROM_TABLE_ETM | 2085 |
| ETM | |
| 1.3.1670ROM_TABLE_END | 2086 |
| END | |
| 1.3.1671ROM_TABLE_MEMTYPE | 2087 |

| | |
|----------|--|
| MEMTYPE | |
| 1.3.1672 | ROM_TABLE_PID42088 |
| | ROM Table Peripheral Identification Register 4 |
| 1.3.1673 | ROM_TABLE_PID52089 |
| | ROM Table Peripheral Identification Register 5 |
| 1.3.1674 | ROM_TABLE_PID62090 |
| | ROM Table Peripheral Identification Register 6 |
| 1.3.1675 | ROM_TABLE_PID72091 |
| | ROM Table Peripheral Identification Register 7 |
| 1.3.1676 | ROM_TABLE_PID02092 |
| | ROM Table Peripheral Identification Register 0 |
| 1.3.1677 | ROM_TABLE_PID12093 |
| | ROM Table Peripheral Identification Register 1 |
| 1.3.1678 | ROM_TABLE_PID22094 |
| | ROM Table Peripheral Identification Register 2 |
| 1.3.1679 | ROM_TABLE_PID32095 |
| | ROM Table Peripheral Identification Register 3 |
| 1.3.1680 | ROM_TABLE_CID02096 |
| | ROM Table Component Identification Register 0 |
| 1.3.1681 | ROM_TABLE_CID12097 |
| | ROM Table Component Identification Register 1 |
| 1.3.1682 | ROM_TABLE_CID22098 |
| | ROM Table Component Identification Register 2 |
| 1.3.1683 | ROM_TABLE_CID32099 |
| | ROM Table Component Identification Register 3 |

Register Mapping



Register Mapping discusses the registers of the PSoC 5LP device. It lists all the registers in mapping tables, in address order.

See the *PSoC 5LP Architecture TRM (Technical Reference Manual)* for complete functionality.

1.1 Maneuvering Around the Registers

For ease-of-use, this chapter is formatted so that there is one register per page, although some registers use two pages. On each page, from top to bottom, there are four sections:

1. Register name and address (from lowest to highest).
2. Register table showing the bit organization, with reserved bits grayed out.
3. Written description of register specifics or links to additional register information.
4. Detailed register bit descriptions.

1.2 Register Conventions

The following table lists the register conventions.

| Convention | Example | Description |
|------------------------------|----------|---|
| 'x' in a register name | ACBxxCR1 | Multiple instances/address ranges of the same register |
| R | R : 00 | Read register or bit(s) |
| W | W : 00 | Write register or bit(s) |
| WOC | WOC:0 | Write one to clear |
| WZC | WZC:0 | Write zero to clear |
| RC | RC:0 | Read to clear |
| WC | WC:0 | Write to clear |
| NA | NA:000 | Reserved |
| U | R:U | Undefined |
| 00 | RW : 00 | Reset value is 0x00 |
| XX | RW : XX | Register is not reset |
| Empty, grayed out table cell | | Reserved bit or group of bits, unless otherwise stated. Write reserved bits to zero. Software cannot make any assumptions about return values. |

1.3 PSoC 5LP Register Map

The PSoC 5LP device has a total register address space of 4 GB (32-bit addressing scheme).

| Register Name | Purpose | Address |
|-------------------------|--|----------------------------------|
| FLASH_DATA[0..262143] | DATA | @[0..262143 * 0x1] |
| SRAM_CODE64K[0..16383] | Code System Memory Bank | @0x1fff8000 + [0..16383 * 0x1] |
| SRAM_CODE32K[0..8191] | Code System Memory Bank | @0x1ffc000 + [0..8191 * 0x1] |
| SRAM_CODE16K[0..4095] | Code System Memory Bank | @0x1ffe000 + [0..4095 * 0x1] |
| SRAM_CODE[0..4095] | Code System Memory Bank | @0x1fff000 + [0..4095 * 0x1] |
| SRAM_DATA[0..4095] | Data System Memory Bank | @0x20000000 + [0..4095 * 0x1] |
| SRAM_DATA16K[0..4095] | Data System Memory Bank | @0x20001000 + [0..4095 * 0x1] |
| SRAM_DATA32K[0..8191] | Data System Memory Bank | @0x20002000 + [0..8191 * 0x1] |
| SRAM_DATA64K[0..16383] | Data System Memory Bank | @0x20004000 + [0..16383 * 0x1] |
| DMA_SRAM64K[0..16383] | Data System Memory Bank | @0x20008000 + [0..16383 * 0x1] |
| DMA_SRAM32K[0..8191] | Data System Memory Bank | @0x2000c000 + [0..8191 * 0x1] |
| DMA_SRAM16K[0..4095] | Data System Memory Bank | @0x2000e000 + [0..4095 * 0x1] |
| DMA_SRAM[0..4095] | Data System Memory Bank | @0x2000f000 + [0..4095 * 0x1] |
| CLKDIST_CR | Configuration Register CR | 0x40004000 |
| CLKDIST_LD | LOAD Register | 0x40004001 |
| CLKDIST_WRK0 | LSB Shadow Divider Value Register | 0x40004002 |
| CLKDIST_WRK1 | MSB Shadow Divider Value Register | 0x40004003 |
| CLKDIST_MSTR0 | Master clock (clk_sync_d) Divider Value Register | 0x40004004 |
| CLKDIST_MSTR1 | Master (clk_sync_d) Configuration Register/CPU Divider Value | 0x40004005 |
| CLKDIST_BCFG0 | CLK_BUS LSB Divider Value Register | 0x40004006 |
| CLKDIST_BCFG1 | CLK_BUS MSB Divider Value Register | 0x40004007 |
| CLKDIST_BCFG2 | CLK_BUS Configuration Register | 0x40004008 |
| CLKDIST_UCFG | USB Configuration Register | 0x40004009 |
| CLKDIST_DLY0 | Delay block Configuration Register | 0x4000400a |
| CLKDIST_DLY1 | Delay block Configuration Register | 0x4000400b |
| CLKDIST_DMASK | Digital Clock Mask Register | 0x40004010 |
| CLKDIST_AMASK | Analog Clock Mask Register | 0x40004014 |
| CLKDIST_DCFG[0..7]_CFG0 | LSB Divider Value Register | @0x40004080 + [0..7 * 0x4] |
| CLKDIST_DCFG[0..7]_CFG1 | MSB Divider Value Register | @0x40004080 + [0..7 * 0x4] + 0x1 |
| CLKDIST_DCFG[0..7]_CFG2 | Configuration Register | @0x40004080 + [0..7 * 0x4] + 0x2 |
| CLKDIST_ACFG[0..3]_CFG0 | LSB Divider Value Register | @0x40004100 + [0..3 * 0x4] |
| CLKDIST_ACFG[0..3]_CFG1 | MSB Divider Value Register | @0x40004100 + [0..3 * 0x4] + 0x1 |
| CLKDIST_ACFG[0..3]_CFG2 | Configuration Register | @0x40004100 + [0..3 * 0x4] + 0x2 |
| CLKDIST_ACFG[0..3]_CFG3 | Analog clocks Configuration Register | @0x40004100 + [0..3 * 0x4] + 0x3 |
| FASTCLK_IMO_CR | Internal Main Oscillator Control Register | 0x40004200 |
| FASTCLK_XMHZ_CSR | External 4-25 MHz Crystal Oscillator Status and Control Register | 0x40004210 |
| FASTCLK_XMHZ_TST | External 4-25 MHz Crystal Oscillator Test Register | 0x40004211 |
| FASTCLK_XMHZ_CFG0 | External 4-25 MHz Crystal Oscillator Configuration Register 0 | 0x40004212 |

| Register Name | Purpose | Address |
|-------------------|---|------------|
| FASTCLK_XMHZ_CFG1 | External 4-25 MHz Crystal Oscillator Configuration Register 1 | 0x40004213 |
| FASTCLK_PLL_CFG0 | PLL Configuration Register | 0x40004220 |
| FASTCLK_PLL_CFG1 | PLL Control Register | 0x40004221 |
| FASTCLK_PLL_P | PLL P-Counter Configuration Register | 0x40004222 |
| FASTCLK_PLL_Q | PLL Q-Counter Configuration Register | 0x40004223 |
| FASTCLK_PLL_TST | PLL Test Register | 0x40004224 |
| FASTCLK_PLL_SR | PLL Status Register | 0x40004225 |
| SLOWCLK_ILO_CR0 | Internal Low-speed Oscillator Control Register 0 | 0x40004300 |
| SLOWCLK_ILO_CR1 | Internal Low-speed Oscillator Control Register 1 | 0x40004301 |
| SLOWCLK_X32_CR | External 32kHz Crystal Oscillator Control Register | 0x40004308 |
| SLOWCLK_X32_CFG | External 32kHz Crystal Oscillator Configuration Register | 0x40004309 |
| SLOWCLK_X32_TST | External 32kHz Crystal Oscillator Test Register | 0x4000430a |
| BOOST_CR0 | Boost Control 0 | 0x40004320 |
| BOOST_CR1 | Boost Control 1 | 0x40004321 |
| BOOST_CR2 | Boost Control 2 | 0x40004322 |
| BOOST_CR3 | Boost Control 3 | 0x40004323 |
| BOOST_SR | Boost Status | 0x40004324 |
| BOOST_CR4 | Boost Control Register 4 | 0x40004325 |
| BOOST_SR2 | Boost Status Register 2 | 0x40004326 |
| PWRSYS_CR0 | Power System Control Register 0 | 0x40004330 |
| PWRSYS_CR1 | Power System Control Register 1 | 0x40004331 |
| PM_TW_CFG0 | Timewheel Configuration Register 0 | 0x40004380 |
| PM_TW_CFG1 | Timewheel Configuration Register 1 | 0x40004381 |
| PM_TW_CFG2 | Timewheel Configuration Register 2 | 0x40004382 |
| PM_WDT_CFG | Watchdog Timer Configuration Register | 0x40004383 |
| PM_WDT_CR | Watchdog Timer Control Register | 0x40004384 |
| PM_INT_SR | Power Manager Interrupt Status Register | 0x40004390 |
| PM_MODE_CFG0 | Power Mode Configuration Register 0 | 0x40004391 |
| PM_MODE_CFG1 | Power Mode Configuration Register 1 | 0x40004392 |
| PM_MODE_CSR | Power Mode Control/Status Register | 0x40004393 |
| PM_USB_CR0 | USB Power Mode Control Register 0 | 0x40004394 |
| PM_WAKEUP_CFG0 | Power Mode Wakeup Mask Configuration Register 0 | 0x40004398 |
| PM_WAKEUP_CFG1 | Power Mode Wakeup Mask Configuration Register 1 | 0x40004399 |
| PM_WAKEUP_CFG2 | Power Mode Wakeup Mask Configuration Register 2 | 0x4000439a |
| PM_ACT_CFG0 | Active Power Mode Configuration Register 0 | 0x400043a0 |
| PM_ACT_CFG1 | Active Power Mode Configuration Register 1 | 0x400043a1 |
| PM_ACT_CFG2 | Active Power Mode Configuration Register 2 | 0x400043a2 |
| PM_ACT_CFG3 | Active Power Mode Configuration Register 3 | 0x400043a3 |
| PM_ACT_CFG4 | Active Power Mode Configuration Register 4 | 0x400043a4 |
| PM_ACT_CFG5 | Active Power Mode Configuration Register 5 | 0x400043a5 |

| Register Name | Purpose | Address |
|---------------------------|---|--|
| PM_ACT_CFG6 | Active Power Mode Configuration Register 6 | 0x400043a6 |
| PM_ACT_CFG7 | Active Power Mode Configuration Register 7 | 0x400043a7 |
| PM_ACT_CFG8 | Active Power Mode Configuration Register 8 | 0x400043a8 |
| PM_ACT_CFG9 | Active Power Mode Configuration Register 9 | 0x400043a9 |
| PM_ACT_CFG10 | Active Power Mode Configuration Register 10 | 0x400043aa |
| PM_ACT_CFG11 | Active Power Mode Configuration Register 11 | 0x400043ab |
| PM_ACT_CFG12 | Active Power Mode Configuration Register 12 | 0x400043ac |
| PM_ACT_CFG13 | Active Power Mode Configuration Register 13 | 0x400043ad |
| PM_STBY_CFG0 | Standby Power Mode Configuration Register 0 | 0x400043b0 |
| PM_STBY_CFG1 | Standby Power Mode Configuration Register 1 | 0x400043b1 |
| PM_STBY_CFG2 | Standby Power Mode Configuration Register 2 | 0x400043b2 |
| PM_STBY_CFG3 | Standby Power Mode Configuration Register 3 | 0x400043b3 |
| PM_STBY_CFG4 | Standby Power Mode Configuration Register 4 | 0x400043b4 |
| PM_STBY_CFG5 | Standby Power Mode Configuration Register 5 | 0x400043b5 |
| PM_STBY_CFG6 | Standby Power Mode Configuration Register 6 | 0x400043b6 |
| PM_STBY_CFG7 | Standby Power Mode Configuration Register 7 | 0x400043b7 |
| PM_STBY_CFG8 | Standby Power Mode Configuration Register 8 | 0x400043b8 |
| PM_STBY_CFG9 | Standby Power Mode Configuration Register 9 | 0x400043b9 |
| PM_STBY_CFG10 | Standby Power Mode Configuration Register 10 | 0x400043ba |
| PM_STBY_CFG11 | Standby Power Mode Configuration Register 11 | 0x400043bb |
| PM_STBY_CFG12 | Standby Power Mode Configuration Register 12 | 0x400043bc |
| PM_STBY_CFG13 | Standby Power Mode Configuration Register 13 | 0x400043bd |
| PM_AVAIL_CR0 | Power Mode Available Subsystem Control Register 0 | 0x400043c0 |
| PM_AVAIL_CR1 | Power Mode Available Subsystem Control Register 1 | 0x400043c1 |
| PM_AVAIL_CR2 | Power Mode Available Subsystem Control Register 2 | 0x400043c2 |
| PM_AVAIL_CR3 | Power Mode Available Subsystem Control Register 3 | 0x400043c3 |
| PM_AVAIL_CR4 | Power Mode Available Subsystem Control Register 4 | 0x400043c4 |
| PM_AVAIL_CR5 | Power Mode Available Subsystem Control Register 5 | 0x400043c5 |
| PM_AVAIL_CR6 | Power Mode Available Subsystem Control Register 6 | 0x400043c6 |
| PM_AVAIL_SR0 | Power Mode Available Subsystem Status Register 0 | 0x400043d0 |
| PM_AVAIL_SR1 | Power Mode Available Subsystem Status Register 1 | 0x400043d1 |
| PM_AVAIL_SR2 | Power Mode Available Subsystem Status Register 2 | 0x400043d2 |
| PM_AVAIL_SR3 | Power Mode Available Subsystem Status Register 3 | 0x400043d3 |
| PM_AVAIL_SR4 | Power Mode Available Subsystem Status Register 4 | 0x400043d4 |
| PM_AVAIL_SR5 | Power Mode Available Subsystem Status Register 5 | 0x400043d5 |
| PM_AVAIL_SR6 | Power Mode Available Subsystem Status Register 6 | 0x400043d6 |
| PICU[0..15]_INTTYPE[0..7] | Port Interrupt Control Type Register | @(0x40004500 + [0..15 * 0x8]) + [0..7 * 0x1] |
| PICU[0..15]_INTSTAT | Port Interrupt Control Status Register | @0x40004580 + [0..15 * 0x1] |
| PICU[0..15]_SNAP | Port Interrupt Control Snap Shot Register | @0x40004590 + [0..15 * 0x1] |

| Register Name | Purpose | Address |
|-------------------------|---|----------------------------------|
| PICU[0..15]_DISABLE_COR | Disable Status Register Clear on Read Feature | @0x400045a0 + [0..15 * 0x1] |
| DAC[0..3]_TR | DAC Block Trim Register | @0x40004608 + [0..3 * 0x1] |
| NPUMP_DSM_TR0 | Delta Sigma Modulator (DSM) Negative Pump Trim Register 0 | 0x40004610 |
| NPUMP_SC_TR0 | Switched Cap Negative Pump Trim Register 0 | 0x40004611 |
| NPUMP_OPAMP_TR0 | Analog Linear Output Buffer (OPAMP) Negative Pump Trim Register 0 | 0x40004612 |
| SAR[0..1]_TR0 | SAR trim register 0 | @0x40004614 + [0..1 * 0x2] |
| OPAMP[0..3]_TR0 | Analog Output Buffer Trim Register 0 | @0x40004620 + [0..3 * 0x2] |
| OPAMP[0..3]_TR1 | Analog Output Buffer Trim Register 1 | @0x40004620 + [0..3 * 0x2] + 0x1 |
| CMP[0..3]_TR0 | Comparator Trim Register | @0x40004630 + [0..3 * 0x2] |
| CMP[0..3]_TR1 | Comparator Trim Register | @0x40004630 + [0..3 * 0x2] + 0x1 |
| PWRSYS_HIB_TR0 | Hibernate Trim Register 0 | 0x40004680 |
| PWRSYS_HIB_TR1 | Hibernate Trim Register 1 | 0x40004681 |
| PWRSYS_I2C_TR | I2C Regulator Trim Register 1 | 0x40004682 |
| PWRSYS_SLP_TR | Sleep Regulator Trim Register | 0x40004683 |
| PWRSYS_BUZZ_TR | Power Mode Buzz Trim Register | 0x40004684 |
| PWRSYS_WAKE_TR0 | Power Mode Wakeup Trim Register 0 | 0x40004685 |
| PWRSYS_WAKE_TR1 | Power Mode Wakeup Trim Register 1 | 0x40004686 |
| PWRSYS_BREF_TR | Boot Reference Trim Register | 0x40004687 |
| PWRSYS_BG_TR | Bandgap Trim | 0x40004688 |
| PWRSYS_WAKE_TR2 | Power Mode Wakeup Trim Register 2 | 0x40004689 |
| PWRSYS_WAKE_TR3 | Power Mode Wakeup Trim Register 3 | 0x4000468a |
| ILO_TR0 | Internal Low-speed Oscillator Trim Register | 0x40004690 |
| ILO_TR1 | Internal Low-speed Oscillator Coarse Trim Register | 0x40004691 |
| X32_TR | 32 kHz Watch Crystal Oscillator Trim Register | 0x40004698 |
| IMO_TR0 | Internal Main Oscillator Trim Register 0 | 0x400046a0 |
| IMO_TR1 | Internal Main Oscillator Trim Register 1 | 0x400046a1 |
| IMO_GAIN | Internal Main Oscillator Gain Trim Register | 0x400046a2 |
| IMO_C36M | Internal Main Oscillator 36 MHz clock control register {INTERNAL} | 0x400046a3 |
| IMO_TR2 | Internal Main Oscillator Trim Register 2 | 0x400046a4 |
| XMHZ_TR | External 4-25 MHz Crystal Oscillator Trim Register | 0x400046a8 |
| DLY | Delay block Configuration Register | 0x400046c0 |
| MLOGIC_WNDG_CFG0 | MLogic Wounding Register 0 | 0x400046e0 |
| MLOGIC_WNDG_CFG1 | MLogic Wounding Register 1 | 0x400046e1 |
| MLOGIC_DMPSTR | Dumpster Register | 0x400046e2 |
| MLOGIC_SEG_CR | Segment Control Register | 0x400046e4 |
| MLOGIC_SEG_CFG0 | Segment Configuration Register | 0x400046e5 |
| MLOGIC_DEBUG | MLOGIC Debug Register | 0x400046e8 |
| MLOGIC_CPU_SCR_CPU_SCR | System Status and Control Register | 0x400046ea |
| MLOGIC_REV_ID | Silicon Revision ID | 0x400046ec |
| RESET_IPOR_CR0 | Imprecise Power On Reset Control Register 0 | 0x400046f0 |
| RESET_IPOR_CR1 | Imprecise Power On Reset Control Register 1 | 0x400046f1 |

| Register Name | Purpose | Address |
|--------------------------|---|------------------------------|
| RESET_IPOR_CR2 | Imprecise Power On Reset Control Register 2 | 0x400046f2 |
| RESET_IPOR_CR3 | Imprecise Power On Reset Control Register 3 | 0x400046f3 |
| RESET_CR0 | LVI Set Point Control Register | 0x400046f4 |
| RESET_CR1 | Reset System Control Register | 0x400046f5 |
| RESET_CR2 | Software Reset Control Register | 0x400046f6 |
| RESET_CR3 | LVD/POR Mode Control Register | 0x400046f7 |
| RESET_CR4 | Reset Ignore Control Register | 0x400046f8 |
| RESET_CR5 | Reset Ignore Control Register | 0x400046f9 |
| RESET_SR0 | Reset and Voltage Detection Status Register 0 | 0x400046fa |
| RESET_SR1 | Reset and Voltage Detection Status Register 1 | 0x400046fb |
| RESET_SR2 | Reset and Voltage Detection Status Register 2 | 0x400046fc |
| RESET_SR3 | Reset and Voltage Detection Status Register 3 | 0x400046fd |
| RESET_TR | PRES Trim Register | 0x400046fe |
| SPC_FM_EE_CR | FM_EE_CR | 0x40004700 |
| SPC_FM_EE_WAKE_CNT | FM_EE_WAKE_CNT | 0x40004701 |
| SPC_EE_SCR | EEPROM Status & Control Register | 0x40004702 |
| SPC_EE_ERR | EEPROM Error Register | 0x40004703 |
| SPC_CPU_DATA | SPC CPU Data Register | 0x40004720 |
| SPC_DMA_DATA | SPC DMA Data Register | 0x40004721 |
| SPC_SR | SPC Status Register | 0x40004722 |
| SPC_CR | SPC Control Register | 0x40004723 |
| SPC_DMM_MAP_SRAM[0..127] | SPC Direct Memory Mapping | @0x40004780 + [0..127 * 0x1] |
| CACHE_CC_CTL | Cache Control Register | 0x40004800 |
| CACHE_ECC_CORR | Error Correction detected | 0x40004880 |
| CACHE_ECC_ERR | Error Correction failed | 0x40004888 |
| CACHE_FLASH_ERR | FLASH error | 0x40004890 |
| CACHE_HITMISS | HIT/MISS counters | 0x40004898 |
| I2C_XCFG | I2C Extended Configuration Register | 0x400049c8 |
| I2C_ADR | I2C Slave Address Register | 0x400049ca |
| I2C_CFG | I2C Configuration Register | 0x400049d6 |
| I2C_CSR | I2C Control and Status Register | 0x400049d7 |
| I2C_D | I2C Data Register | 0x400049d8 |
| I2C_MCSR | I2C Master Control and Status Register | 0x400049d9 |
| I2C_CLK_DIV1 | I2C Clock Divide Factor Register-1 | 0x400049db |
| I2C_CLK_DIV2 | I2C Clock Divide Factor Register-2 | 0x400049dc |
| I2C_TMOUT_CSR | I2C TIMEOUT CSR. | 0x400049dd |
| I2C_TMOUT_SR | I2C TIMEOUT SR. | 0x400049de |
| I2C_TMOUT_CFG0 | I2C TIMEOUT Period Configuration | 0x400049df |
| I2C_TMOUT_CFG1 | I2C TIMEOUT Period Configuration | 0x400049e0 |
| DEC_CR | Decimator Control Register | 0x40004e00 |
| DEC_SR | Decimator Status Register | 0x40004e01 |
| DEC_SHIFT1 | Decimator Shifter 1 (Input) | 0x40004e02 |

| Register Name | Purpose | Address |
|--------------------------|---|---|
| DEC_SHIFT2 | Decimator Shifter 2 (Output) | 0x40004e03 |
| DEC_DR2 | Decimator Decimation Rate (2) | 0x40004e04 |
| DEC_DR2H | Decimator Decimation Rate (2) and Overflow Correction | 0x40004e05 |
| DEC_DR1 | Decimator Decimation Rate (1) of CIC Filter | 0x40004e06 |
| DEC_OCOR | Decimator Offset Correction Coefficient (Low Byte) | 0x40004e08 |
| DEC_OCORM | Decimator Offset Correction Coefficient (Middle Byte) | 0x40004e09 |
| DEC_OCORH | Decimator Offset Correction Coefficient (High Byte) | 0x40004e0a |
| DEC_GCOR | Decimator Gain Correction Coefficient (Low Byte) | 0x40004e0c |
| DEC_GCORH | Decimator Gain Correction Coefficient (High Byte) | 0x40004e0d |
| DEC_GVAL | Decimator Gain Correction Size Register | 0x40004e0e |
| DEC_OUTSAMP | Decimator Output Data Sample (Low Byte) | 0x40004e10 |
| DEC_OUTSAMPM | Decimator Output Data Sample (Middle Byte) | 0x40004e11 |
| DEC_OUTSAMPH | Decimator Output Data Sample (High Byte) | 0x40004e12 |
| DEC_OUTSAMPS | Decimator Output Data Sample (Sign Extension) | 0x40004e13 |
| DEC_COHER | Decimator Coherency Register | 0x40004e14 |
| TMR[0..3]_CFG0 | Configuration Register CFG0 | @0x40004f00 + [0..3 * 0xc] |
| TMR[0..3]_CFG1 | Configuration Register CFG1 | @0x40004f00 + [0..3 * 0xc] + 0x1 |
| TMR[0..3]_CFG2 | Configuration Register CFG2 | @0x40004f00 + [0..3 * 0xc] + 0x2 |
| TMR[0..3]_SR0 | Status Register SR0 | @0x40004f00 + [0..3 * 0xc] + 0x3 |
| TMR[0..3]_PER0 | Timer Period Register PER0 | @0x40004f00 + [0..3 * 0xc] + 0x4 |
| TMR[0..3]_PER1 | Timer Period Register PER1 | @0x40004f00 + [0..3 * 0xc] + 0x5 |
| TMR[0..3]_CNT_CMP0 | Count/Comparator value CNT/CMP0 | @0x40004f00 + [0..3 * 0xc] + 0x6 |
| TMR[0..3]_CNT_CMP1 | Count/Comparator value CNT/CMP1 | @0x40004f00 + [0..3 * 0xc] + 0x7 |
| TMR[0..3]_CAP0 | Capture Value CAP0 | @0x40004f00 + [0..3 * 0xc] + 0x8 |
| TMR[0..3]_CAP1 | Capture Value CAP1 | @0x40004f00 + [0..3 * 0xc] + 0x9 |
| TMR[0..3]_RT0 | Configuration Register RT0 | @0x40004f00 + [0..3 * 0xc] + 0xa |
| TMR[0..3]_RT1 | Configuration Register RT1 | @0x40004f00 + [0..3 * 0xc] + 0xb |
| PRT[0..14]_PC[0..7] | Port Pin Configuration Register | @(0x40005000 + [0..14 * 0x8]) + [0..7 * 0x1] |
| IO_PC_PRT15_PC[0..5] | Port Pin Configuration Register | @0x40005078 + [0..5 * 0x1] |
| IO_PC_PRT15_7_6_PC[0..1] | Port Pin Configuration Register | @0x4000507e + [0..1 * 0x1] |
| PRT[0..14]_DR_ALIAS | Aliased Port Data Output Register | @0x40005080 + [0..14 * 0x1] |
| PRT15_DR_15_ALIAS | Aliased Port Data Output Register | 0x4000508f |
| PRT[0..14]_PS_ALIAS | Aliased Port Pin State Register | @0x40005090 + [0..14 * 0x1] |
| PRT15_PS15_ALIAS | Aliased Port Pin State Register | 0x4000509f |
| PRT[0..11]_DR | Port Data Output Register | @0x40005100 + [0..11 * 0x10] |
| PRT[0..11]_PS | Port Pin State Register1 | @0x40005100 + [0..11 * 0x10] + 0x1 |
| PRT[0..11]_DM[0..2] | Port Drive Mode Register | @(0x40005100 + [0..11 * 0x10]) + 0x2 + [0..2 * 0x1] |
| PRT[0..11]_SLW | Port slew rate control | @0x40005100 + [0..11 * 0x10] + 0x5 |
| PRT[0..11]_BYP | Port Bypass enable | @0x40005100 + [0..11 * 0x10] + 0x6 |
| PRT[0..11]_BIE | Port Bidirection enable | @0x40005100 + [0..11 * 0x10] + 0x7 |
| PRT[0..11]_INP_DIS | Input buffer disable override | @0x40005100 + [0..11 * 0x10] + 0x8 |

| Register Name | Purpose | Address |
|------------------------|--|------------------------------------|
| PRT[0..11]_CTL | Port wide control signals | @0x40005100 + [0..11 * 0x10] + 0x9 |
| PRT[0..11]_PRT | Port wide configuration register | @0x40005100 + [0..11 * 0x10] + 0xa |
| PRT[0..11]_BIT_MASK | Bit-mask for Aliased Register access | @0x40005100 + [0..11 * 0x10] + 0xb |
| PRT[0..11]_AMUX | Port Analog global mux bus enable | @0x40005100 + [0..11 * 0x10] + 0xc |
| PRT[0..11]_AG | Port Analog global enable | @0x40005100 + [0..11 * 0x10] + 0xd |
| PRT[0..11]_LCD_COM_SEG | Port LCD Com seg bits. | @0x40005100 + [0..11 * 0x10] + 0xe |
| PRT[0..11]_LCD_EN | Port LCD enable register. | @0x40005100 + [0..11 * 0x10] + 0xf |
| PRT12_DR | Port Data Output Register | 0x400051c0 |
| PRT12_PS | Port Pin State Register1 | 0x400051c1 |
| PRT12_DM[0..2] | Port Drive Mode Register | @0x400051c2 + [0..2 * 0x1] |
| PRT12_SLW | Port slew rate control | 0x400051c5 |
| PRT12_BYP | Port Bypass enable | 0x400051c6 |
| PRT12_BIE | Port Bidirection enable | 0x400051c7 |
| PRT12_INP_DIS | Input buffer disable override | 0x400051c8 |
| PRT12_SIO_HYST_EN | SIO Hysteresis enable | 0x400051c9 |
| PRT12_PRT | Port wide configuration register | 0x400051ca |
| PRT12_BIT_MASK | Bit-mask for Aliased Register access | 0x400051cb |
| PRT12_SIO_REG_HIFREQ | Regulated pull-up driver DC current setting | 0x400051cc |
| PRT12_AG | Port Analog global enable | 0x400051cd |
| PRT12_SIO_CFG | SIO Input Output Configuration | 0x400051ce |
| PRT12_SIO_DIFF | Differential Input Buffer reference voltage selection | 0x400051cf |
| PRT15_DR | Port Data Output Register | 0x400051f0 |
| PRT15_PS | Port Pin State Register1 | 0x400051f1 |
| PRT15_DM0 | Port Drive Mode Register | 0x400051f2 |
| PRT15_DM1 | Port Drive Mode Register | 0x400051f3 |
| PRT15_DM2 | Port Drive Mode Register | 0x400051f4 |
| PRT15_SLW | Port slew rate control | 0x400051f5 |
| PRT15_BYP | Port Bypass enable | 0x400051f6 |
| PRT15_BIE | Port Bidirection enable | 0x400051f7 |
| PRT15_INP_DIS | Input buffer disable override | 0x400051f8 |
| PRT15_CTL | Port wide control signals | 0x400051f9 |
| PRT15_PRT | Port wide configuration register | 0x400051fa |
| PRT15_BIT_MASK | Bit-mask for Aliased Register access | 0x400051fb |
| PRT15_AMUX | Port Analog global mux bus enable | 0x400051fc |
| PRT15_AG | Port Analog global enable | 0x400051fd |
| PRT15_LCD_COM_SEG | Port LCD Com seg bits. | 0x400051fe |
| PRT15_LCD_EN | Port LCD enable register. | 0x400051ff |
| PRT0_OUT_SEL0 | Digital System Interconnect Port Pin Output Select Registers. | 0x40005200 |
| PRT0_OUT_SEL1 | Digital System Interconnect Port Pin Output Select Registers. | 0x40005201 |
| PRT0_OE_SEL0 | Dynamic Drive Strength of Port Output Enable Select registers. | 0x40005202 |

| Register Name | Purpose | Address |
|------------------|---|------------|
| PRT0_OE_SEL1 | Dynamic Drive Stength of Port Output Enable Select registers. | 0x40005203 |
| PRT0_DBL_SYNC_IN | DSI double sync enable register. | 0x40005204 |
| PRT0_SYNC_OUT | DSI sync out enable register. | 0x40005205 |
| PRT0_CAPS_SEL | Global DSI select register. | 0x40005206 |
| PRT1_OUT_SELO | Digital System Interconnect Port Pin Output Select Registers. | 0x40005208 |
| PRT1_OUT_SEL1 | Digital System Interconnect Port Pin Output Select Registers. | 0x40005209 |
| PRT1_OE_SELO | Dynamic Drive Stength of Port Output Enable Select registers. | 0x4000520a |
| PRT1_OE_SEL1 | Dynamic Drive Stength of Port Output Enable Select registers. | 0x4000520b |
| PRT1_DBL_SYNC_IN | DSI double sync enable register. | 0x4000520c |
| PRT1_SYNC_OUT | DSI sync out enable register. | 0x4000520d |
| PRT1_CAPS_SEL | Global DSI select register. | 0x4000520e |
| PRT2_OUT_SELO | Digital System Interconnect Port Pin Output Select Registers. | 0x40005210 |
| PRT2_OUT_SEL1 | Digital System Interconnect Port Pin Output Select Registers. | 0x40005211 |
| PRT2_OE_SELO | Dynamic Drive Stength of Port Output Enable Select registers. | 0x40005212 |
| PRT2_OE_SEL1 | Dynamic Drive Stength of Port Output Enable Select registers. | 0x40005213 |
| PRT2_DBL_SYNC_IN | DSI double sync enable register. | 0x40005214 |
| PRT2_SYNC_OUT | DSI sync out enable register. | 0x40005215 |
| PRT2_CAPS_SEL | Global DSI select register. | 0x40005216 |
| PRT3_OUT_SELO | Digital System Interconnect Port Pin Output Select Registers. | 0x40005218 |
| PRT3_OUT_SEL1 | Digital System Interconnect Port Pin Output Select Registers. | 0x40005219 |
| PRT3_OE_SELO | Dynamic Drive Stength of Port Output Enable Select registers. | 0x4000521a |
| PRT3_OE_SEL1 | Dynamic Drive Stength of Port Output Enable Select registers. | 0x4000521b |
| PRT3_DBL_SYNC_IN | DSI double sync enable register. | 0x4000521c |
| PRT3_SYNC_OUT | DSI sync out enable register. | 0x4000521d |
| PRT3_CAPS_SEL | Global DSI select register. | 0x4000521e |
| PRT4_OUT_SELO | Digital System Interconnect Port Pin Output Select Registers. | 0x40005220 |
| PRT4_OUT_SEL1 | Digital System Interconnect Port Pin Output Select Registers. | 0x40005221 |
| PRT4_OE_SELO | Dynamic Drive Stength of Port Output Enable Select registers. | 0x40005222 |
| PRT4_OE_SEL1 | Dynamic Drive Stength of Port Output Enable Select registers. | 0x40005223 |
| PRT4_DBL_SYNC_IN | DSI double sync enable register. | 0x40005224 |
| PRT4_SYNC_OUT | DSI sync out enable register. | 0x40005225 |
| PRT4_CAPS_SEL | Global DSI select register. | 0x40005226 |
| PRT5_OUT_SELO | Digital System Interconnect Port Pin Output Select Registers. | 0x40005228 |

| Register Name | Purpose | Address |
|---------------------|--|------------|
| PRT5_OUT_SEL1 | Digital System Interconnect Port Pin Output Select Registers. | 0x40005229 |
| PRT5_OE_SELO | Dynamic Drive Strength of Port Output Enable Select registers. | 0x4000522a |
| PRT5_OE_SEL1 | Dynamic Drive Strength of Port Output Enable Select registers. | 0x4000522b |
| PRT5_DBL_SYNC_IN | DSI double sync enable register. | 0x4000522c |
| PRT5_SYNC_OUT | DSI sync out enable register. | 0x4000522d |
| PRT5_CAPS_SEL | Global DSI select register. | 0x4000522e |
| PRT6_OUT_SELO | Digital System Interconnect Port Pin Output Select Registers. | 0x40005230 |
| PRT6_OUT_SEL1 | Digital System Interconnect Port Pin Output Select Registers. | 0x40005231 |
| PRT6_OE_SELO | Dynamic Drive Strength of Port Output Enable Select registers. | 0x40005232 |
| PRT6_OE_SEL1 | Dynamic Drive Strength of Port Output Enable Select registers. | 0x40005233 |
| PRT6_DBL_SYNC_IN | DSI double sync enable register. | 0x40005234 |
| PRT6_SYNC_OUT | DSI sync out enable register. | 0x40005235 |
| PRT6_CAPS_SEL | Global DSI select register. | 0x40005236 |
| PRT12_OUT_SELO | Digital System Interconnect Port Pin Output Select Registers. | 0x40005260 |
| PRT12_OUT_SEL1 | Digital System Interconnect Port Pin Output Select Registers. | 0x40005261 |
| PRT12_OE_SELO | Dynamic Drive Strength of Port Output Enable Select registers. | 0x40005262 |
| PRT12_OE_SEL1 | Dynamic Drive Strength of Port Output Enable Select registers. | 0x40005263 |
| PRT12_DBL_SYNC_IN | DSI double sync enable register. | 0x40005264 |
| PRT12_SYNC_OUT | DSI sync out enable register. | 0x40005265 |
| PRT15_OUT_SELO | Digital System Interconnect Port Pin Output Select Registers. | 0x40005278 |
| PRT15_OUT_SEL1 | Digital System Interconnect Port Pin Output Select Registers. | 0x40005279 |
| PRT15_OE_SELO | Dynamic Drive Strength of Port Output Enable Select registers. | 0x4000527a |
| PRT15_OE_SEL1 | Dynamic Drive Strength of Port Output Enable Select registers. | 0x4000527b |
| PRT15_DBL_SYNC_IN | DSI double sync enable register. | 0x4000527c |
| PRT15_SYNC_OUT | DSI sync out enable register. | 0x4000527d |
| PRT15_CAPS_SEL | Global DSI select register. | 0x4000527e |
| EMIF_NO_UDB | EMIF UDB/NO_UDB Mode Register | 0x40005400 |
| EMIF_RP_WAIT_STATES | External Memory Interface Read Path Wait States Register | 0x40005401 |
| EMIF_MEM_DWN | External Memory Power Down Register | 0x40005402 |
| EMIF_MEMCLK_DIV | External Memory Clock Divider Register | 0x40005403 |
| EMIF_CLOCK_EN | EMIF Clock Enable Register | 0x40005404 |
| EMIF_EM_TYPE | External Memory Type Register | 0x40005405 |
| EMIF_WP_WAIT_STATES | External Memory Interface Write Path Wait States Register | 0x40005406 |

| Register Name | Purpose | Address |
|--------------------|--|----------------------------------|
| SC[0..3]_CR0 | Switched Capacitor Control Register 0 | @0x40005800 + [0..3 * 0x4] |
| SC[0..3]_CR1 | Switched Capacitor Control Register 1 | @0x40005800 + [0..3 * 0x4] + 0x1 |
| SC[0..3]_CR2 | Switched Capacitor Control Register 2 | @0x40005800 + [0..3 * 0x4] + 0x2 |
| DAC[0..3]_CR0 | DAC Block Control Register 0 | @0x40005820 + [0..3 * 0x4] |
| DAC[0..3]_CR1 | DAC Block Control Register 1 | @0x40005820 + [0..3 * 0x4] + 0x1 |
| DAC[0..3]_TST | DAC Block Test Register | @0x40005820 + [0..3 * 0x4] + 0x2 |
| CMP[0..3]_CR | Comparator Control Register | @0x40005840 + [0..3 * 0x1] |
| LUT[0..3]_CR | LUT Config Register | @0x40005848 + [0..3 * 0x2] |
| LUT[0..3]_MX | LUT Input Mux Config Register | @0x40005848 + [0..3 * 0x2] + 0x1 |
| OPAMP[0..3]_CR | Analog Output Buffer Configuration Register | @0x40005858 + [0..3 * 0x2] |
| OPAMP[0..3]_RSVD | OPAMP reserved | @0x40005858 + [0..3 * 0x2] + 0x1 |
| LCDDAC_CR0 | LCD Control Register 0 | 0x40005868 |
| LCDDAC_CR1 | LCDDAC Control Register 1 | 0x40005869 |
| LCDDRVR_CR | LCD Control Register | 0x4000586a |
| LCDTMR_CFG | LCD Timer Configuration Register | 0x4000586b |
| BG_CR0 | Bandgap Precision Reference Control 0 | 0x4000586c |
| BG_RSVD | Bandgap Precision Reference Reserved Register | 0x4000586d |
| BG_DFT0 | Bandgap Precision Reference DFT Register 0 | 0x4000586e |
| BG_DFT1 | Bandgap Precision Reference DFT Register 1 | 0x4000586f |
| CAPSL_CFG0 | Capsense Reference Driver Configuration Register | 0x40005870 |
| CAPSL_CFG1 | Capsense IO Configuration Register | 0x40005871 |
| CAPSR_CFG0 | Capsense Reference Driver Configuration Register | 0x40005872 |
| CAPSR_CFG1 | Capsense IO Configuration Register | 0x40005873 |
| PUMP_CR0 | Pump Configuration Register 0 | 0x40005876 |
| PUMP_CR1 | Pump Configuration Register 1 | 0x40005877 |
| LPF0_CR0 | Low Pass Filter Control Register | 0x40005878 |
| LPF0_RSVD | LPF Reserved | 0x40005879 |
| LPF1_CR0 | Low Pass Filter Control Register | 0x4000587a |
| LPF1_RSVD | LPF Reserved | 0x4000587b |
| ANAIF_CFG_MISC_CR0 | MISC Control Register 0 | 0x4000587c |
| DSM[0..0]_CR0 | Delta Sigma Modulator Control Register 0 | 0x40005880 |
| DSM[0..0]_CR1 | Delta Sigma Modulator Control Register 1 | 0x40005881 |
| DSM[0..0]_CR2 | Delta Sigma Modulator Control Register 2 | 0x40005882 |
| DSM[0..0]_CR3 | Delta Sigma Modulator Control Register 3 | 0x40005883 |
| DSM[0..0]_CR4 | Delta Sigma Modulator Control Register 4 | 0x40005884 |
| DSM[0..0]_CR5 | Delta Sigma Modulator Control Register 5 | 0x40005885 |
| DSM[0..0]_CR6 | Delta Sigma Modulator Control Register 6 | 0x40005886 |
| DSM[0..0]_CR7 | Delta Sigma Modulator Control Register 7 | 0x40005887 |
| DSM[0..0]_CR8 | Delta Sigma Modulator Control Register 8 | 0x40005888 |
| DSM[0..0]_CR9 | Delta Sigma Modulator Control Register 9 | 0x40005889 |
| DSM[0..0]_CR10 | Delta Sigma Modulator Control Register 10 | 0x4000588a |
| DSM[0..0]_CR11 | Delta Sigma Modulator Control Register 11 | 0x4000588b |

Register Mapping

| Register Name | Purpose | Address |
|-----------------|---|----------------------------------|
| DSM[0..0]_CR12 | Delta Sigma Modulator Control Register 12 | 0x4000588c |
| DSM[0..0]_CR13 | Delta Sigma Modulator Control Register 13 | 0x4000588d |
| DSM[0..0]_CR14 | Delta Sigma Modulator Control Register 14 | 0x4000588e |
| DSM[0..0]_CR15 | Delta Sigma Modulator Control Register 15 | 0x4000588f |
| DSM[0..0]_CR16 | Delta Sigma Modulator Control Register 0 | 0x40005890 |
| DSM[0..0]_CR17 | Delta Sigma Modulator Control Register | 0x40005891 |
| DSM[0..0]_REF0 | Delta Sigma Modulator Reference Register 0 | 0x40005892 |
| DSM[0..0]_REF1 | Delta Sigma Modulator Reference Register 1 | 0x40005893 |
| DSM[0..0]_REF2 | Delta Sigma Modulator Reference Register 2 | 0x40005894 |
| DSM[0..0]_REF3 | Delta Sigma Modulator Reference Register 1 | 0x40005895 |
| DSM[0..0]_DEMO | Delta Sigma Modulator Dynamic Element Matching Register 0 | 0x40005896 |
| DSM[0..0]_DEM1 | Delta Sigma Modulator Dynamic Element Matching Register 1 | 0x40005897 |
| DSM[0..0]_TST0 | Delta Sigma Modulator Test Register 0 | 0x40005898 |
| DSM[0..0]_TST1 | Delta Sigma Modulator Test Register 1 | 0x40005899 |
| DSM[0..0]_BUF0 | Delta Sigma Modulator Buffer Register 0 | 0x4000589a |
| DSM[0..0]_BUF1 | Delta Sigma Modulator Buffer Register 1 | 0x4000589b |
| DSM[0..0]_BUF2 | Delta Sigma Modulator Buffer Register 2 | 0x4000589c |
| DSM[0..0]_BUF3 | Delta Sigma Modulator Buffer Register 2 | 0x4000589d |
| DSM[0..0]_MISC | Delta Sigma Modulator Miscellaneous register | 0x4000589e |
| DSM[0..0]_RSVD1 | Delta Sigma Modulator RSVD 1 | 0x4000589f |
| SAR[0..1]_CSR0 | SAR status and control register 0 | @0x40005900 + [0..1 * 0x8] |
| SAR[0..1]_CSR1 | SAR status and control register 1 | @0x40005900 + [0..1 * 0x8] + 0x1 |
| SAR[0..1]_CSR2 | SAR status and control register 2 | @0x40005900 + [0..1 * 0x8] + 0x2 |
| SAR[0..1]_CSR3 | SAR status and control register 3 | @0x40005900 + [0..1 * 0x8] + 0x3 |
| SAR[0..1]_CSR4 | SAR status and control register 4 | @0x40005900 + [0..1 * 0x8] + 0x4 |
| SAR[0..1]_CSR5 | SAR status and control register 5 | @0x40005900 + [0..1 * 0x8] + 0x5 |
| SAR[0..1]_CSR6 | SAR status and control register 6 | @0x40005900 + [0..1 * 0x8] + 0x6 |
| SC0_SW0 | Switched Capacitor Analog Routing Register 0 | 0x40005a00 |
| SC0_SW2 | Switched Capacitor Analog Routing Register 2 | 0x40005a02 |
| SC0_SW3 | Switched Capacitor Analog Routing Register 3 | 0x40005a03 |
| SC0_SW4 | Switched Capacitor Analog Routing Register 4 | 0x40005a04 |
| SC0_SW6 | Switched Capacitor Analog Routing Register 6 | 0x40005a06 |
| SC0_SW7 | Switched Capacitor Analog Routing Register 7 | 0x40005a07 |
| SC0_SW8 | Switched Capacitor Analog Routing Register 8 | 0x40005a08 |
| SC0_SW10 | Switched Capacitor Analog Routing Register 10 | 0x40005a0a |
| SC0_CLK | Switched Capacitor Clock Selection Register | 0x40005a0b |
| SC0_BST | Switched Capacitor Boost Clock Selection Register | 0x40005a0c |
| SC1_SW0 | Switched Capacitor Analog Routing Register 0 | 0x40005a10 |
| SC1_SW2 | Switched Capacitor Analog Routing Register 2 | 0x40005a12 |
| SC1_SW3 | Switched Capacitor Analog Routing Register 3 | 0x40005a13 |
| SC1_SW4 | Switched Capacitor Analog Routing Register 4 | 0x40005a14 |

| Register Name | Purpose | Address |
|---------------|---|------------|
| SC1_SW6 | Switched Capacitor Analog Routing Register 6 | 0x40005a16 |
| SC1_SW7 | Switched Capacitor Analog Routing Register 7 | 0x40005a17 |
| SC1_SW8 | Switched Capacitor Analog Routing Register 8 | 0x40005a18 |
| SC1_SW10 | Switched Capacitor Analog Routing Register 10 | 0x40005a1a |
| SC1_CLK | Switched Capacitor Clock Selection Register | 0x40005a1b |
| SC1_BST | Switched Capacitor Boost Clock Selection Register | 0x40005a1c |
| SC2_SW0 | Switched Capacitor Analog Routing Register 0 | 0x40005a20 |
| SC2_SW2 | Switched Capacitor Analog Routing Register 2 | 0x40005a22 |
| SC2_SW3 | Switched Capacitor Analog Routing Register 3 | 0x40005a23 |
| SC2_SW4 | Switched Capacitor Analog Routing Register 4 | 0x40005a24 |
| SC2_SW6 | Switched Capacitor Analog Routing Register 6 | 0x40005a26 |
| SC2_SW7 | Switched Capacitor Analog Routing Register 7 | 0x40005a27 |
| SC2_SW8 | Switched Capacitor Analog Routing Register 8 | 0x40005a28 |
| SC2_SW10 | Switched Capacitor Analog Routing Register 10 | 0x40005a2a |
| SC2_CLK | Switched Capacitor Clock Selection Register | 0x40005a2b |
| SC2_BST | Switched Capacitor Boost Clock Selection Register | 0x40005a2c |
| SC3_SW0 | Switched Capacitor Analog Routing Register 0 | 0x40005a30 |
| SC3_SW2 | Switched Capacitor Analog Routing Register 2 | 0x40005a32 |
| SC3_SW3 | Switched Capacitor Analog Routing Register 3 | 0x40005a33 |
| SC3_SW4 | Switched Capacitor Analog Routing Register 4 | 0x40005a34 |
| SC3_SW6 | Switched Capacitor Analog Routing Register 6 | 0x40005a36 |
| SC3_SW7 | Switched Capacitor Analog Routing Register 7 | 0x40005a37 |
| SC3_SW8 | Switched Capacitor Analog Routing Register 8 | 0x40005a38 |
| SC3_SW10 | Switched Capacitor Analog Routing Register 10 | 0x40005a3a |
| SC3_CLK | Switched Capacitor Clock Selection Register | 0x40005a3b |
| SC3_BST | Switched Capacitor Boost Clock Selection Register | 0x40005a3c |
| DAC0_SW0 | DAC Analog Routing Register 0 | 0x40005a80 |
| DAC0_SW2 | DAC Analog Routing Register 2 | 0x40005a82 |
| DAC0_SW3 | DAC Analog Routing Register 3 | 0x40005a83 |
| DAC0_SW4 | DAC Analog Routing Register 4 | 0x40005a84 |
| DAC0_STROBE | DAC Strobe Register | 0x40005a87 |
| DAC1_SW0 | DAC Analog Routing Register 0 | 0x40005a88 |
| DAC1_SW2 | DAC Analog Routing Register 2 | 0x40005a8a |
| DAC1_SW3 | DAC Analog Routing Register 3 | 0x40005a8b |
| DAC1_SW4 | DAC Analog Routing Register 4 | 0x40005a8c |
| DAC1_STROBE | DAC Strobe Register | 0x40005a8f |
| DAC2_SW0 | DAC Analog Routing Register 0 | 0x40005a90 |
| DAC2_SW2 | DAC Analog Routing Register 2 | 0x40005a92 |
| DAC2_SW3 | DAC Analog Routing Register 3 | 0x40005a93 |
| DAC2_SW4 | DAC Analog Routing Register 4 | 0x40005a94 |
| DAC2_STROBE | DAC Strobe Register | 0x40005a97 |
| DAC3_SW0 | DAC Analog Routing Register 0 | 0x40005a98 |

| Register Name | Purpose | Address |
|---------------|---|------------|
| DAC3_SW2 | DAC Analog Routing Register 2 | 0x40005a9a |
| DAC3_SW3 | DAC Analog Routing Register 3 | 0x40005a9b |
| DAC3_SW4 | DAC Analog Routing Register 4 | 0x40005a9c |
| DAC3_STROBE | DAC Strobe Register | 0x40005a9f |
| CMP0_SW0 | Comparator Analog Routing Register 0 | 0x40005ac0 |
| CMP0_SW2 | Comparator Analog Routing Register 2 | 0x40005ac2 |
| CMP0_SW3 | Comparator Analog Routing Register 3 | 0x40005ac3 |
| CMP0_SW4 | Comparator Analog Routing Register 4 | 0x40005ac4 |
| CMP0_SW6 | Comparator Analog Routing Register 6 | 0x40005ac6 |
| CMP0_CLK | Comparator Clock Control Register | 0x40005ac7 |
| CMP1_SW0 | Comparator Analog Routing Register 0 | 0x40005ac8 |
| CMP1_SW2 | Comparator Analog Routing Register 2 | 0x40005aca |
| CMP1_SW3 | Comparator Analog Routing Register 3 | 0x40005acb |
| CMP1_SW4 | Comparator Analog Routing Register 4 | 0x40005acc |
| CMP1_SW6 | Comparator Analog Routing Register 6 | 0x40005ace |
| CMP1_CLK | Comparator Clock Control Register | 0x40005acf |
| CMP2_SW0 | Comparator Analog Routing Register 0 | 0x40005ad0 |
| CMP2_SW2 | Comparator Analog Routing Register 2 | 0x40005ad2 |
| CMP2_SW3 | Comparator Analog Routing Register 3 | 0x40005ad3 |
| CMP2_SW4 | Comparator Analog Routing Register 4 | 0x40005ad4 |
| CMP2_SW6 | Comparator Analog Routing Register 6 | 0x40005ad6 |
| CMP2_CLK | Comparator Clock Control Register | 0x40005ad7 |
| CMP3_SW0 | Comparator Analog Routing Register 0 | 0x40005ad8 |
| CMP3_SW2 | Comparator Analog Routing Register 2 | 0x40005ada |
| CMP3_SW3 | Comparator Analog Routing Register 3 | 0x40005adb |
| CMP3_SW4 | Comparator Analog Routing Register 4 | 0x40005adc |
| CMP3_SW6 | Comparator Analog Routing Register 6 | 0x40005ade |
| CMP3_CLK | Comparator Clock Control Register | 0x40005adf |
| DSM0_SW0 | Delta Sigma Modulator Analog Routing Register 0 | 0x40005b00 |
| DSM0_SW2 | Delta Sigma Modulator Analog Routing Register 2 | 0x40005b02 |
| DSM0_SW3 | Delta Sigma Modulator Analog Routing Register 3 | 0x40005b03 |
| DSM0_SW4 | Delta Sigma Modulator Analog Routing Register 4 | 0x40005b04 |
| DSM0_SW6 | Delta Sigma Modulator Analog Routing Register 6 | 0x40005b06 |
| DSM0_CLK | Delta Sigma Modulator Clock Selection Register | 0x40005b07 |
| SAR0_SW0 | SAR Analog Routing Register 0 | 0x40005b20 |
| SAR0_SW2 | SAR Analog Routing Register 2 | 0x40005b22 |
| SAR0_SW3 | SAR Analog Routing Register 3 | 0x40005b23 |
| SAR0_SW4 | SAR Analog Routing Register 4 | 0x40005b24 |
| SAR0_SW6 | SAR Analog Routing Register 6 | 0x40005b26 |
| SAR0_CLK | SAR Clock Selection Register | 0x40005b27 |
| SAR1_SW0 | SAR Analog Routing Register 0 | 0x40005b28 |
| SAR1_SW2 | SAR Analog Routing Register 2 | 0x40005b2a |

| Register Name | Purpose | Address |
|----------------|---|----------------------------|
| SAR1_SW3 | SAR Analog Routing Register 3 | 0x40005b2b |
| SAR1_SW4 | SAR Analog Routing Register 4 | 0x40005b2c |
| SAR1_SW6 | SAR Analog Routing Register 6 | 0x40005b2e |
| SAR1_CLK | SAR Clock Selection Register | 0x40005b2f |
| OPAMP0_MX | Analog Buffer Input Selection Register | 0x40005b40 |
| OPAMP0_SW | Analog Buffer Routing Switch Register | 0x40005b41 |
| OPAMP1_MX | Analog Buffer Input Selection Register | 0x40005b42 |
| OPAMP1_SW | Analog Buffer Routing Switch Register | 0x40005b43 |
| OPAMP2_MX | Analog Buffer Input Selection Register | 0x40005b44 |
| OPAMP2_SW | Analog Buffer Routing Switch Register | 0x40005b45 |
| OPAMP3_MX | Analog Buffer Input Selection Register | 0x40005b46 |
| OPAMP3_SW | Analog Buffer Routing Switch Register | 0x40005b47 |
| LCDDAC_SW0 | LCDDAC Switch Register 0 | 0x40005b50 |
| LCDDAC_SW1 | LCDDAC Switch Register 1 | 0x40005b51 |
| LCDDAC_SW2 | LCDDAC Switch Register 2 | 0x40005b52 |
| LCDDAC_SW3 | LCDDAC Switch Register 3 | 0x40005b53 |
| LCDDAC_SW4 | LCDDAC Switch Register 3 | 0x40005b54 |
| SC_MISC | Switched Cap Miscellaneous Control Register | 0x40005b56 |
| BUS_SW0 | Bus Switch Register 0 | 0x40005b58 |
| BUS_SW2 | Bus Switch Register 2 | 0x40005b5a |
| BUS_SW3 | Bus Switch Register 3 | 0x40005b5b |
| DFT_CR0 | DFT Control Register 0 | 0x40005b5c |
| DFT_CR1 | DFT Control Register 1 | 0x40005b5d |
| DFT_CR2 | DFT Control Register 2 | 0x40005b5e |
| DFT_CR3 | DFT Control Register 3 | 0x40005b5f |
| DFT_CR4 | DFT Control Register 4 | 0x40005b60 |
| DFT_CR5 | DFT Control Register 5 | 0x40005b61 |
| DAC[0..3]_D | DAC Data Register | @0x40005b80 + [0..3 * 0x1] |
| DSM[0..0]_OUT0 | DSM Output Register 0 | 0x40005b88 |
| DSM[0..0]_OUT1 | DSM Output Register 1 | 0x40005b89 |
| LUT_SR | LUT Status Register | 0x40005b90 |
| LUT_WRK1 | Reserved | 0x40005b91 |
| LUT_MSK | LUT Interrupt ReQuest (IRQ) Mask Register | 0x40005b92 |
| LUT_CLK | LUT CLK Register | 0x40005b93 |
| LUT_CPTR | LUT Capture Mode Register | 0x40005b94 |
| CMP_WRK | Comparator output working register | 0x40005b96 |
| CMP_TST | Comparator Test Register | 0x40005b97 |
| SC_SR | Switched Capacitor Status Register | 0x40005b98 |
| SC_WRK1 | Reserved | 0x40005b99 |
| SC_MSK | SC IRQ Mask Register | 0x40005b9a |
| SC_CMPINV | SC comparator inversion | 0x40005b9b |
| SC_CPTR | SC Capture Mode Register | 0x40005b9c |

| Register Name | Purpose | Address |
|--------------------|--|----------------------------------|
| SAR[0..1]_WRK0 | SAR working register 0 | @0x40005ba0 + [0..1 * 0x2] |
| SAR[0..1]_WRK1 | SAR register 1 | @0x40005ba0 + [0..1 * 0x2] + 0x1 |
| ANAIF_WRK_SARS_SOF | SAR Global Start-of-frame register | 0x40005ba8 |
| USB_EP0_DR[0..7] | Control End point EP0 Data Register | @0x40006000 + [0..7 * 0x1] |
| USB_CR0 | USB control 0 Register | 0x40006008 |
| USB_CR1 | USB control 1 Register | 0x40006009 |
| USB_SIE_EP_INT_EN | USB SIE Data Endpoints Interrupt Enable Register | 0x4000600a |
| USB_SIE_EP_INT_SR | SIE Data Endpoint Interrupt Status | 0x4000600b |
| USB_SIE_EP1_CNT0 | Non-control endpoint count register | 0x4000600c |
| USB_SIE_EP1_CNT1 | Non-control endpoint count register | 0x4000600d |
| USB_SIE_EP1_CR0 | | |
| USB_USBIO_CR0 | USBIO Control 0 Register | 0x40006010 |
| USB_USBIO_CR2 | USBIO control 2 Register | 0x40006011 |
| USB_USBIO_CR1 | USBIO control 1 Register | 0x40006012 |
| USB_DYN_RECONFIG | USB Dynamic reconfiguration register | 0x40006014 |
| USB_SOF0 | Start Of Frame Register | 0x40006018 |
| USB_SOF1 | Start Of Frame Register | 0x40006019 |
| USB_SIE_EP2_CNT0 | Non-control endpoint count register | 0x4000601c |
| USB_SIE_EP2_CNT1 | Non-control endpoint count register | 0x4000601d |
| USB_SIE_EP2_CR0 | | |
| USB_OSCLK_DR0 | Oscillator lock data register 0 | 0x40006020 |
| USB_OSCLK_DR1 | Oscillator lock data register 1 | 0x40006021 |
| USB_EP0_CR | Endpoint0 control Register | 0x40006028 |
| USB_EP0_CNT | Endpoint0 count Register | 0x40006029 |
| USB_SIE_EP3_CNT0 | Non-control endpoint count register | 0x4000602c |
| USB_SIE_EP3_CNT1 | Non-control endpoint count register | 0x4000602d |
| USB_SIE_EP3_CR0 | | |
| USB_SIE_EP4_CNT0 | Non-control endpoint count register | 0x4000603c |
| USB_SIE_EP4_CNT1 | Non-control endpoint count register | 0x4000603d |
| USB_SIE_EP4_CR0 | | |
| USB_SIE_EP5_CNT0 | Non-control endpoint count register | 0x4000604c |
| USB_SIE_EP5_CNT1 | Non-control endpoint count register | 0x4000604d |
| USB_SIE_EP5_CR0 | | |
| USB_SIE_EP6_CNT0 | Non-control endpoint count register | 0x4000605c |
| USB_SIE_EP6_CNT1 | Non-control endpoint count register | 0x4000605d |
| USB_SIE_EP6_CR0 | | |
| USB_SIE_EP7_CNT0 | Non-control endpoint count register | 0x4000606c |
| USB_SIE_EP7_CNT1 | Non-control endpoint count register | 0x4000606d |
| USB_SIE_EP7_CR0 | | |
| USB_SIE_EP8_CNT0 | Non-control endpoint count register | 0x4000607c |
| USB_SIE_EP8_CNT1 | Non-control endpoint count register | 0x4000607d |
| USB_SIE_EP8_CR0 | | |

| Register Name | Purpose | Address |
|--------------------|---|------------|
| USB_ARB_EP1_CFG | Endpoint Configuration Register | 0x40006080 |
| USB_ARB_EP1_INT_EN | Endpoint Interrupt Enable Register | 0x40006081 |
| USB_ARB_EP1_SR | Endpoint Status Register | 0x40006082 |
| USB_ARB_RW1_WA | Endpoint Write Address value | 0x40006084 |
| USB_ARB_RW1_WA_MSB | Endpoint Write Address value | 0x40006085 |
| USB_ARB_RW1_RA | Endpoint Read Address value | 0x40006086 |
| USB_ARB_RW1_RA_MSB | Endpoint Read Address value | 0x40006087 |
| USB_ARB_RW1_DR | Endpoint Data Register | 0x40006088 |
| USB_BUF_SIZE | Dedicated Endpoint Buffer Size Register | 0x4000608c |
| USB_EP_ACTIVE | Endpoint Active Indication Register | 0x4000608e |
| USB_EP_TYPE | Endpoint Type (IN/OUT) Indication | 0x4000608f |
| USB_ARB_EP2_CFG | Endpoint Configuration Register | 0x40006090 |
| USB_ARB_EP2_INT_EN | Endpoint Interrupt Enable Register | 0x40006091 |
| USB_ARB_EP2_SR | Endpoint Status Register | 0x40006092 |
| USB_ARB_RW2_WA | Endpoint Write Address value | 0x40006094 |
| USB_ARB_RW2_WA_MSB | Endpoint Write Address value | 0x40006095 |
| USB_ARB_RW2_RA | Endpoint Read Address value | 0x40006096 |
| USB_ARB_RW2_RA_MSB | Endpoint Read Address value | 0x40006097 |
| USB_ARB_RW2_DR | Endpoint Data Register | 0x40006098 |
| USB_ARB_CFG | Arbiter Configuration Register | 0x4000609c |
| USB_USB_CLK_EN | USB Block Clock Enable Register | 0x4000609d |
| USB_ARB_INT_EN | Arbiter Interrupt Enable | 0x4000609e |
| USB_ARB_INT_SR | Arbiter Interrupt Status | 0x4000609f |
| USB_ARB_EP3_CFG | Endpoint Configuration Register | 0x400060a0 |
| USB_ARB_EP3_INT_EN | Endpoint Interrupt Enable Register | 0x400060a1 |
| USB_ARB_EP3_SR | Endpoint Status Register | 0x400060a2 |
| USB_ARB_RW3_WA | Endpoint Write Address value | 0x400060a4 |
| USB_ARB_RW3_WA_MSB | Endpoint Write Address value | 0x400060a5 |
| USB_ARB_RW3_RA | Endpoint Read Address value | 0x400060a6 |
| USB_ARB_RW3_RA_MSB | Endpoint Read Address value | 0x400060a7 |
| USB_ARB_RW3_DR | Endpoint Data Register | 0x400060a8 |
| USB_CWA | Common Area Write Address | 0x400060ac |
| USB_CWA_MSB | Common Area Write Address | 0x400060ad |
| USB_ARB_EP4_CFG | Endpoint Configuration Register | 0x400060b0 |
| USB_ARB_EP4_INT_EN | Endpoint Interrupt Enable Register | 0x400060b1 |
| USB_ARB_EP4_SR | Endpoint Status Register | 0x400060b2 |
| USB_ARB_RW4_WA | Endpoint Write Address value | 0x400060b4 |
| USB_ARB_RW4_WA_MSB | Endpoint Write Address value | 0x400060b5 |
| USB_ARB_RW4_RA | Endpoint Read Address value | 0x400060b6 |
| USB_ARB_RW4_RA_MSB | Endpoint Read Address value | 0x400060b7 |
| USB_ARB_RW4_DR | Endpoint Data Register | 0x400060b8 |
| USB_DMA_THRES | DMA Burst / Threshold Configuration | 0x400060bc |

Register Mapping

| Register Name | Purpose | Address |
|----------------------|-------------------------------------|------------------------------------|
| USB_DMA_THRES_MSB | DMA Burst / Threshold Configuration | 0x400060bd |
| USB_ARB_EP5_CFG | Endpoint Configuration Register | 0x400060c0 |
| USB_ARB_EP5_INT_EN | Endpoint Interrupt Enable Register | 0x400060c1 |
| USB_ARB_EP5_SR | Endpoint Status Register | 0x400060c2 |
| USB_ARB_RW5_WA | Endpoint Write Address value | 0x400060c4 |
| USB_ARB_RW5_WA_MSB | Endpoint Write Address value | 0x400060c5 |
| USB_ARB_RW5_RA | Endpoint Read Address value | 0x400060c6 |
| USB_ARB_RW5_RA_MSB | Endpoint Read Address value | 0x400060c7 |
| USB_ARB_RW5_DR | Endpoint Data Register | 0x400060c8 |
| USB_BUS_RST_CNT | Bus Reset Count Register | 0x400060cc |
| USB_ARB_EP6_CFG | Endpoint Configuration Register | 0x400060d0 |
| USB_ARB_EP6_INT_EN | Endpoint Interrupt Enable Register | 0x400060d1 |
| USB_ARB_EP6_SR | Endpoint Status Register | 0x400060d2 |
| USB_ARB_RW6_WA | Endpoint Write Address value | 0x400060d4 |
| USB_ARB_RW6_WA_MSB | Endpoint Write Address value | 0x400060d5 |
| USB_ARB_RW6_RA | Endpoint Read Address value | 0x400060d6 |
| USB_ARB_RW6_RA_MSB | Endpoint Read Address value | 0x400060d7 |
| USB_ARB_RW6_DR | Endpoint Data Register | 0x400060d8 |
| USB_ARB_EP7_CFG | Endpoint Configuration Register | 0x400060e0 |
| USB_ARB_EP7_INT_EN | Endpoint Interrupt Enable Register | 0x400060e1 |
| USB_ARB_EP7_SR | Endpoint Status Register | 0x400060e2 |
| USB_ARB_RW7_WA | Endpoint Write Address value | 0x400060e4 |
| USB_ARB_RW7_WA_MSB | Endpoint Write Address value | 0x400060e5 |
| USB_ARB_RW7_RA | Endpoint Read Address value | 0x400060e6 |
| USB_ARB_RW7_RA_MSB | Endpoint Read Address value | 0x400060e7 |
| USB_ARB_RW7_DR | Endpoint Data Register | 0x400060e8 |
| USB_ARB_EP8_CFG | Endpoint Configuration Register | 0x400060f0 |
| USB_ARB_EP8_INT_EN | Endpoint Interrupt Enable Register | 0x400060f1 |
| USB_ARB_EP8_SR | Endpoint Status Register | 0x400060f2 |
| USB_ARB_RW8_WA | Endpoint Write Address value | 0x400060f4 |
| USB_ARB_RW8_WA_MSB | Endpoint Write Address value | 0x400060f5 |
| USB_ARB_RW8_RA | Endpoint Read Address value | 0x400060f6 |
| USB_ARB_RW8_RA_MSB | Endpoint Read Address value | 0x400060f7 |
| USB_ARB_RW8_DR | Endpoint Data Register | 0x400060f8 |
| USB_MEM_DATA[0..511] | DATA | @0x40006100 + [0..511 * 0x1] |
| B[0..3]_UDB00_A0 | UDB00_A0 | @0x40006400 + [0..3 * 0x100] |
| B[0..3]_UDB01_A0 | UDB01_A0 | @0x40006400 + [0..3 * 0x100] + 0x1 |
| B[0..3]_UDB02_A0 | UDB02_A0 | @0x40006400 + [0..3 * 0x100] + 0x2 |
| B[0..3]_UDB03_A0 | UDB03_A0 | @0x40006400 + [0..3 * 0x100] + 0x3 |
| B[0..3]_UDB04_A0 | UDB04_A0 | @0x40006400 + [0..3 * 0x100] + 0x4 |
| B[0..3]_UDB05_A0 | UDB05_A0 | @0x40006400 + [0..3 * 0x100] + 0x5 |
| B[0..3]_UDB06_A0 | UDB06_A0 | @0x40006400 + [0..3 * 0x100] + 0x6 |

| Register Name | Purpose | Address |
|------------------|----------|-------------------------------------|
| B[0..3]_UDB07_A0 | UDB07_A0 | @0x40006400 + [0..3 * 0x100] + 0x7 |
| B[0..3]_UDB08_A0 | UDB08_A0 | @0x40006400 + [0..3 * 0x100] + 0x8 |
| B[0..3]_UDB09_A0 | UDB09_A0 | @0x40006400 + [0..3 * 0x100] + 0x9 |
| B[0..3]_UDB10_A0 | UDB10_A0 | @0x40006400 + [0..3 * 0x100] + 0xa |
| B[0..3]_UDB11_A0 | UDB11_A0 | @0x40006400 + [0..3 * 0x100] + 0xb |
| B[0..3]_UDB12_A0 | UDB12_A0 | @0x40006400 + [0..3 * 0x100] + 0xc |
| B[0..3]_UDB13_A0 | UDB13_A0 | @0x40006400 + [0..3 * 0x100] + 0xd |
| B[0..3]_UDB14_A0 | UDB14_A0 | @0x40006400 + [0..3 * 0x100] + 0xe |
| B[0..3]_UDB15_A0 | UDB15_A0 | @0x40006400 + [0..3 * 0x100] + 0xf |
| B[0..3]_UDB00_A1 | UDB00_A1 | @0x40006400 + [0..3 * 0x100] + 0x10 |
| B[0..3]_UDB01_A1 | UDB01_A1 | @0x40006400 + [0..3 * 0x100] + 0x11 |
| B[0..3]_UDB02_A1 | UDB02_A1 | @0x40006400 + [0..3 * 0x100] + 0x12 |
| B[0..3]_UDB03_A1 | UDB03_A1 | @0x40006400 + [0..3 * 0x100] + 0x13 |
| B[0..3]_UDB04_A1 | UDB04_A1 | @0x40006400 + [0..3 * 0x100] + 0x14 |
| B[0..3]_UDB05_A1 | UDB05_A1 | @0x40006400 + [0..3 * 0x100] + 0x15 |
| B[0..3]_UDB06_A1 | UDB06_A1 | @0x40006400 + [0..3 * 0x100] + 0x16 |
| B[0..3]_UDB07_A1 | UDB07_A1 | @0x40006400 + [0..3 * 0x100] + 0x17 |
| B[0..3]_UDB08_A1 | UDB08_A1 | @0x40006400 + [0..3 * 0x100] + 0x18 |
| B[0..3]_UDB09_A1 | UDB09_A1 | @0x40006400 + [0..3 * 0x100] + 0x19 |
| B[0..3]_UDB10_A1 | UDB10_A1 | @0x40006400 + [0..3 * 0x100] + 0x1a |
| B[0..3]_UDB11_A1 | UDB11_A1 | @0x40006400 + [0..3 * 0x100] + 0x1b |
| B[0..3]_UDB12_A1 | UDB12_A1 | @0x40006400 + [0..3 * 0x100] + 0x1c |
| B[0..3]_UDB13_A1 | UDB13_A1 | @0x40006400 + [0..3 * 0x100] + 0x1d |
| B[0..3]_UDB14_A1 | UDB14_A1 | @0x40006400 + [0..3 * 0x100] + 0x1e |
| B[0..3]_UDB15_A1 | UDB15_A1 | @0x40006400 + [0..3 * 0x100] + 0x1f |
| B[0..3]_UDB00_D0 | UDB00_D0 | @0x40006400 + [0..3 * 0x100] + 0x20 |
| B[0..3]_UDB01_D0 | UDB01_D0 | @0x40006400 + [0..3 * 0x100] + 0x21 |
| B[0..3]_UDB02_D0 | UDB02_D0 | @0x40006400 + [0..3 * 0x100] + 0x22 |
| B[0..3]_UDB03_D0 | UDB03_D0 | @0x40006400 + [0..3 * 0x100] + 0x23 |
| B[0..3]_UDB04_D0 | UDB04_D0 | @0x40006400 + [0..3 * 0x100] + 0x24 |
| B[0..3]_UDB05_D0 | UDB05_D0 | @0x40006400 + [0..3 * 0x100] + 0x25 |
| B[0..3]_UDB06_D0 | UDB06_D0 | @0x40006400 + [0..3 * 0x100] + 0x26 |
| B[0..3]_UDB07_D0 | UDB07_D0 | @0x40006400 + [0..3 * 0x100] + 0x27 |
| B[0..3]_UDB08_D0 | UDB08_D0 | @0x40006400 + [0..3 * 0x100] + 0x28 |
| B[0..3]_UDB09_D0 | UDB09_D0 | @0x40006400 + [0..3 * 0x100] + 0x29 |
| B[0..3]_UDB10_D0 | UDB10_D0 | @0x40006400 + [0..3 * 0x100] + 0x2a |
| B[0..3]_UDB11_D0 | UDB11_D0 | @0x40006400 + [0..3 * 0x100] + 0x2b |
| B[0..3]_UDB12_D0 | UDB12_D0 | @0x40006400 + [0..3 * 0x100] + 0x2c |
| B[0..3]_UDB13_D0 | UDB13_D0 | @0x40006400 + [0..3 * 0x100] + 0x2d |
| B[0..3]_UDB14_D0 | UDB14_D0 | @0x40006400 + [0..3 * 0x100] + 0x2e |
| B[0..3]_UDB15_D0 | UDB15_D0 | @0x40006400 + [0..3 * 0x100] + 0x2f |
| B[0..3]_UDB00_D1 | UDB00_D1 | @0x40006400 + [0..3 * 0x100] + 0x30 |

Register Mapping

| Register Name | Purpose | Address |
|------------------|----------|-------------------------------------|
| B[0..3]_UDB01_D1 | UDB01_D1 | @0x40006400 + [0..3 * 0x100] + 0x31 |
| B[0..3]_UDB02_D1 | UDB02_D1 | @0x40006400 + [0..3 * 0x100] + 0x32 |
| B[0..3]_UDB03_D1 | UDB03_D1 | @0x40006400 + [0..3 * 0x100] + 0x33 |
| B[0..3]_UDB04_D1 | UDB04_D1 | @0x40006400 + [0..3 * 0x100] + 0x34 |
| B[0..3]_UDB05_D1 | UDB05_D1 | @0x40006400 + [0..3 * 0x100] + 0x35 |
| B[0..3]_UDB06_D1 | UDB06_D1 | @0x40006400 + [0..3 * 0x100] + 0x36 |
| B[0..3]_UDB07_D1 | UDB07_D1 | @0x40006400 + [0..3 * 0x100] + 0x37 |
| B[0..3]_UDB08_D1 | UDB08_D1 | @0x40006400 + [0..3 * 0x100] + 0x38 |
| B[0..3]_UDB09_D1 | UDB09_D1 | @0x40006400 + [0..3 * 0x100] + 0x39 |
| B[0..3]_UDB10_D1 | UDB10_D1 | @0x40006400 + [0..3 * 0x100] + 0x3a |
| B[0..3]_UDB11_D1 | UDB11_D1 | @0x40006400 + [0..3 * 0x100] + 0x3b |
| B[0..3]_UDB12_D1 | UDB12_D1 | @0x40006400 + [0..3 * 0x100] + 0x3c |
| B[0..3]_UDB13_D1 | UDB13_D1 | @0x40006400 + [0..3 * 0x100] + 0x3d |
| B[0..3]_UDB14_D1 | UDB14_D1 | @0x40006400 + [0..3 * 0x100] + 0x3e |
| B[0..3]_UDB15_D1 | UDB15_D1 | @0x40006400 + [0..3 * 0x100] + 0x3f |
| B[0..3]_UDB00_F0 | UDB00_F0 | @0x40006400 + [0..3 * 0x100] + 0x40 |
| B[0..3]_UDB01_F0 | UDB01_F0 | @0x40006400 + [0..3 * 0x100] + 0x41 |
| B[0..3]_UDB02_F0 | UDB02_F0 | @0x40006400 + [0..3 * 0x100] + 0x42 |
| B[0..3]_UDB03_F0 | UDB03_F0 | @0x40006400 + [0..3 * 0x100] + 0x43 |
| B[0..3]_UDB04_F0 | UDB04_F0 | @0x40006400 + [0..3 * 0x100] + 0x44 |
| B[0..3]_UDB05_F0 | UDB05_F0 | @0x40006400 + [0..3 * 0x100] + 0x45 |
| B[0..3]_UDB06_F0 | UDB06_F0 | @0x40006400 + [0..3 * 0x100] + 0x46 |
| B[0..3]_UDB07_F0 | UDB07_F0 | @0x40006400 + [0..3 * 0x100] + 0x47 |
| B[0..3]_UDB08_F0 | UDB08_F0 | @0x40006400 + [0..3 * 0x100] + 0x48 |
| B[0..3]_UDB09_F0 | UDB09_F0 | @0x40006400 + [0..3 * 0x100] + 0x49 |
| B[0..3]_UDB10_F0 | UDB10_F0 | @0x40006400 + [0..3 * 0x100] + 0x4a |
| B[0..3]_UDB11_F0 | UDB11_F0 | @0x40006400 + [0..3 * 0x100] + 0x4b |
| B[0..3]_UDB12_F0 | UDB12_F0 | @0x40006400 + [0..3 * 0x100] + 0x4c |
| B[0..3]_UDB13_F0 | UDB13_F0 | @0x40006400 + [0..3 * 0x100] + 0x4d |
| B[0..3]_UDB14_F0 | UDB14_F0 | @0x40006400 + [0..3 * 0x100] + 0x4e |
| B[0..3]_UDB15_F0 | UDB15_F0 | @0x40006400 + [0..3 * 0x100] + 0x4f |
| B[0..3]_UDB00_F1 | UDB00_F1 | @0x40006400 + [0..3 * 0x100] + 0x50 |
| B[0..3]_UDB01_F1 | UDB01_F1 | @0x40006400 + [0..3 * 0x100] + 0x51 |
| B[0..3]_UDB02_F1 | UDB02_F1 | @0x40006400 + [0..3 * 0x100] + 0x52 |
| B[0..3]_UDB03_F1 | UDB03_F1 | @0x40006400 + [0..3 * 0x100] + 0x53 |
| B[0..3]_UDB04_F1 | UDB04_F1 | @0x40006400 + [0..3 * 0x100] + 0x54 |
| B[0..3]_UDB05_F1 | UDB05_F1 | @0x40006400 + [0..3 * 0x100] + 0x55 |
| B[0..3]_UDB06_F1 | UDB06_F1 | @0x40006400 + [0..3 * 0x100] + 0x56 |
| B[0..3]_UDB07_F1 | UDB07_F1 | @0x40006400 + [0..3 * 0x100] + 0x57 |
| B[0..3]_UDB08_F1 | UDB08_F1 | @0x40006400 + [0..3 * 0x100] + 0x58 |
| B[0..3]_UDB09_F1 | UDB09_F1 | @0x40006400 + [0..3 * 0x100] + 0x59 |
| B[0..3]_UDB10_F1 | UDB10_F1 | @0x40006400 + [0..3 * 0x100] + 0x5a |

| Register Name | Purpose | Address |
|-------------------|-----------|-------------------------------------|
| B[0..3]_UDB11_F1 | UDB11_F1 | @0x40006400 + [0..3 * 0x100] + 0x5b |
| B[0..3]_UDB12_F1 | UDB12_F1 | @0x40006400 + [0..3 * 0x100] + 0x5c |
| B[0..3]_UDB13_F1 | UDB13_F1 | @0x40006400 + [0..3 * 0x100] + 0x5d |
| B[0..3]_UDB14_F1 | UDB14_F1 | @0x40006400 + [0..3 * 0x100] + 0x5e |
| B[0..3]_UDB15_F1 | UDB15_F1 | @0x40006400 + [0..3 * 0x100] + 0x5f |
| B[0..3]_UDB00_ST | UDB00_ST | @0x40006400 + [0..3 * 0x100] + 0x60 |
| B[0..3]_UDB01_ST | UDB01_ST | @0x40006400 + [0..3 * 0x100] + 0x61 |
| B[0..3]_UDB02_ST | UDB02_ST | @0x40006400 + [0..3 * 0x100] + 0x62 |
| B[0..3]_UDB03_ST | UDB03_ST | @0x40006400 + [0..3 * 0x100] + 0x63 |
| B[0..3]_UDB04_ST | UDB04_ST | @0x40006400 + [0..3 * 0x100] + 0x64 |
| B[0..3]_UDB05_ST | UDB05_ST | @0x40006400 + [0..3 * 0x100] + 0x65 |
| B[0..3]_UDB06_ST | UDB06_ST | @0x40006400 + [0..3 * 0x100] + 0x66 |
| B[0..3]_UDB07_ST | UDB07_ST | @0x40006400 + [0..3 * 0x100] + 0x67 |
| B[0..3]_UDB08_ST | UDB08_ST | @0x40006400 + [0..3 * 0x100] + 0x68 |
| B[0..3]_UDB09_ST | UDB09_ST | @0x40006400 + [0..3 * 0x100] + 0x69 |
| B[0..3]_UDB10_ST | UDB10_ST | @0x40006400 + [0..3 * 0x100] + 0x6a |
| B[0..3]_UDB11_ST | UDB11_ST | @0x40006400 + [0..3 * 0x100] + 0x6b |
| B[0..3]_UDB12_ST | UDB12_ST | @0x40006400 + [0..3 * 0x100] + 0x6c |
| B[0..3]_UDB13_ST | UDB13_ST | @0x40006400 + [0..3 * 0x100] + 0x6d |
| B[0..3]_UDB14_ST | UDB14_ST | @0x40006400 + [0..3 * 0x100] + 0x6e |
| B[0..3]_UDB15_ST | UDB15_ST | @0x40006400 + [0..3 * 0x100] + 0x6f |
| B[0..3]_UDB00_CTL | UDB00_CTL | @0x40006400 + [0..3 * 0x100] + 0x70 |
| B[0..3]_UDB01_CTL | UDB01_CTL | @0x40006400 + [0..3 * 0x100] + 0x71 |
| B[0..3]_UDB02_CTL | UDB02_CTL | @0x40006400 + [0..3 * 0x100] + 0x72 |
| B[0..3]_UDB03_CTL | UDB03_CTL | @0x40006400 + [0..3 * 0x100] + 0x73 |
| B[0..3]_UDB04_CTL | UDB04_CTL | @0x40006400 + [0..3 * 0x100] + 0x74 |
| B[0..3]_UDB05_CTL | UDB05_CTL | @0x40006400 + [0..3 * 0x100] + 0x75 |
| B[0..3]_UDB06_CTL | UDB06_CTL | @0x40006400 + [0..3 * 0x100] + 0x76 |
| B[0..3]_UDB07_CTL | UDB07_CTL | @0x40006400 + [0..3 * 0x100] + 0x77 |
| B[0..3]_UDB08_CTL | UDB08_CTL | @0x40006400 + [0..3 * 0x100] + 0x78 |
| B[0..3]_UDB09_CTL | UDB09_CTL | @0x40006400 + [0..3 * 0x100] + 0x79 |
| B[0..3]_UDB10_CTL | UDB10_CTL | @0x40006400 + [0..3 * 0x100] + 0x7a |
| B[0..3]_UDB11_CTL | UDB11_CTL | @0x40006400 + [0..3 * 0x100] + 0x7b |
| B[0..3]_UDB12_CTL | UDB12_CTL | @0x40006400 + [0..3 * 0x100] + 0x7c |
| B[0..3]_UDB13_CTL | UDB13_CTL | @0x40006400 + [0..3 * 0x100] + 0x7d |
| B[0..3]_UDB14_CTL | UDB14_CTL | @0x40006400 + [0..3 * 0x100] + 0x7e |
| B[0..3]_UDB15_CTL | UDB15_CTL | @0x40006400 + [0..3 * 0x100] + 0x7f |
| B[0..3]_UDB00_MSK | UDB00_MSK | @0x40006400 + [0..3 * 0x100] + 0x80 |
| B[0..3]_UDB01_MSK | UDB01_MSK | @0x40006400 + [0..3 * 0x100] + 0x81 |
| B[0..3]_UDB02_MSK | UDB02_MSK | @0x40006400 + [0..3 * 0x100] + 0x82 |
| B[0..3]_UDB03_MSK | UDB03_MSK | @0x40006400 + [0..3 * 0x100] + 0x83 |
| B[0..3]_UDB04_MSK | UDB04_MSK | @0x40006400 + [0..3 * 0x100] + 0x84 |

Register Mapping

| Register Name | Purpose | Address |
|--------------------|------------|-------------------------------------|
| B[0..3]_UDB05_MSK | UDB05_MSK | @0x40006400 + [0..3 * 0x100] + 0x85 |
| B[0..3]_UDB06_MSK | UDB06_MSK | @0x40006400 + [0..3 * 0x100] + 0x86 |
| B[0..3]_UDB07_MSK | UDB07_MSK | @0x40006400 + [0..3 * 0x100] + 0x87 |
| B[0..3]_UDB08_MSK | UDB08_MSK | @0x40006400 + [0..3 * 0x100] + 0x88 |
| B[0..3]_UDB09_MSK | UDB09_MSK | @0x40006400 + [0..3 * 0x100] + 0x89 |
| B[0..3]_UDB10_MSK | UDB10_MSK | @0x40006400 + [0..3 * 0x100] + 0x8a |
| B[0..3]_UDB11_MSK | UDB11_MSK | @0x40006400 + [0..3 * 0x100] + 0x8b |
| B[0..3]_UDB12_MSK | UDB12_MSK | @0x40006400 + [0..3 * 0x100] + 0x8c |
| B[0..3]_UDB13_MSK | UDB13_MSK | @0x40006400 + [0..3 * 0x100] + 0x8d |
| B[0..3]_UDB14_MSK | UDB14_MSK | @0x40006400 + [0..3 * 0x100] + 0x8e |
| B[0..3]_UDB15_MSK | UDB15_MSK | @0x40006400 + [0..3 * 0x100] + 0x8f |
| B[0..3]_UDB00_ACTL | UDB00_ACTL | @0x40006400 + [0..3 * 0x100] + 0x90 |
| B[0..3]_UDB01_ACTL | UDB01_ACTL | @0x40006400 + [0..3 * 0x100] + 0x91 |
| B[0..3]_UDB02_ACTL | UDB02_ACTL | @0x40006400 + [0..3 * 0x100] + 0x92 |
| B[0..3]_UDB03_ACTL | UDB03_ACTL | @0x40006400 + [0..3 * 0x100] + 0x93 |
| B[0..3]_UDB04_ACTL | UDB04_ACTL | @0x40006400 + [0..3 * 0x100] + 0x94 |
| B[0..3]_UDB05_ACTL | UDB05_ACTL | @0x40006400 + [0..3 * 0x100] + 0x95 |
| B[0..3]_UDB06_ACTL | UDB06_ACTL | @0x40006400 + [0..3 * 0x100] + 0x96 |
| B[0..3]_UDB07_ACTL | UDB07_ACTL | @0x40006400 + [0..3 * 0x100] + 0x97 |
| B[0..3]_UDB08_ACTL | UDB08_ACTL | @0x40006400 + [0..3 * 0x100] + 0x98 |
| B[0..3]_UDB09_ACTL | UDB09_ACTL | @0x40006400 + [0..3 * 0x100] + 0x99 |
| B[0..3]_UDB10_ACTL | UDB10_ACTL | @0x40006400 + [0..3 * 0x100] + 0x9a |
| B[0..3]_UDB11_ACTL | UDB11_ACTL | @0x40006400 + [0..3 * 0x100] + 0x9b |
| B[0..3]_UDB12_ACTL | UDB12_ACTL | @0x40006400 + [0..3 * 0x100] + 0x9c |
| B[0..3]_UDB13_ACTL | UDB13_ACTL | @0x40006400 + [0..3 * 0x100] + 0x9d |
| B[0..3]_UDB14_ACTL | UDB14_ACTL | @0x40006400 + [0..3 * 0x100] + 0x9e |
| B[0..3]_UDB15_ACTL | UDB15_ACTL | @0x40006400 + [0..3 * 0x100] + 0x9f |
| B[0..3]_UDB00_MC | UDB00_MC | @0x40006400 + [0..3 * 0x100] + 0xa0 |
| B[0..3]_UDB01_MC | UDB01_MC | @0x40006400 + [0..3 * 0x100] + 0xa1 |
| B[0..3]_UDB02_MC | UDB02_MC | @0x40006400 + [0..3 * 0x100] + 0xa2 |
| B[0..3]_UDB03_MC | UDB03_MC | @0x40006400 + [0..3 * 0x100] + 0xa3 |
| B[0..3]_UDB04_MC | UDB04_MC | @0x40006400 + [0..3 * 0x100] + 0xa4 |
| B[0..3]_UDB05_MC | UDB05_MC | @0x40006400 + [0..3 * 0x100] + 0xa5 |
| B[0..3]_UDB06_MC | UDB06_MC | @0x40006400 + [0..3 * 0x100] + 0xa6 |
| B[0..3]_UDB07_MC | UDB07_MC | @0x40006400 + [0..3 * 0x100] + 0xa7 |
| B[0..3]_UDB08_MC | UDB08_MC | @0x40006400 + [0..3 * 0x100] + 0xa8 |
| B[0..3]_UDB09_MC | UDB09_MC | @0x40006400 + [0..3 * 0x100] + 0xa9 |
| B[0..3]_UDB10_MC | UDB10_MC | @0x40006400 + [0..3 * 0x100] + 0xaa |
| B[0..3]_UDB11_MC | UDB11_MC | @0x40006400 + [0..3 * 0x100] + 0xab |
| B[0..3]_UDB12_MC | UDB12_MC | @0x40006400 + [0..3 * 0x100] + 0xac |
| B[0..3]_UDB13_MC | UDB13_MC | @0x40006400 + [0..3 * 0x100] + 0xad |
| B[0..3]_UDB14_MC | UDB14_MC | @0x40006400 + [0..3 * 0x100] + 0xae |

| Register Name | Purpose | Address |
|---------------------|-------------|-------------------------------------|
| B[0..3]_UDB15_MC | UDB15_MC | @0x40006400 + [0..3 * 0x100] + 0xaf |
| B[0..3]_UDB00_01_A0 | UDB00_01_A0 | @0x40006800 + [0..3 * 0x200] |
| B[0..3]_UDB01_02_A0 | UDB01_02_A0 | @0x40006800 + [0..3 * 0x200] + 0x2 |
| B[0..3]_UDB02_03_A0 | UDB02_03_A0 | @0x40006800 + [0..3 * 0x200] + 0x4 |
| B[0..3]_UDB03_04_A0 | UDB03_04_A0 | @0x40006800 + [0..3 * 0x200] + 0x6 |
| B[0..3]_UDB04_05_A0 | UDB04_05_A0 | @0x40006800 + [0..3 * 0x200] + 0x8 |
| B[0..3]_UDB05_06_A0 | UDB05_06_A0 | @0x40006800 + [0..3 * 0x200] + 0xa |
| B[0..3]_UDB06_07_A0 | UDB06_07_A0 | @0x40006800 + [0..3 * 0x200] + 0xc |
| B[0..3]_UDB07_08_A0 | UDB07_08_A0 | @0x40006800 + [0..3 * 0x200] + 0xe |
| B[0..3]_UDB08_09_A0 | UDB08_09_A0 | @0x40006800 + [0..3 * 0x200] + 0x10 |
| B[0..3]_UDB09_10_A0 | UDB09_10_A0 | @0x40006800 + [0..3 * 0x200] + 0x12 |
| B[0..3]_UDB10_11_A0 | UDB10_11_A0 | @0x40006800 + [0..3 * 0x200] + 0x14 |
| B[0..3]_UDB11_12_A0 | UDB11_12_A0 | @0x40006800 + [0..3 * 0x200] + 0x16 |
| B[0..3]_UDB12_13_A0 | UDB12_13_A0 | @0x40006800 + [0..3 * 0x200] + 0x18 |
| B[0..3]_UDB13_14_A0 | UDB13_14_A0 | @0x40006800 + [0..3 * 0x200] + 0x1a |
| B[0..3]_UDB14_15_A0 | UDB14_15_A0 | @0x40006800 + [0..3 * 0x200] + 0x1c |
| B[0..3]_UDB00_01_A1 | UDB00_01_A1 | @0x40006800 + [0..3 * 0x200] + 0x20 |
| B[0..3]_UDB01_02_A1 | UDB01_02_A1 | @0x40006800 + [0..3 * 0x200] + 0x22 |
| B[0..3]_UDB02_03_A1 | UDB02_03_A1 | @0x40006800 + [0..3 * 0x200] + 0x24 |
| B[0..3]_UDB03_04_A1 | UDB03_04_A1 | @0x40006800 + [0..3 * 0x200] + 0x26 |
| B[0..3]_UDB04_05_A1 | UDB04_05_A1 | @0x40006800 + [0..3 * 0x200] + 0x28 |
| B[0..3]_UDB05_06_A1 | UDB05_06_A1 | @0x40006800 + [0..3 * 0x200] + 0x2a |
| B[0..3]_UDB06_07_A1 | UDB06_07_A1 | @0x40006800 + [0..3 * 0x200] + 0x2c |
| B[0..3]_UDB07_08_A1 | UDB07_08_A1 | @0x40006800 + [0..3 * 0x200] + 0x2e |
| B[0..3]_UDB08_09_A1 | UDB08_09_A1 | @0x40006800 + [0..3 * 0x200] + 0x30 |
| B[0..3]_UDB09_10_A1 | UDB09_10_A1 | @0x40006800 + [0..3 * 0x200] + 0x32 |
| B[0..3]_UDB10_11_A1 | UDB10_11_A1 | @0x40006800 + [0..3 * 0x200] + 0x34 |
| B[0..3]_UDB11_12_A1 | UDB11_12_A1 | @0x40006800 + [0..3 * 0x200] + 0x36 |
| B[0..3]_UDB12_13_A1 | UDB12_13_A1 | @0x40006800 + [0..3 * 0x200] + 0x38 |
| B[0..3]_UDB13_14_A1 | UDB13_14_A1 | @0x40006800 + [0..3 * 0x200] + 0x3a |
| B[0..3]_UDB14_15_A1 | UDB14_15_A1 | @0x40006800 + [0..3 * 0x200] + 0x3c |
| B[0..3]_UDB00_01_D0 | UDB00_01_D0 | @0x40006800 + [0..3 * 0x200] + 0x40 |
| B[0..3]_UDB01_02_D0 | UDB01_02_D0 | @0x40006800 + [0..3 * 0x200] + 0x42 |
| B[0..3]_UDB02_03_D0 | UDB02_03_D0 | @0x40006800 + [0..3 * 0x200] + 0x44 |
| B[0..3]_UDB03_04_D0 | UDB03_04_D0 | @0x40006800 + [0..3 * 0x200] + 0x46 |
| B[0..3]_UDB04_05_D0 | UDB04_05_D0 | @0x40006800 + [0..3 * 0x200] + 0x48 |
| B[0..3]_UDB05_06_D0 | UDB05_06_D0 | @0x40006800 + [0..3 * 0x200] + 0x4a |
| B[0..3]_UDB06_07_D0 | UDB06_07_D0 | @0x40006800 + [0..3 * 0x200] + 0x4c |
| B[0..3]_UDB07_08_D0 | UDB07_08_D0 | @0x40006800 + [0..3 * 0x200] + 0x4e |
| B[0..3]_UDB08_09_D0 | UDB08_09_D0 | @0x40006800 + [0..3 * 0x200] + 0x50 |
| B[0..3]_UDB09_10_D0 | UDB09_10_D0 | @0x40006800 + [0..3 * 0x200] + 0x52 |
| B[0..3]_UDB10_11_D0 | UDB10_11_D0 | @0x40006800 + [0..3 * 0x200] + 0x54 |

Register Mapping

| Register Name | Purpose | Address |
|---------------------|-------------|-------------------------------------|
| B[0..3]_UDB11_12_D0 | UDB11_12_D0 | @0x40006800 + [0..3 * 0x200] + 0x56 |
| B[0..3]_UDB12_13_D0 | UDB12_13_D0 | @0x40006800 + [0..3 * 0x200] + 0x58 |
| B[0..3]_UDB13_14_D0 | UDB13_14_D0 | @0x40006800 + [0..3 * 0x200] + 0x5a |
| B[0..3]_UDB14_15_D0 | UDB14_15_D0 | @0x40006800 + [0..3 * 0x200] + 0x5c |
| B[0..3]_UDB00_01_D1 | UDB00_01_D1 | @0x40006800 + [0..3 * 0x200] + 0x60 |
| B[0..3]_UDB01_02_D1 | UDB01_02_D1 | @0x40006800 + [0..3 * 0x200] + 0x62 |
| B[0..3]_UDB02_03_D1 | UDB02_03_D1 | @0x40006800 + [0..3 * 0x200] + 0x64 |
| B[0..3]_UDB03_04_D1 | UDB03_04_D1 | @0x40006800 + [0..3 * 0x200] + 0x66 |
| B[0..3]_UDB04_05_D1 | UDB04_05_D1 | @0x40006800 + [0..3 * 0x200] + 0x68 |
| B[0..3]_UDB05_06_D1 | UDB05_06_D1 | @0x40006800 + [0..3 * 0x200] + 0x6a |
| B[0..3]_UDB06_07_D1 | UDB06_07_D1 | @0x40006800 + [0..3 * 0x200] + 0x6c |
| B[0..3]_UDB07_08_D1 | UDB07_08_D1 | @0x40006800 + [0..3 * 0x200] + 0x6e |
| B[0..3]_UDB08_09_D1 | UDB08_09_D1 | @0x40006800 + [0..3 * 0x200] + 0x70 |
| B[0..3]_UDB09_10_D1 | UDB09_10_D1 | @0x40006800 + [0..3 * 0x200] + 0x72 |
| B[0..3]_UDB10_11_D1 | UDB10_11_D1 | @0x40006800 + [0..3 * 0x200] + 0x74 |
| B[0..3]_UDB11_12_D1 | UDB11_12_D1 | @0x40006800 + [0..3 * 0x200] + 0x76 |
| B[0..3]_UDB12_13_D1 | UDB12_13_D1 | @0x40006800 + [0..3 * 0x200] + 0x78 |
| B[0..3]_UDB13_14_D1 | UDB13_14_D1 | @0x40006800 + [0..3 * 0x200] + 0x7a |
| B[0..3]_UDB14_15_D1 | UDB14_15_D1 | @0x40006800 + [0..3 * 0x200] + 0x7c |
| B[0..3]_UDB00_01_F0 | UDB00_01_F0 | @0x40006800 + [0..3 * 0x200] + 0x80 |
| B[0..3]_UDB01_02_F0 | UDB01_02_F0 | @0x40006800 + [0..3 * 0x200] + 0x82 |
| B[0..3]_UDB02_03_F0 | UDB02_03_F0 | @0x40006800 + [0..3 * 0x200] + 0x84 |
| B[0..3]_UDB03_04_F0 | UDB03_04_F0 | @0x40006800 + [0..3 * 0x200] + 0x86 |
| B[0..3]_UDB04_05_F0 | UDB04_05_F0 | @0x40006800 + [0..3 * 0x200] + 0x88 |
| B[0..3]_UDB05_06_F0 | UDB05_06_F0 | @0x40006800 + [0..3 * 0x200] + 0x8a |
| B[0..3]_UDB06_07_F0 | UDB06_07_F0 | @0x40006800 + [0..3 * 0x200] + 0x8c |
| B[0..3]_UDB07_08_F0 | UDB07_08_F0 | @0x40006800 + [0..3 * 0x200] + 0x8e |
| B[0..3]_UDB08_09_F0 | UDB08_09_F0 | @0x40006800 + [0..3 * 0x200] + 0x90 |
| B[0..3]_UDB09_10_F0 | UDB09_10_F0 | @0x40006800 + [0..3 * 0x200] + 0x92 |
| B[0..3]_UDB10_11_F0 | UDB10_11_F0 | @0x40006800 + [0..3 * 0x200] + 0x94 |
| B[0..3]_UDB11_12_F0 | UDB11_12_F0 | @0x40006800 + [0..3 * 0x200] + 0x96 |
| B[0..3]_UDB12_13_F0 | UDB12_13_F0 | @0x40006800 + [0..3 * 0x200] + 0x98 |
| B[0..3]_UDB13_14_F0 | UDB13_14_F0 | @0x40006800 + [0..3 * 0x200] + 0x9a |
| B[0..3]_UDB14_15_F0 | UDB14_15_F0 | @0x40006800 + [0..3 * 0x200] + 0x9c |
| B[0..3]_UDB00_01_F1 | UDB00_01_F1 | @0x40006800 + [0..3 * 0x200] + 0xa0 |
| B[0..3]_UDB01_02_F1 | UDB01_02_F1 | @0x40006800 + [0..3 * 0x200] + 0xa2 |
| B[0..3]_UDB02_03_F1 | UDB02_03_F1 | @0x40006800 + [0..3 * 0x200] + 0xa4 |
| B[0..3]_UDB03_04_F1 | UDB03_04_F1 | @0x40006800 + [0..3 * 0x200] + 0xa6 |
| B[0..3]_UDB04_05_F1 | UDB04_05_F1 | @0x40006800 + [0..3 * 0x200] + 0xa8 |
| B[0..3]_UDB05_06_F1 | UDB05_06_F1 | @0x40006800 + [0..3 * 0x200] + 0xaa |
| B[0..3]_UDB06_07_F1 | UDB06_07_F1 | @0x40006800 + [0..3 * 0x200] + 0xac |
| B[0..3]_UDB07_08_F1 | UDB07_08_F1 | @0x40006800 + [0..3 * 0x200] + 0xae |

| Register Name | Purpose | Address |
|----------------------|--------------|--------------------------------------|
| B[0..3]_UDB08_09_F1 | UDB08_09_F1 | @0x40006800 + [0..3 * 0x200] + 0xb0 |
| B[0..3]_UDB09_10_F1 | UDB09_10_F1 | @0x40006800 + [0..3 * 0x200] + 0xb2 |
| B[0..3]_UDB10_11_F1 | UDB10_11_F1 | @0x40006800 + [0..3 * 0x200] + 0xb4 |
| B[0..3]_UDB11_12_F1 | UDB11_12_F1 | @0x40006800 + [0..3 * 0x200] + 0xb6 |
| B[0..3]_UDB12_13_F1 | UDB12_13_F1 | @0x40006800 + [0..3 * 0x200] + 0xb8 |
| B[0..3]_UDB13_14_F1 | UDB13_14_F1 | @0x40006800 + [0..3 * 0x200] + 0xba |
| B[0..3]_UDB14_15_F1 | UDB14_15_F1 | @0x40006800 + [0..3 * 0x200] + 0xbc |
| B[0..3]_UDB00_01_ST | UDB00_01_ST | @0x40006800 + [0..3 * 0x200] + 0xc0 |
| B[0..3]_UDB01_02_ST | UDB01_02_ST | @0x40006800 + [0..3 * 0x200] + 0xc2 |
| B[0..3]_UDB02_03_ST | UDB02_03_ST | @0x40006800 + [0..3 * 0x200] + 0xc4 |
| B[0..3]_UDB03_04_ST | UDB03_04_ST | @0x40006800 + [0..3 * 0x200] + 0xc6 |
| B[0..3]_UDB04_05_ST | UDB04_05_ST | @0x40006800 + [0..3 * 0x200] + 0xc8 |
| B[0..3]_UDB05_06_ST | UDB05_06_ST | @0x40006800 + [0..3 * 0x200] + 0xca |
| B[0..3]_UDB06_07_ST | UDB06_07_ST | @0x40006800 + [0..3 * 0x200] + 0xcc |
| B[0..3]_UDB07_08_ST | UDB07_08_ST | @0x40006800 + [0..3 * 0x200] + 0xce |
| B[0..3]_UDB08_09_ST | UDB08_09_ST | @0x40006800 + [0..3 * 0x200] + 0xd0 |
| B[0..3]_UDB09_10_ST | UDB09_10_ST | @0x40006800 + [0..3 * 0x200] + 0xd2 |
| B[0..3]_UDB10_11_ST | UDB10_11_ST | @0x40006800 + [0..3 * 0x200] + 0xd4 |
| B[0..3]_UDB11_12_ST | UDB11_12_ST | @0x40006800 + [0..3 * 0x200] + 0xd6 |
| B[0..3]_UDB12_13_ST | UDB12_13_ST | @0x40006800 + [0..3 * 0x200] + 0xd8 |
| B[0..3]_UDB13_14_ST | UDB13_14_ST | @0x40006800 + [0..3 * 0x200] + 0xda |
| B[0..3]_UDB14_15_ST | UDB14_15_ST | @0x40006800 + [0..3 * 0x200] + 0xdc |
| B[0..3]_UDB00_01_CTL | UDB00_01_CTL | @0x40006800 + [0..3 * 0x200] + 0xe0 |
| B[0..3]_UDB01_02_CTL | UDB01_02_CTL | @0x40006800 + [0..3 * 0x200] + 0xe2 |
| B[0..3]_UDB02_03_CTL | UDB02_03_CTL | @0x40006800 + [0..3 * 0x200] + 0xe4 |
| B[0..3]_UDB03_04_CTL | UDB03_04_CTL | @0x40006800 + [0..3 * 0x200] + 0xe6 |
| B[0..3]_UDB04_05_CTL | UDB04_05_CTL | @0x40006800 + [0..3 * 0x200] + 0xe8 |
| B[0..3]_UDB05_06_CTL | UDB05_06_CTL | @0x40006800 + [0..3 * 0x200] + 0xea |
| B[0..3]_UDB06_07_CTL | UDB06_07_CTL | @0x40006800 + [0..3 * 0x200] + 0xec |
| B[0..3]_UDB07_08_CTL | UDB07_08_CTL | @0x40006800 + [0..3 * 0x200] + 0xee |
| B[0..3]_UDB08_09_CTL | UDB08_09_CTL | @0x40006800 + [0..3 * 0x200] + 0xf0 |
| B[0..3]_UDB09_10_CTL | UDB09_10_CTL | @0x40006800 + [0..3 * 0x200] + 0xf2 |
| B[0..3]_UDB10_11_CTL | UDB10_11_CTL | @0x40006800 + [0..3 * 0x200] + 0xf4 |
| B[0..3]_UDB11_12_CTL | UDB11_12_CTL | @0x40006800 + [0..3 * 0x200] + 0xf6 |
| B[0..3]_UDB12_13_CTL | UDB12_13_CTL | @0x40006800 + [0..3 * 0x200] + 0xf8 |
| B[0..3]_UDB13_14_CTL | UDB13_14_CTL | @0x40006800 + [0..3 * 0x200] + 0xfa |
| B[0..3]_UDB14_15_CTL | UDB14_15_CTL | @0x40006800 + [0..3 * 0x200] + 0xfc |
| B[0..3]_UDB00_01_MSK | UDB00_01_MSK | @0x40006800 + [0..3 * 0x200] + 0x100 |
| B[0..3]_UDB01_02_MSK | UDB01_02_MSK | @0x40006800 + [0..3 * 0x200] + 0x102 |
| B[0..3]_UDB02_03_MSK | UDB02_03_MSK | @0x40006800 + [0..3 * 0x200] + 0x104 |
| B[0..3]_UDB03_04_MSK | UDB03_04_MSK | @0x40006800 + [0..3 * 0x200] + 0x106 |
| B[0..3]_UDB04_05_MSK | UDB04_05_MSK | @0x40006800 + [0..3 * 0x200] + 0x108 |

Register Mapping

| Register Name | Purpose | Address |
|-----------------------|---------------|--------------------------------------|
| B[0..3]_UDB05_06_MSK | UDB05_06_MSK | @0x40006800 + [0..3 * 0x200] + 0x10a |
| B[0..3]_UDB06_07_MSK | UDB06_07_MSK | @0x40006800 + [0..3 * 0x200] + 0x10c |
| B[0..3]_UDB07_08_MSK | UDB07_08_MSK | @0x40006800 + [0..3 * 0x200] + 0x10e |
| B[0..3]_UDB08_09_MSK | UDB08_09_MSK | @0x40006800 + [0..3 * 0x200] + 0x110 |
| B[0..3]_UDB09_10_MSK | UDB09_10_MSK | @0x40006800 + [0..3 * 0x200] + 0x112 |
| B[0..3]_UDB10_11_MSK | UDB10_11_MSK | @0x40006800 + [0..3 * 0x200] + 0x114 |
| B[0..3]_UDB11_12_MSK | UDB11_12_MSK | @0x40006800 + [0..3 * 0x200] + 0x116 |
| B[0..3]_UDB12_13_MSK | UDB12_13_MSK | @0x40006800 + [0..3 * 0x200] + 0x118 |
| B[0..3]_UDB13_14_MSK | UDB13_14_MSK | @0x40006800 + [0..3 * 0x200] + 0x11a |
| B[0..3]_UDB14_15_MSK | UDB14_15_MSK | @0x40006800 + [0..3 * 0x200] + 0x11c |
| B[0..3]_UDB00_01_ACTL | UDB00_01_ACTL | @0x40006800 + [0..3 * 0x200] + 0x120 |
| B[0..3]_UDB01_02_ACTL | UDB01_02_ACTL | @0x40006800 + [0..3 * 0x200] + 0x122 |
| B[0..3]_UDB02_03_ACTL | UDB02_03_ACTL | @0x40006800 + [0..3 * 0x200] + 0x124 |
| B[0..3]_UDB03_04_ACTL | UDB03_04_ACTL | @0x40006800 + [0..3 * 0x200] + 0x126 |
| B[0..3]_UDB04_05_ACTL | UDB04_05_ACTL | @0x40006800 + [0..3 * 0x200] + 0x128 |
| B[0..3]_UDB05_06_ACTL | UDB05_06_ACTL | @0x40006800 + [0..3 * 0x200] + 0x12a |
| B[0..3]_UDB06_07_ACTL | UDB06_07_ACTL | @0x40006800 + [0..3 * 0x200] + 0x12c |
| B[0..3]_UDB07_08_ACTL | UDB07_08_ACTL | @0x40006800 + [0..3 * 0x200] + 0x12e |
| B[0..3]_UDB08_09_ACTL | UDB08_09_ACTL | @0x40006800 + [0..3 * 0x200] + 0x130 |
| B[0..3]_UDB09_10_ACTL | UDB09_10_ACTL | @0x40006800 + [0..3 * 0x200] + 0x132 |
| B[0..3]_UDB10_11_ACTL | UDB10_11_ACTL | @0x40006800 + [0..3 * 0x200] + 0x134 |
| B[0..3]_UDB11_12_ACTL | UDB11_12_ACTL | @0x40006800 + [0..3 * 0x200] + 0x136 |
| B[0..3]_UDB12_13_ACTL | UDB12_13_ACTL | @0x40006800 + [0..3 * 0x200] + 0x138 |
| B[0..3]_UDB13_14_ACTL | UDB13_14_ACTL | @0x40006800 + [0..3 * 0x200] + 0x13a |
| B[0..3]_UDB14_15_ACTL | UDB14_15_ACTL | @0x40006800 + [0..3 * 0x200] + 0x13c |
| B[0..3]_UDB00_01_MC | UDB00_01_MC | @0x40006800 + [0..3 * 0x200] + 0x140 |
| B[0..3]_UDB01_02_MC | UDB01_02_MC | @0x40006800 + [0..3 * 0x200] + 0x142 |
| B[0..3]_UDB02_03_MC | UDB02_03_MC | @0x40006800 + [0..3 * 0x200] + 0x144 |
| B[0..3]_UDB03_04_MC | UDB03_04_MC | @0x40006800 + [0..3 * 0x200] + 0x146 |
| B[0..3]_UDB04_05_MC | UDB04_05_MC | @0x40006800 + [0..3 * 0x200] + 0x148 |
| B[0..3]_UDB05_06_MC | UDB05_06_MC | @0x40006800 + [0..3 * 0x200] + 0x14a |
| B[0..3]_UDB06_07_MC | UDB06_07_MC | @0x40006800 + [0..3 * 0x200] + 0x14c |
| B[0..3]_UDB07_08_MC | UDB07_08_MC | @0x40006800 + [0..3 * 0x200] + 0x14e |
| B[0..3]_UDB08_09_MC | UDB08_09_MC | @0x40006800 + [0..3 * 0x200] + 0x150 |
| B[0..3]_UDB09_10_MC | UDB09_10_MC | @0x40006800 + [0..3 * 0x200] + 0x152 |
| B[0..3]_UDB10_11_MC | UDB10_11_MC | @0x40006800 + [0..3 * 0x200] + 0x154 |
| B[0..3]_UDB11_12_MC | UDB11_12_MC | @0x40006800 + [0..3 * 0x200] + 0x156 |
| B[0..3]_UDB12_13_MC | UDB12_13_MC | @0x40006800 + [0..3 * 0x200] + 0x158 |
| B[0..3]_UDB13_14_MC | UDB13_14_MC | @0x40006800 + [0..3 * 0x200] + 0x15a |
| B[0..3]_UDB14_15_MC | UDB14_15_MC | @0x40006800 + [0..3 * 0x200] + 0x15c |
| B[0..3]_UDB00_A0_A1 | UDB00_A0_A1 | @0x40006800 + [0..3 * 0x200] |
| B[0..3]_UDB01_A0_A1 | UDB01_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x2 |

| Register Name | Purpose | Address |
|---------------------|-------------|-------------------------------------|
| B[0..3]_UDB02_A0_A1 | UDB02_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x4 |
| B[0..3]_UDB03_A0_A1 | UDB03_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x6 |
| B[0..3]_UDB04_A0_A1 | UDB04_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x8 |
| B[0..3]_UDB05_A0_A1 | UDB05_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0xa |
| B[0..3]_UDB06_A0_A1 | UDB06_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0xc |
| B[0..3]_UDB07_A0_A1 | UDB07_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0xe |
| B[0..3]_UDB08_A0_A1 | UDB08_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x10 |
| B[0..3]_UDB09_A0_A1 | UDB09_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x12 |
| B[0..3]_UDB10_A0_A1 | UDB10_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x14 |
| B[0..3]_UDB11_A0_A1 | UDB11_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x16 |
| B[0..3]_UDB12_A0_A1 | UDB12_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x18 |
| B[0..3]_UDB13_A0_A1 | UDB13_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x1a |
| B[0..3]_UDB14_A0_A1 | UDB14_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x1c |
| B[0..3]_UDB15_A0_A1 | UDB15_A0_A1 | @0x40006800 + [0..3 * 0x200] + 0x1e |
| B[0..3]_UDB00_D0_D1 | UDB00_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x40 |
| B[0..3]_UDB01_D0_D1 | UDB01_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x42 |
| B[0..3]_UDB02_D0_D1 | UDB02_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x44 |
| B[0..3]_UDB03_D0_D1 | UDB03_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x46 |
| B[0..3]_UDB04_D0_D1 | UDB04_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x48 |
| B[0..3]_UDB05_D0_D1 | UDB05_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x4a |
| B[0..3]_UDB06_D0_D1 | UDB06_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x4c |
| B[0..3]_UDB07_D0_D1 | UDB07_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x4e |
| B[0..3]_UDB08_D0_D1 | UDB08_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x50 |
| B[0..3]_UDB09_D0_D1 | UDB09_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x52 |
| B[0..3]_UDB10_D0_D1 | UDB10_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x54 |
| B[0..3]_UDB11_D0_D1 | UDB11_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x56 |
| B[0..3]_UDB12_D0_D1 | UDB12_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x58 |
| B[0..3]_UDB13_D0_D1 | UDB13_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x5a |
| B[0..3]_UDB14_D0_D1 | UDB14_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x5c |
| B[0..3]_UDB15_D0_D1 | UDB15_D0_D1 | @0x40006800 + [0..3 * 0x200] + 0x5e |
| B[0..3]_UDB00_F0_F1 | UDB00_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x80 |
| B[0..3]_UDB01_F0_F1 | UDB01_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x82 |
| B[0..3]_UDB02_F0_F1 | UDB02_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x84 |
| B[0..3]_UDB03_F0_F1 | UDB03_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x86 |
| B[0..3]_UDB04_F0_F1 | UDB04_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x88 |
| B[0..3]_UDB05_F0_F1 | UDB05_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x8a |
| B[0..3]_UDB06_F0_F1 | UDB06_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x8c |
| B[0..3]_UDB07_F0_F1 | UDB07_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x8e |
| B[0..3]_UDB08_F0_F1 | UDB08_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x90 |
| B[0..3]_UDB09_F0_F1 | UDB09_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x92 |
| B[0..3]_UDB10_F0_F1 | UDB10_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x94 |
| B[0..3]_UDB11_F0_F1 | UDB11_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x96 |

Register Mapping

| Register Name | Purpose | Address |
|------------------------|----------------|--------------------------------------|
| B[0..3]_UDB12_F0_F1 | UDB12_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x98 |
| B[0..3]_UDB13_F0_F1 | UDB13_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x9a |
| B[0..3]_UDB14_F0_F1 | UDB14_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x9c |
| B[0..3]_UDB15_F0_F1 | UDB15_F0_F1 | @0x40006800 + [0..3 * 0x200] + 0x9e |
| B[0..3]_UDB00_ST_CTL | UDB00_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xc0 |
| B[0..3]_UDB01_ST_CTL | UDB01_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xc2 |
| B[0..3]_UDB02_ST_CTL | UDB02_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xc4 |
| B[0..3]_UDB03_ST_CTL | UDB03_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xc6 |
| B[0..3]_UDB04_ST_CTL | UDB04_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xc8 |
| B[0..3]_UDB05_ST_CTL | UDB05_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xca |
| B[0..3]_UDB06_ST_CTL | UDB06_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xcc |
| B[0..3]_UDB07_ST_CTL | UDB07_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xce |
| B[0..3]_UDB08_ST_CTL | UDB08_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xd0 |
| B[0..3]_UDB09_ST_CTL | UDB09_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xd2 |
| B[0..3]_UDB10_ST_CTL | UDB10_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xd4 |
| B[0..3]_UDB11_ST_CTL | UDB11_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xd6 |
| B[0..3]_UDB12_ST_CTL | UDB12_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xd8 |
| B[0..3]_UDB13_ST_CTL | UDB13_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xda |
| B[0..3]_UDB14_ST_CTL | UDB14_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xdc |
| B[0..3]_UDB15_ST_CTL | UDB15_ST_CTL | @0x40006800 + [0..3 * 0x200] + 0xde |
| B[0..3]_UDB00_MSK_ACTL | UDB00_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x100 |
| B[0..3]_UDB01_MSK_ACTL | UDB01_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x102 |
| B[0..3]_UDB02_MSK_ACTL | UDB02_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x104 |
| B[0..3]_UDB03_MSK_ACTL | UDB03_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x106 |
| B[0..3]_UDB04_MSK_ACTL | UDB04_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x108 |
| B[0..3]_UDB05_MSK_ACTL | UDB05_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x10a |
| B[0..3]_UDB06_MSK_ACTL | UDB06_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x10c |
| B[0..3]_UDB07_MSK_ACTL | UDB07_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x10e |
| B[0..3]_UDB08_MSK_ACTL | UDB08_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x110 |
| B[0..3]_UDB09_MSK_ACTL | UDB09_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x112 |
| B[0..3]_UDB10_MSK_ACTL | UDB10_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x114 |
| B[0..3]_UDB11_MSK_ACTL | UDB11_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x116 |
| B[0..3]_UDB12_MSK_ACTL | UDB12_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x118 |
| B[0..3]_UDB13_MSK_ACTL | UDB13_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x11a |
| B[0..3]_UDB14_MSK_ACTL | UDB14_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x11c |
| B[0..3]_UDB15_MSK_ACTL | UDB15_MSK_ACTL | @0x40006800 + [0..3 * 0x200] + 0x11e |
| B[0..3]_UDB00_MC_00 | UDB00_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x140 |
| B[0..3]_UDB01_MC_00 | UDB01_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x142 |
| B[0..3]_UDB02_MC_00 | UDB02_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x144 |
| B[0..3]_UDB03_MC_00 | UDB03_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x146 |
| B[0..3]_UDB04_MC_00 | UDB04_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x148 |
| B[0..3]_UDB05_MC_00 | UDB05_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x14a |

| Register Name | Purpose | Address |
|---------------------------------|--|--------------------------------------|
| B[0..3]_UDB06_MC_00 | UDB06_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x14c |
| B[0..3]_UDB07_MC_00 | UDB07_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x14e |
| B[0..3]_UDB08_MC_00 | UDB08_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x150 |
| B[0..3]_UDB09_MC_00 | UDB09_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x152 |
| B[0..3]_UDB10_MC_00 | UDB10_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x154 |
| B[0..3]_UDB11_MC_00 | UDB11_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x156 |
| B[0..3]_UDB12_MC_00 | UDB12_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x158 |
| B[0..3]_UDB13_MC_00 | UDB13_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x15a |
| B[0..3]_UDB14_MC_00 | UDB14_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x15c |
| B[0..3]_UDB15_MC_00 | UDB15_MC_00 | @0x40006800 + [0..3 * 0x200] + 0x15e |
| PHUB_CFG | PHUB Configuration | 0x40007000 |
| PHUB_ERR | PHUB Error Detection | 0x40007004 |
| PHUB_ERR_ADR | PHUB Error Address | 0x40007008 |
| PHUB_CH[0..23]_BASIC_CFG | Channel Basic Configuration Register | @0x40007010 + [0..23 * 0x10] |
| PHUB_CH[0..23]_ACTION | Channel Action | @0x40007010 + [0..23 * 0x10] + 0x4 |
| PHUB_CH[0..23]_BASIC_STATUS | Channel Basic Status Register | @0x40007010 + [0..23 * 0x10] + 0x8 |
| PHUB_CFGMEM[0..23]_CFG0 | PHUB Channel Configuration Register 0 | @0x40007600 + [0..23 * 0x8] |
| PHUB_CFGMEM[0..23]_CFG1 | PHUB Channel Configuration Register 1 | @0x40007600 + [0..23 * 0x8] + 0x4 |
| PHUB_TDMEM[0..127]_ORIG_TD0 | PHUB Original Transaction Descriptor 0 | @0x40007800 + [0..127 * 0x8] |
| PHUB_TDMEM[0..127]_ORIG_TD1 | PHUB Original Transaction Descriptor 0 | @0x40007800 + [0..127 * 0x8] + 0x4 |
| EE_DATA[0..2047] | EEPROM Memory | @0x40008000 + [0..2047 * 0x1] |
| CAN[0..0]_CSR_INT_SR | INT_SR | 0x4000a000 |
| CAN[0..0]_CSR_INT_EN | INT_EN | 0x4000a004 |
| CAN[0..0]_CSR_BUF_SR | BUF_SR | 0x4000a008 |
| CAN[0..0]_CSR_ERR_SR | ERR_SR | 0x4000a00c |
| CAN[0..0]_CSR_CMD | CMD | 0x4000a010 |
| CAN[0..0]_CSR_CFG | CFG | 0x4000a014 |
| CAN[0..0]_TX[0..7]_CMD | TXCMD | @0x4000a020 + [0..7 * 0x10] |
| CAN[0..0]_TX[0..7]_ID | TXID | @0x4000a020 + [0..7 * 0x10] + 0x4 |
| CAN[0..0]_TX[0..7]_DH | TXDH | @0x4000a020 + [0..7 * 0x10] + 0x8 |
| CAN[0..0]_TX[0..7]_DL | TXDL | @0x4000a020 + [0..7 * 0x10] + 0xc |
| CAN[0..0]_RX[0..15]_CMD | RXCMD | @0x4000a0a0 + [0..15 * 0x20] |
| CAN[0..0]_RX[0..15]_ID | RXID | @0x4000a0a0 + [0..15 * 0x20] + 0x4 |
| CAN[0..0]_RX[0..15]_DH | RXDH | @0x4000a0a0 + [0..15 * 0x20] + 0x8 |
| CAN[0..0]_RX[0..15]_DL | RXDL | @0x4000a0a0 + [0..15 * 0x20] + 0xc |
| CAN[0..0]_RX[0..15]_AMR | RXAMR | @0x4000a0a0 + [0..15 * 0x20] + 0x10 |
| CAN[0..0]_RX[0..15]_ACR | RXACR | @0x4000a0a0 + [0..15 * 0x20] + 0x14 |
| CAN[0..0]_RX[0..15]_AMRD | RXAMRD | @0x4000a0a0 + [0..15 * 0x20] + 0x18 |
| CAN[0..0]_RX[0..15]_ACRD | RXACRD | @0x4000a0a0 + [0..15 * 0x20] + 0x1c |
| DFB[0..0]_DPA_SRAM_DATA[0..127] | Data RAM A | @0x4000c000 + [0..127 * 0x4] |
| DFB[0..0]_DPB_SRAM_DATA[0..127] | DFB Data RAM B | @0x4000c200 + [0..127 * 0x4] |
| DFB[0..0]_CSA_SRAM_DATA[0..63] | DFB Control Store A | @0x4000c400 + [0..63 * 0x4] |

Register Mapping

| Register Name | Purpose | Address |
|--|---------------------------------------|--|
| DFB[0..0]_CSB_SRAM_DATA[0..63] | DFB Control Store B | @0x4000c500 + [0..63 * 0x4] |
| DFB[0..0]_FSM_SRAM_DATA[0..63] | DFB Code Store B | @0x4000c600 + [0..63 * 0x4] |
| DFB[0..0]_ACU_SRAM_DATA[0..15] | DFB Address Store | @0x4000c700 + [0..15 * 0x4] |
| DFB[0..0]_CR | DFB Command Register | 0x4000c780 |
| DFB[0..0]_SR | DFB Status Register | 0x4000c784 |
| DFB[0..0]_RAM_EN | DFB RAM Enable Register | 0x4000c788 |
| DFB[0..0]_RAM_DIR | DFB RAM Direction Register | 0x4000c78c |
| DFB[0..0]_SEMA | DFB Semaphore Register | 0x4000c790 |
| DFB[0..0]_DSI_CTRL | DFB Global Control Register | 0x4000c794 |
| DFB[0..0]_INT_CTRL | DFB Interrupt Control Register | 0x4000c798 |
| DFB[0..0]_DMA_CTRL | DFB DMAREQ Control Register | 0x4000c79c |
| DFB[0..0]_STAGEA | DFB Low Byte Staging Register A | 0x4000c7a0 |
| DFB[0..0]_STAGEAM | DFB Middle Byte Staging Register A | 0x4000c7a1 |
| DFB[0..0]_STAGEAH | DFB High Byte Staging Register A | 0x4000c7a2 |
| DFB[0..0]_STAGEB | DFB Low Byte Staging Register B | 0x4000c7a4 |
| DFB[0..0]_STAGEBM | DFB Middle Byte Staging Register B | 0x4000c7a5 |
| DFB[0..0]_STAGEBH | DFB High Byte Staging Register B | 0x4000c7a6 |
| DFB[0..0]_HOLDA | DFB Low Byte Holding Register A | 0x4000c7a8 |
| DFB[0..0]_HOLDAM | DFB Middle Byte Holding Register A | 0x4000c7a9 |
| DFB[0..0]_HOLDAH | DFB High Byte Holding Register A | 0x4000c7aa |
| DFB[0..0]_HOLDAS | DFB Holding Register A Sign Extension | 0x4000c7ab |
| DFB[0..0]_HOLDB | DFB Low Byte Holding Register B | 0x4000c7ac |
| DFB[0..0]_HOLDBM | DFB Middle Byte Holding Register B | 0x4000c7ad |
| DFB[0..0]_HOLDBH | DFB High Byte Holding Register B | 0x4000c7ae |
| DFB[0..0]_HOLDBS | DFB Holding Register B Sign Extension | 0x4000c7af |
| DFB[0..0]_COHER | DFB Coherency Register | 0x4000c7b0 |
| DFB[0..0]_DALIGN | DFB Data Alignment Register | 0x4000c7b4 |
| B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] | PLD_IT | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + [0..11 * 0x4] |
| B[0..3]_P[0..7]_U[0..1]_PLD_ORI[0..3] | PLD_ORI | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x30 + [0..3 * 0x2] |
| B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST | MC_CFG_CEN_CONST | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x38 |
| B[0..3]_P[0..7]_U[0..1]_MC_CFG_XORFB | MC_CFG_XORFB | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x3a |
| B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET | MC_CFG_SET_RESET | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x3c |
| B[0..3]_P[0..7]_U[0..1]_MC_CFG_BYPASS | MC_CFG_BYPASS | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x3e |
| B[0..3]_P[0..7]_U[0..1]_CFG0 | CFG0 | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x40 |
| B[0..3]_P[0..7]_U[0..1]_CFG1 | CFG1 | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x41 |
| B[0..3]_P[0..7]_U[0..1]_CFG2 | CFG2 | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x42 |
| B[0..3]_P[0..7]_U[0..1]_CFG3 | CFG3 | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x43 |

| Register Name | Purpose | Address |
|-------------------------------|---------|---|
| B[0..3]_P[0..7]_U[0..1]_CFG4 | CFG4 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x44 |
| B[0..3]_P[0..7]_U[0..1]_CFG5 | CFG5 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x45 |
| B[0..3]_P[0..7]_U[0..1]_CFG6 | CFG6 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x46 |
| B[0..3]_P[0..7]_U[0..1]_CFG7 | CFG7 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x47 |
| B[0..3]_P[0..7]_U[0..1]_CFG8 | CFG8 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x48 |
| B[0..3]_P[0..7]_U[0..1]_CFG9 | CFG9 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x49 |
| B[0..3]_P[0..7]_U[0..1]_CFG10 | CFG10 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4a |
| B[0..3]_P[0..7]_U[0..1]_CFG11 | CFG11 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4b |
| B[0..3]_P[0..7]_U[0..1]_CFG12 | CFG12 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4c |
| B[0..3]_P[0..7]_U[0..1]_CFG13 | CFG13 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4d |
| B[0..3]_P[0..7]_U[0..1]_CFG14 | CFG14 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4e |
| B[0..3]_P[0..7]_U[0..1]_CFG15 | CFG15 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4f |
| B[0..3]_P[0..7]_U[0..1]_CFG16 | CFG16 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x50 |
| B[0..3]_P[0..7]_U[0..1]_CFG17 | CFG17 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x51 |
| B[0..3]_P[0..7]_U[0..1]_CFG18 | CFG18 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x52 |
| B[0..3]_P[0..7]_U[0..1]_CFG19 | CFG19 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x53 |
| B[0..3]_P[0..7]_U[0..1]_CFG20 | CFG20 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x54 |
| B[0..3]_P[0..7]_U[0..1]_CFG21 | CFG21 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x55 |
| B[0..3]_P[0..7]_U[0..1]_CFG22 | CFG22 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x56 |
| B[0..3]_P[0..7]_U[0..1]_CFG23 | CFG23 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x57 |
| B[0..3]_P[0..7]_U[0..1]_CFG24 | CFG24 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x58 |
| B[0..3]_P[0..7]_U[0..1]_CFG25 | CFG25 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x59 |
| B[0..3]_P[0..7]_U[0..1]_CFG26 | CFG26 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5a |
| B[0..3]_P[0..7]_U[0..1]_CFG27 | CFG27 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5b |
| B[0..3]_P[0..7]_U[0..1]_CFG28 | CFG28 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5c |
| B[0..3]_P[0..7]_U[0..1]_CFG29 | CFG29 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5d |
| B[0..3]_P[0..7]_U[0..1]_CFG30 | CFG30 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5e |

Register Mapping

| Register Name | Purpose | Address |
|------------------------------------|---------|--|
| B[0..3]_P[0..7]_U[0..1]_CFG31 | CFG31 | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5f |
| B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] | DCFG | @(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x60 + [0..7 * 0x2] |
| B[0..3]_P[0..7]_ROUTE_HC[0..127] | HC | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x100 + [0..127 * 0x1] |
| B[0..3]_P[0..7]_ROUTE_HV_L[0..15] | HV_L | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x180 + [0..15 * 0x1] |
| B[0..3]_P[0..7]_ROUTE_HS[0..23] | HS | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x190 + [0..23 * 0x1] |
| B[0..3]_P[0..7]_ROUTE_HV_R[0..15] | HV_R | @((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x1a8 + [0..15 * 0x1] |
| B[0..3]_P[0..7]_ROUTE_PLD0IN0 | PLD0IN0 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1c0 |
| B[0..3]_P[0..7]_ROUTE_PLD0IN1 | PLD0IN1 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1c2 |
| B[0..3]_P[0..7]_ROUTE_PLD0IN2 | PLD0IN2 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1c4 |
| B[0..3]_P[0..7]_ROUTE_PLD1IN0 | PLD1IN0 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ca |
| B[0..3]_P[0..7]_ROUTE_PLD1IN1 | PLD1IN1 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1cc |
| B[0..3]_P[0..7]_ROUTE_PLD1IN2 | PLD1IN2 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ce |
| B[0..3]_P[0..7]_ROUTE_DPIN0 | DPIN0 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d0 |
| B[0..3]_P[0..7]_ROUTE_DPIN1 | DPIN1 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d2 |
| B[0..3]_P[0..7]_ROUTE_SCIN | SCIN | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d6 |
| B[0..3]_P[0..7]_ROUTE_SCI0IN | SCI0IN | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d8 |
| B[0..3]_P[0..7]_ROUTE_RCIN | RCIN | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1de |
| B[0..3]_P[0..7]_ROUTE_VS0 | VS0 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e0 |
| B[0..3]_P[0..7]_ROUTE_VS1 | VS1 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e2 |
| B[0..3]_P[0..7]_ROUTE_VS2 | VS2 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e4 |
| B[0..3]_P[0..7]_ROUTE_VS3 | VS3 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e6 |
| B[0..3]_P[0..7]_ROUTE_VS4 | VS4 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e8 |
| B[0..3]_P[0..7]_ROUTE_VS5 | VS5 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ea |
| B[0..3]_P[0..7]_ROUTE_VS6 | VS6 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ec |
| B[0..3]_P[0..7]_ROUTE_VS7 | VS7 | @(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ee |
| DSI[0..15]_HC[0..127] | HC | @(0x40014000 + [0..15 * 0x100]) + [0..127 * 0x1] |
| DSI[0..15]_HV_L[0..15] | HV_L | @(0x40014000 + [0..15 * 0x100]) + 0x80 + [0..15 * 0x1] |

| Register Name | Purpose | Address |
|------------------------|------------|--|
| DSI[0..15]_HS[0..23] | HS | @(0x40014000 + [0..15 * 0x100]) + 0x90 + [0..23 * 0x1] |
| DSI[0..15]_HV_R[0..15] | HV_R | @(0x40014000 + [0..15 * 0x100]) + 0xa8 + [0..15 * 0x1] |
| DSI[0..15]_DSIINP0 | DSIINP0 | @0x40014000 + [0..15 * 0x100] + 0xc0 |
| DSI[0..15]_DSIINP1 | DSIINP1 | @0x40014000 + [0..15 * 0x100] + 0xc2 |
| DSI[0..15]_DSIINP2 | DSIINP2 | @0x40014000 + [0..15 * 0x100] + 0xc4 |
| DSI[0..15]_DSIINP3 | DSIINP3 | @0x40014000 + [0..15 * 0x100] + 0xc6 |
| DSI[0..15]_DSIINP4 | DSIINP4 | @0x40014000 + [0..15 * 0x100] + 0xc8 |
| DSI[0..15]_DSIINP5 | DSIINP5 | @0x40014000 + [0..15 * 0x100] + 0xca |
| DSI[0..15]_DSIOUTP0 | DSIOUTP0 | @0x40014000 + [0..15 * 0x100] + 0xcc |
| DSI[0..15]_DSIOUTP1 | DSIOUTP1 | @0x40014000 + [0..15 * 0x100] + 0xce |
| DSI[0..15]_DSIOUTP2 | DSIOUTP2 | @0x40014000 + [0..15 * 0x100] + 0xd0 |
| DSI[0..15]_DSIOUTP3 | DSIOUTP3 | @0x40014000 + [0..15 * 0x100] + 0xd2 |
| DSI[0..15]_DSIOUTT0 | DSIOUTT0 | @0x40014000 + [0..15 * 0x100] + 0xd4 |
| DSI[0..15]_DSIOUTT1 | DSIOUTT1 | @0x40014000 + [0..15 * 0x100] + 0xd6 |
| DSI[0..15]_DSIOUTT2 | DSIOUTT2 | @0x40014000 + [0..15 * 0x100] + 0xd8 |
| DSI[0..15]_DSIOUTT3 | DSIOUTT3 | @0x40014000 + [0..15 * 0x100] + 0xda |
| DSI[0..15]_DSIOUTT4 | DSIOUTT4 | @0x40014000 + [0..15 * 0x100] + 0xdc |
| DSI[0..15]_DSIOUTT5 | DSIOUTT5 | @0x40014000 + [0..15 * 0x100] + 0xde |
| DSI[0..15]_VS0 | VS0 | @0x40014000 + [0..15 * 0x100] + 0xe0 |
| DSI[0..15]_VS1 | VS1 | @0x40014000 + [0..15 * 0x100] + 0xe2 |
| DSI[0..15]_VS2 | VS2 | @0x40014000 + [0..15 * 0x100] + 0xe4 |
| DSI[0..15]_VS3 | VS3 | @0x40014000 + [0..15 * 0x100] + 0xe6 |
| DSI[0..15]_VS4 | VS4 | @0x40014000 + [0..15 * 0x100] + 0xe8 |
| DSI[0..15]_VS5 | VS5 | @0x40014000 + [0..15 * 0x100] + 0xea |
| DSI[0..15]_VS6 | VS6 | @0x40014000 + [0..15 * 0x100] + 0xec |
| DSI[0..15]_VS7 | VS7 | @0x40014000 + [0..15 * 0x100] + 0xee |
| BCTL[0..3]_MDCLK_EN | MDCLK_EN | @0x40015000 + [0..3 * 0x10] |
| BCTL[0..3]_MBCLK_EN | MBCLK_EN | @0x40015000 + [0..3 * 0x10] + 0x1 |
| BCTL[0..3]_WAIT_CFG | WAIT_CFG | @0x40015000 + [0..3 * 0x10] + 0x2 |
| BCTL[0..3]_BANK_CTL | BANK_CTL | @0x40015000 + [0..3 * 0x10] + 0x3 |
| BCTL[0..3]_UDB_TEST_0 | UDB_TEST_0 | @0x40015000 + [0..3 * 0x10] + 0x4 |
| BCTL[0..3]_UDB_TEST_1 | UDB_TEST_1 | @0x40015000 + [0..3 * 0x10] + 0x5 |
| BCTL[0..3]_UDB_TEST_2 | UDB_TEST_2 | @0x40015000 + [0..3 * 0x10] + 0x6 |
| BCTL[0..3]_UDB_TEST_3 | UDB_TEST_3 | @0x40015000 + [0..3 * 0x10] + 0x7 |
| BCTL[0..3]_DCLK_EN0 | DCLK_EN | @0x40015000 + [0..3 * 0x10] + 0x8 |
| BCTL[0..3]_BCLK_EN0 | BCLK_EN | @0x40015000 + [0..3 * 0x10] + 0x9 |
| BCTL[0..3]_DCLK_EN1 | DCLK_EN | @0x40015000 + [0..3 * 0x10] + 0xa |
| BCTL[0..3]_BCLK_EN1 | BCLK_EN | @0x40015000 + [0..3 * 0x10] + 0xb |
| BCTL[0..3]_DCLK_EN2 | DCLK_EN | @0x40015000 + [0..3 * 0x10] + 0xc |
| BCTL[0..3]_BCLK_EN2 | BCLK_EN | @0x40015000 + [0..3 * 0x10] + 0xd |
| BCTL[0..3]_DCLK_EN3 | DCLK_EN | @0x40015000 + [0..3 * 0x10] + 0xe |

| Register Name | Purpose | Address |
|-----------------------|--------------------------------|-----------------------------------|
| BCTL[0..3]_BCLK_EN3 | BCLK_EN | @0x40015000 + [0..3 * 0x10] + 0xf |
| IDMUX_IRQ_CTL[0..7] | Control Register IRQ_CTL | @0x40015100 + [0..7 * 0x1] |
| IDMUX_DRQ_CTL[0..5] | Configuration Register DRQ_CTL | @0x40015110 + [0..5 * 0x1] |
| CACHERAM_DATA[0..255] | Cache SRAM | @0x40030000 + [0..255 * 0x4] |
| SFR_GPIO0 | GPIO0 Register | 0x40050180 |
| SFR_GPIRD0 | GPIRD0 Register | 0x40050189 |
| SFR_GPIO0_SEL | GPIO0_SEL Register | 0x4005018a |
| SFR_GPIO1 | GPIO1 Register | 0x40050190 |
| SFR_GPIRD1 | GPIRD1 Register | 0x40050191 |
| SFR_GPIO2 | GPIO2 Register | 0x40050198 |
| SFR_GPIRD2 | GPIRD2 Register | 0x40050199 |
| SFR_GPIO2_SEL | GPIO2_SEL Register | 0x4005019a |
| SFR_GPIO1_SEL | GPIO1_SEL Register | 0x400501a2 |
| SFR_GPIO3 | GPIO3 Register | 0x400501b0 |
| SFR_GPIRD3 | GPIRD3 Register | 0x400501b1 |
| SFR_GPIO3_SEL | GPIO3_SEL Register | 0x400501b2 |
| SFR_GPIO4 | GPIO4 Register | 0x400501c0 |
| SFR_GPIRD4 | GPIRD4 Register | 0x400501c1 |
| SFR_GPIO4_SEL | GPIO4_SEL Register | 0x400501c2 |
| SFR_GPIO5 | GPIO5 Register | 0x400501c8 |
| SFR_GPIRD5 | GPIRD5 Register | 0x400501c9 |
| SFR_GPIO5_SEL | GPIO5_SEL Register | 0x400501ca |
| SFR_GPIO6 | GPIO6 Register | 0x400501d8 |
| SFR_GPIRD6 | GPIRD6 Register | 0x400501d9 |
| SFR_GPIO6_SEL | GPIO6_SEL Register | 0x400501da |
| SFR_GPIO12 | GPIO12 Register | 0x400501e8 |
| SFR_GPIRD12 | GPIRD12 Register | 0x400501e9 |
| SFR_GPIO12_SEL | GPIO12_SEL Register | 0x400501f2 |
| SFR_GPIO15 | GPIO15 Register | 0x400501f8 |
| SFR_GPIRD15 | GPIRD15 Register | 0x400501f9 |
| SFR_GPIO15_SEL | GPIO15_SEL Register | 0x400501fa |
| TC_TST_CR1 | Test Control Register 1 | 0x40050200 |
| TC_TST_CR2 | Test Control Register 2 | 0x40050201 |
| TC_TST_CR3 | Test Control Register 3 | 0x40050202 |
| TC_TST_CR4 | Test Control Register 4 | 0x40050203 |
| TC_TST_CR5 | Test Control Register 5 | 0x40050204 |
| TC_TST_CR6 | Test Control Register 6 | 0x40050205 |
| TC_TST_KEY | Test Key Register | 0x40050210 |
| TC_PM_CTRL | Power Mode Control | 0x40050214 |
| P3BA_Y_START | Y_START | 0x40050300 |
| P3BA_YROLL | YROLL | 0x40050301 |
| P3BA_YCFG | YCFG | 0x40050302 |

| Register Name | Purpose | Address |
|----------------------|-------------------------------|------------|
| P3BA_X_START1 | X_START1 | 0x40050303 |
| P3BA_X_START2 | X_START2 | 0x40050304 |
| P3BA_XROLL1 | XROLL1 | 0x40050305 |
| P3BA_XROLL2 | XROLL2 | 0x40050306 |
| P3BA_XINC | XINC | 0x40050307 |
| P3BA_XCFG | XCFG | 0x40050308 |
| P3BA_OFFSETADDR1 | OFFSETADDR1 | 0x40050309 |
| P3BA_OFFSETADDR2 | OFFSETADDR2 | 0x4005030a |
| P3BA_OFFSETADDR3 | OFFSETADDR3 | 0x4005030b |
| P3BA_ABSADDR1 | ABSADDR1 | 0x4005030c |
| P3BA_ABSADDR2 | ABSADDR2 | 0x4005030d |
| P3BA_ABSADDR3 | ABSADDR3 | 0x4005030e |
| P3BA_ABSADDR4 | ABSADDR4 | 0x4005030f |
| P3BA_DATCFG1 | DATCFG1 | 0x40050310 |
| P3BA_DATCFG2 | DATCFG2 | 0x40050311 |
| P3BA_CMP_RSLT1 | CMP_RSLT1 | 0x40050314 |
| P3BA_CMP_RSLT2 | CMP_RSLT2 | 0x40050315 |
| P3BA_CMP_RSLT3 | CMP_RSLT3 | 0x40050316 |
| P3BA_CMP_RSLT4 | CMP_RSLT4 | 0x40050317 |
| P3BA_DATA_REG1 | DATA_REG1 | 0x40050318 |
| P3BA_DATA_REG2 | DATA_REG2 | 0x40050319 |
| P3BA_DATA_REG3 | DATA_REG3 | 0x4005031a |
| P3BA_DATA_REG4 | DATA_REG4 | 0x4005031b |
| P3BA_EXP_DATA1 | EXP_DATA1 | 0x4005031c |
| P3BA_EXP_DATA2 | EXP_DATA2 | 0x4005031d |
| P3BA_EXP_DATA3 | EXP_DATA3 | 0x4005031e |
| P3BA_EXP_DATA4 | EXP_DATA4 | 0x4005031f |
| P3BA_MSTR_HRDATA1 | MSTR_HRDATA1 | 0x40050320 |
| P3BA_MSTR_HRDATA2 | MSTR_HRDATA2 | 0x40050321 |
| P3BA_MSTR_HRDATA3 | MSTR_HRDATA3 | 0x40050322 |
| P3BA_MSTR_HRDATA4 | MSTR_HRDATA4 | 0x40050323 |
| P3BA_BIST_EN | BIST_EN | 0x40050324 |
| P3BA_PHUB_MASTER_SSR | PHUB_MASTER_SSR | 0x40050325 |
| P3BA_SEQCFG1 | SEQCFG1 | 0x40050326 |
| P3BA_SEQCFG2 | SEQCFG2 | 0x40050327 |
| P3BA_Y_CURR | Y_CURR | 0x40050328 |
| P3BA_X_CURR1 | X_CURR1 | 0x40050329 |
| P3BA_X_CURR2 | X_CURR2 | 0x4005032a |
| PANTHER_STCALIB_CFG | SYSTICK Calibration register | 0x40080000 |
| PANTHER_WAITPIPE | Wait State Pipeline | 0x40080004 |
| PANTHER_TRACE_CFG | Debug Trace Configuration | 0x40080008 |
| PANTHER_DBG_CFG | Embedded Trace Overflow Stall | 0x4008000c |

| Register Name | Purpose | Address |
|--------------------------------|-------------------------|--------------------------------|
| PANTHER_CM3_LCKRST_STAT | Status Register | 0x40080018 |
| PANTHER_DEVICE_ID | Device Identification | 0x4008001c |
| FLSECC_DATA[0..32767] | DATA | @0x48000000 + [0..32767 * 0x1] |
| FLSHID_RSVD[0..127] | RSVD | @0x49000000 + [0..127 * 0x1] |
| FLSHID_CUST_MDATA[0..127] | Customer Meta Data | @0x49000080 + [0..127 * 0x1] |
| FLSHID_CUST_TABLES_Y_LOC | Y location | 0x49000100 |
| FLSHID_CUST_TABLES_X_LOC | X location | 0x49000101 |
| FLSHID_CUST_TABLES_WAFER_NUM | Wafer Number | 0x49000102 |
| FLSHID_CUST_TABLES_LOT_LSB | Lot Number LSB | 0x49000103 |
| FLSHID_CUST_TABLES_LOT_MSB | Lot Number MSB | 0x49000104 |
| FLSHID_CUST_TABLES_WRK_WK | Work Week | 0x49000105 |
| FLSHID_CUST_TABLES_FAB_YR | Fab/Yr | 0x49000106 |
| FLSHID_CUST_TABLES_MINOR | Minor Part Number | 0x49000107 |
| FLSHID_CUST_TABLES_IMO_3MHZ | IMO Trim - 3 MHz | 0x49000108 |
| FLSHID_CUST_TABLES_IMO_6MHZ | IMO Trim - 6 MHz | 0x49000109 |
| FLSHID_CUST_TABLES_IMO_12MHZ | IMO Trim - 12 MHz | 0x4900010a |
| FLSHID_CUST_TABLES_IMO_24MHZ | IMO Trim - 24 MHz | 0x4900010b |
| FLSHID_CUST_TABLES_IMO_67MHZ | IMO Trim - 67 MHz | 0x4900010c |
| FLSHID_CUST_TABLES_IMO_80MHZ | IMO Trim - 80 MHz | 0x4900010d |
| FLSHID_CUST_TABLES_IMO_92MHZ | IMO Trim - 92 MHz | 0x4900010e |
| FLSHID_CUST_TABLES_IMO_USB | IMO Trim - USB Mode | 0x4900010f |
| FLSHID_CUST_TABLES_CMP0_TR0_HS | CMP0_TR0 High Speed | 0x49000110 |
| FLSHID_CUST_TABLES_CMP1_TR0_HS | CMP1_TR0 High Speed | 0x49000111 |
| FLSHID_CUST_TABLES_CMP2_TR0_HS | CMP2_TR0 High Speed | 0x49000112 |
| FLSHID_CUST_TABLES_CMP3_TR0_HS | CMP3_TR0 High Speed | 0x49000113 |
| FLSHID_CUST_TABLES_CMP0_TR1_HS | CMP0_TR1 High Speed | 0x49000114 |
| FLSHID_CUST_TABLES_CMP1_TR1_HS | CMP1_TR1 High Speed | 0x49000115 |
| FLSHID_CUST_TABLES_CMP2_TR1_HS | CMP2_TR1 High Speed | 0x49000116 |
| FLSHID_CUST_TABLES_CMP3_TR1_HS | CMP3_TR1 High Speed | 0x49000117 |
| FLSHID_CUST_TABLES_DEC_M1 | Decimator Trim - Mode 1 | 0x49000118 |
| FLSHID_CUST_TABLES_DEC_M2 | Decimator Trim - mode 2 | 0x49000119 |
| FLSHID_CUST_TABLES_DEC_M3 | Decimator Trim - mode 3 | 0x4900011a |
| FLSHID_CUST_TABLES_DEC_M4 | Decimator Trim - mode 4 | 0x4900011b |
| FLSHID_CUST_TABLES_DEC_M5 | Decimator Trim - mode 5 | 0x4900011c |
| FLSHID_CUST_TABLES_DEC_M6 | Decimator Trim - mode 6 | 0x4900011d |
| FLSHID_CUST_TABLES_DEC_M7 | Decimator Trim - Mode 7 | 0x4900011e |
| FLSHID_CUST_TABLES_DEC_M8 | Decimator Trim - Mode 8 | 0x4900011f |
| FLSHID_CUST_TABLES_DAC0_M1 | DAC0_TR Trim - Mode 1 | 0x49000120 |
| FLSHID_CUST_TABLES_DAC0_M2 | DAC0_TR Trim - mode 2 | 0x49000121 |
| FLSHID_CUST_TABLES_DAC0_M3 | DAC0_TR Trim - mode 3 | 0x49000122 |
| FLSHID_CUST_TABLES_DAC0_M4 | DAC0_TR Trim - mode 4 | 0x49000123 |
| FLSHID_CUST_TABLES_DAC0_M5 | DAC0_TR Trim - mode 5 | 0x49000124 |

| Register Name | Purpose | Address |
|-------------------------------|-----------------------|-----------------------------|
| FLSHID_CUST_TABLES_DAC0_M6 | DAC0_TR Trim - mode 6 | 0x49000125 |
| FLSHID_CUST_TABLES_DAC0_M7 | DAC0_TR Trim - mode 7 | 0x49000126 |
| FLSHID_CUST_TABLES_DAC0_M8 | DAC0_TR Trim - mode 8 | 0x49000127 |
| FLSHID_CUST_TABLES_DAC2_M1 | DAC2_TR Trim - Mode 1 | 0x49000128 |
| FLSHID_CUST_TABLES_DAC2_M2 | DAC2_TR Trim - mode 2 | 0x49000129 |
| FLSHID_CUST_TABLES_DAC2_M3 | DAC2_TR Trim - mode 3 | 0x4900012a |
| FLSHID_CUST_TABLES_DAC2_M4 | DAC2_TR Trim - mode 4 | 0x4900012b |
| FLSHID_CUST_TABLES_DAC2_M5 | DAC2_TR Trim - mode 5 | 0x4900012c |
| FLSHID_CUST_TABLES_DAC2_M6 | DAC2_TR Trim - mode 6 | 0x4900012d |
| FLSHID_CUST_TABLES_DAC2_M7 | DAC2_TR Trim - mode 7 | 0x4900012e |
| FLSHID_CUST_TABLES_DAC2_M8 | DAC2_TR Trim - mode 8 | 0x4900012f |
| FLSHID_CUST_TABLES_DAC1_M1 | DAC1_TR Trim - Mode 1 | 0x49000130 |
| FLSHID_CUST_TABLES_DAC1_M2 | DAC1_TR Trim - mode 2 | 0x49000131 |
| FLSHID_CUST_TABLES_DAC1_M3 | DAC1_TR Trim - mode 3 | 0x49000132 |
| FLSHID_CUST_TABLES_DAC1_M4 | DAC1_TR Trim - mode 4 | 0x49000133 |
| FLSHID_CUST_TABLES_DAC1_M5 | DAC1_TR Trim - mode 5 | 0x49000134 |
| FLSHID_CUST_TABLES_DAC1_M6 | DAC1_TR Trim - mode 6 | 0x49000135 |
| FLSHID_CUST_TABLES_DAC1_M7 | DAC1_TR Trim - mode 7 | 0x49000136 |
| FLSHID_CUST_TABLES_DAC1_M8 | DAC1_TR Trim - mode 8 | 0x49000137 |
| FLSHID_CUST_TABLES_DAC3_M1 | DAC3_TR Trim - Mode 1 | 0x49000138 |
| FLSHID_CUST_TABLES_DAC3_M2 | DAC3_TR Trim - mode 2 | 0x49000139 |
| FLSHID_CUST_TABLES_DAC3_M3 | DAC3_TR Trim - mode 3 | 0x4900013a |
| FLSHID_CUST_TABLES_DAC3_M4 | DAC3_TR Trim - mode 4 | 0x4900013b |
| FLSHID_CUST_TABLES_DAC3_M5 | DAC3_TR Trim - mode 5 | 0x4900013c |
| FLSHID_CUST_TABLES_DAC3_M6 | DAC3_TR Trim - mode 6 | 0x4900013d |
| FLSHID_CUST_TABLES_DAC3_M7 | DAC3_TR Trim - mode 7 | 0x4900013e |
| FLSHID_CUST_TABLES_DAC3_M8 | DAC3_TR Trim - mode 8 | 0x4900013f |
| FLSHID_PETE_DATA[0..31] | PE/TE Data | @0x49000140 + [0..31 * 0x1] |
| FLSHID_SPC_PARAMS[0..31] | SPC Parameters | @0x49000160 + [0..31 * 0x1] |
| FLSHID_MFG_CFG_WNDG_CFG0 | MLOGIC_WNDG_CFG0 Trim | 0x49000180 |
| FLSHID_MFG_CFG_WNDG_CFG1 | MLOGIC_WNDG_CFG1 Trim | 0x49000182 |
| FLSHID_MFG_CFG_PWRSYS_BG_TR | PWRSYS_BG_TR Trim | 0x49000184 |
| FLSHID_MFG_CFG_RESET_TR | RESET_TR Trim | 0x49000186 |
| FLSHID_MFG_CFG_IMO_TR1 | IMO_TR1 Trim | 0x49000188 |
| FLSHID_MFG_CFG_IMO_GAIN | IMO_GAIN Trim | 0x4900018a |
| FLSHID_MFG_CFG_IMO_TR2 | IMO_TR2 Trim | 0x4900018c |
| FLSHID_MFG_CFG_IMO_C36M | IMO_C36M Trim | 0x4900018e |
| FLSHID_MFG_CFG_PWRSYS_BREF_TR | PWRSYS_BREF_TR Trim | 0x49000190 |
| FLSHID_MFG_CFG_PWRSYS_BUZZ_TR | PWRSYS_BUZZ_TR Trim | 0x49000192 |
| FLSHID_MFG_CFG_PWRSYS_I2C_TR | PWRSYS_I2C_TR Trim | 0x49000194 |
| FLSHID_MFG_CFG_PWRSYS_HIB_TR0 | PWRSYS_HIB_TR0 Trim | 0x49000196 |
| FLSHID_MFG_CFG_PWRSYS_HIB_TR1 | PWRSYS_HIB_TR1 Trim | 0x49000198 |

Register Mapping

| Register Name | Purpose | Address |
|----------------------------------|--|----------------------------------|
| FLSHID_MFG_CFG_PWRSYS_SLP_TR | PWRSYS_SLP_TR Trim | 0x4900019a |
| FLSHID_MFG_CFG_ILO_TR0 | ILO_TR0 Trim | 0x4900019c |
| FLSHID_MFG_CFG_ILO_TR1 | ILO_TR1 Trim | 0x4900019e |
| FLSHID_MFG_CFG_X32_TR | X32_TR Trim | 0x490001a0 |
| FLSHID_MFG_CFG_XMHZ_TR | XMHZ_TR Trim | 0x490001a2 |
| FLSHID_MFG_CFG_OPAMP0_TR0 | OPAMP0_TR0 Trim | 0x490001a4 |
| FLSHID_MFG_CFG_OPAMP1_TR0 | OPAMP1_TR0 Trim | 0x490001a6 |
| FLSHID_MFG_CFG_OPAMP2_TR0 | OPAMP2_TR0 Trim | 0x490001a8 |
| FLSHID_MFG_CFG_OPAMP3_TR0 | OPAMP3_TR0 Trim | 0x490001aa |
| FLSHID_MFG_CFG_CMP0_TR0 | CMP0_TR0 Trim | 0x490001ac |
| FLSHID_MFG_CFG_CMP1_TR0 | CMP1_TR0 Trim | 0x490001ae |
| FLSHID_MFG_CFG_CMP2_TR0 | CMP2_TR0 Trim | 0x490001b0 |
| FLSHID_MFG_CFG_CMP3_TR0 | CMP3_TR0 Trim | 0x490001b2 |
| FLSHID_MFG_CFG_CMP0_TR1 | CMP0_TR1 Trim | 0x490001b4 |
| FLSHID_MFG_CFG_CMP1_TR1 | CMP1_TR1 Trim | 0x490001b6 |
| FLSHID_MFG_CFG_CMP2_TR1 | CMP2_TR1 Trim | 0x490001b8 |
| FLSHID_MFG_CFG_CMP3_TR1 | CMP3_TR1 Trim | 0x490001ba |
| FLSHID_MFG_CFG_IPOR_CR0 | IPOR_CR0 Trim | 0x490001bc |
| FLSHID_MFG_CFG_IPOR_CR1 | IPOR_CR1 Trim | 0x490001be |
| FLSHID_MFG_CFG_IPOR_CR2 | IPOR_CR2 Trim | 0x490001c0 |
| FLSHID_MFG_CFG_IPOR_CR3 | IPOR_CR3 Trim | 0x490001c2 |
| FLSHID_MFG_CFG_DLY | DLY Trim | 0x490001c4 |
| FLSHID_MFG_CFG_RESERVED[0..3] | Reserved | @0x490001c6 + [0..3 * 0x2] |
| FLSHID_MFG_CFG_BG_XOVER_INL_TRIM | Bandgap Crossover Trim | 0x490001ce |
| FLSHID_MFG_CFG_RSVD[0..15] | Reserved | @0x490001d0 + [0..15 * 0x2] |
| FLSHID_MFG_CFG_PWRSYS_WAKE_TR0 | PWRSYS_WAKE_TR0 Trim | 0x490001f0 |
| FLSHID_MFG_CFG_PWRSYS_WAKE_TR1 | PWRSYS_WAKE_TR1 Trim | 0x490001f2 |
| FLSHID_MFG_CFG_PWRSYS_WAKE_TR2 | PWRSYS_WAKE_TR2 Trim | 0x490001f4 |
| FLSHID_MFG_CFG_PWRSYS_WAKE_TR3 | PWRSYS_WAKE_TR3 Trim | 0x490001f6 |
| FLSHID_MFG_CFG_RSVD_2[0..2] | Reserved | @0x490001f8 + [0..2 * 0x2] |
| FLSHID_MFG_CFG_CHKSM | Boot Checksum | 0x490001fe |
| EXTMEM_DATA[0..8388607] | DATA | @0x60000000 + [0..8388607 * 0x1] |
| ITM_TRACE_EN | ITM Trace Enable Register | 0xe0000e00 |
| ITM_TRACE_PRIVILEGE | ITM Trace Privilege Register | 0xe0000e40 |
| ITM_TRACE_CTRL | ITM Trace Control Register | 0xe0000e80 |
| ITM_LOCK_ACCESS | ITM Lock Access Register | 0xe0000fb0 |
| ITM_LOCK_STATUS | ITM Lock Status Register | 0xe0000fb4 |
| ITM_PID4 | ITM Peripheral Identification Register 4 | 0xe0000fd0 |
| ITM_PID5 | ITM Peripheral Identification Register 5 | 0xe0000fd4 |
| ITM_PID6 | ITM Peripheral Identification Register 6 | 0xe0000fd8 |
| ITM_PID7 | ITM Peripheral Identification Register 7 | 0xe0000fdc |
| ITM_PID0 | ITM Peripheral Identification Register 0 | 0xe0000fe0 |

| Register Name | Purpose | Address |
|--------------------|---|------------|
| ITM_PID1 | ITM Peripheral Identification Register 1 | 0xe000fe4 |
| ITM_PID2 | ITM Peripheral Identification Register 2 | 0xe000fe8 |
| ITM_PID3 | ITM Peripheral Identification Register 3 | 0xe000fec |
| ITM_CID0 | ITM Component Identification Register 0 | 0xe000ff0 |
| ITM_CID1 | ITM Component Identification Register 1 | 0xe000ff4 |
| ITM_CID2 | ITM Component Identification Register 2 | 0xe000ff8 |
| ITM_CID3 | ITM Component Identification Register 3 | 0xe000ffc |
| DWT_CTRL | DWT Control Register | 0xe0001000 |
| DWT_CYCLE_COUNT | DWT Current PC Sampler Cycle Count Register | 0xe0001004 |
| DWT_CPI_COUNT | DWT CPI Count Register | 0xe0001008 |
| DWT_EXC_OVHD_COUNT | DWT Exception Overhead Count Register | 0xe000100c |
| DWT_SLEEP_COUNT | DWT Sleep Count Register | 0xe0001010 |
| DWT_LSU_COUNT | DWT LSU Count Register | 0xe0001014 |
| DWT_FOLD_COUNT | DWT Fold Count Register | 0xe0001018 |
| DWT_PC_SAMPLE | DWT Program Counter Sample Register | 0xe000101c |
| DWT_COMP_0 | DWT Comparator Registers | 0xe0001020 |
| DWT_MASK_0 | DWT Mask Registers | 0xe0001024 |
| DWT_FUNCTION_0 | DWT Function registers | 0xe0001028 |
| DWT_COMP_1 | DWT Comparator Registers | 0xe0001030 |
| DWT_MASK_1 | DWT Mask Registers | 0xe0001034 |
| DWT_FUNCTION_1 | DWT Function registers | 0xe0001038 |
| DWT_COMP_2 | DWT Comparator Registers | 0xe0001040 |
| DWT_MASK_2 | DWT Mask Registers | 0xe0001044 |
| DWT_FUNCTION_2 | DWT Function registers | 0xe0001048 |
| DWT_COMP_3 | DWT Comparator Registers | 0xe0001050 |
| DWT_MASK_3 | DWT Mask Registers | 0xe0001054 |
| DWT_FUNCTION_3 | DWT Function registers | 0xe0001058 |
| FPB_CTRL | Flash Patch Control Register | 0xe0002000 |
| FPB_REMAP | Flash Patch Remap Register | 0xe0002004 |
| FPB_FP_COMP_0 | Flash Patch Comparator Registers | 0xe0002008 |
| FPB_FP_COMP_1 | Flash Patch Comparator Registers | 0xe000200c |
| FPB_FP_COMP_2 | Flash Patch Comparator Registers | 0xe0002010 |
| FPB_FP_COMP_3 | Flash Patch Comparator Registers | 0xe0002014 |
| FPB_FP_COMP_4 | Flash Patch Comparator Registers | 0xe0002018 |
| FPB_FP_COMP_5 | Flash Patch Comparator Registers | 0xe000201c |
| FPB_FP_COMP_6 | Flash Patch Comparator Registers | 0xe0002020 |
| FPB_FP_COMP_7 | Flash Patch Comparator Registers | 0xe0002024 |
| FPB_PID4 | FPB Peripheral Identification Register 4 | 0xe0002fd0 |
| FPB_PID5 | FPB Peripheral Identification Register 5 | 0xe0002fd4 |
| FPB_PID6 | FPB Peripheral Identification Register 6 | 0xe0002fd8 |
| FPB_PID7 | FPB Peripheral Identification Register 7 | 0xe0002fdc |
| FPB_PID0 | FPB Peripheral Identification Register 0 | 0xe0002fe0 |

| Register Name | Purpose | Address |
|----------------------|--|------------|
| FPB_PID1 | FPB Peripheral Identification Register 1 | 0xe0002fe4 |
| FPB_PID2 | FPB Peripheral Identification Register 2 | 0xe0002fe8 |
| FPB_PID3 | FPB Peripheral Identification Register 3 | 0xe0002fec |
| FPB_CID0 | FPB Component Identification Register 0 | 0xe0002ff0 |
| FPB_CID1 | FPB Component Identification Register 1 | 0xe0002ff4 |
| FPB_CID2 | FPB Component Identification Register 2 | 0xe0002ff8 |
| FPB_CID3 | FPB Component Identification Register 3 | 0xe0002ffc |
| NVIC_INT_CTL_TYPE | Interrupt Controller Type Register | 0xe000e004 |
| NVIC_SYSTICK_CTL | SYSTICK Control and Status register | 0xe000e010 |
| NVIC_SYSTICK_RELOAD | SYSTICK Reload value | 0xe000e014 |
| NVIC_SYSTICK_CURRENT | SYSTICK Counter | 0xe000e018 |
| NVIC_SYSTICK_CAL | SYSTICK Calibration register | 0xe000e01c |
| NVIC_SETENA0 | Interrupt Enable Set 0-31 | 0xe000e100 |
| NVIC_CLRENA0 | Interrupt Enable Clear 0-31 | 0xe000e180 |
| NVIC_SETPEND0 | Interrupt Pending Set 0-31 | 0xe000e200 |
| NVIC_CLRPEND0 | Interrupt Pending Clear 0-31 | 0xe000e280 |
| NVIC_ACTIVE0 | Active Interrupts 0-31 | 0xe000e300 |
| NVIC_PRI_0 | Interrupt Priority 0-31 | 0xe000e400 |
| NVIC_PRI_1 | Interrupt Priority 0-31 | 0xe000e401 |
| NVIC_PRI_2 | Interrupt Priority 0-31 | 0xe000e402 |
| NVIC_PRI_3 | Interrupt Priority 0-31 | 0xe000e403 |
| NVIC_PRI_4 | Interrupt Priority 0-31 | 0xe000e404 |
| NVIC_PRI_5 | Interrupt Priority 0-31 | 0xe000e405 |
| NVIC_PRI_6 | Interrupt Priority 0-31 | 0xe000e406 |
| NVIC_PRI_7 | Interrupt Priority 0-31 | 0xe000e407 |
| NVIC_PRI_8 | Interrupt Priority 0-31 | 0xe000e408 |
| NVIC_PRI_9 | Interrupt Priority 0-31 | 0xe000e409 |
| NVIC_PRI_10 | Interrupt Priority 0-31 | 0xe000e40a |
| NVIC_PRI_11 | Interrupt Priority 0-31 | 0xe000e40b |
| NVIC_PRI_12 | Interrupt Priority 0-31 | 0xe000e40c |
| NVIC_PRI_13 | Interrupt Priority 0-31 | 0xe000e40d |
| NVIC_PRI_14 | Interrupt Priority 0-31 | 0xe000e40e |
| NVIC_PRI_15 | Interrupt Priority 0-31 | 0xe000e40f |
| NVIC_PRI_16 | Interrupt Priority 0-31 | 0xe000e410 |
| NVIC_PRI_17 | Interrupt Priority 0-31 | 0xe000e411 |
| NVIC_PRI_18 | Interrupt Priority 0-31 | 0xe000e412 |
| NVIC_PRI_19 | Interrupt Priority 0-31 | 0xe000e413 |
| NVIC_PRI_20 | Interrupt Priority 0-31 | 0xe000e414 |
| NVIC_PRI_21 | Interrupt Priority 0-31 | 0xe000e415 |
| NVIC_PRI_22 | Interrupt Priority 0-31 | 0xe000e416 |
| NVIC_PRI_23 | Interrupt Priority 0-31 | 0xe000e417 |
| NVIC_PRI_24 | Interrupt Priority 0-31 | 0xe000e418 |

| Register Name | Purpose | Address |
|-----------------------------|--|------------|
| NVIC_PRI_25 | Interrupt Priority 0-31 | 0xe000e419 |
| NVIC_PRI_26 | Interrupt Priority 0-31 | 0xe000e41a |
| NVIC_PRI_27 | Interrupt Priority 0-31 | 0xe000e41b |
| NVIC_PRI_28 | Interrupt Priority 0-31 | 0xe000e41c |
| NVIC_PRI_29 | Interrupt Priority 0-31 | 0xe000e41d |
| NVIC_PRI_30 | Interrupt Priority 0-31 | 0xe000e41e |
| NVIC_PRI_31 | Interrupt Priority 0-31 | 0xe000e41f |
| NVIC_CPUID_BASE | CPU ID Base Register | 0xe000ed00 |
| NVIC_INTR_CTRL_STATE | Interrupt Control State Register | 0xe000ed04 |
| NVIC_VECT_OFFSET | Interrupt Vector Table Offset | 0xe000ed08 |
| NVIC_APPLN_INTR | Application Interrupt and Reset Control Register | 0xe000ed0c |
| NVIC_SYSTEM_CONTROL | System Control Register | 0xe000ed10 |
| NVIC_CFG_CONTROL | Configuration Control Register | 0xe000ed14 |
| NVIC_SYS_PRIO_HANDLER_4_7 | System Handler Priority Registers | 0xe000ed18 |
| NVIC_SYS_PRIO_HANDLER_8_11 | System Handler Priority Registers | 0xe000ed1c |
| NVIC_SYS_PRIO_HANDLER_12_15 | System Handler Priority Registers | 0xe000ed20 |
| NVIC_SYS_HANDLER_CSR | System Handler Control and State Register | 0xe000ed24 |
| NVIC_MEMMAN_FAULT_STATUS | Memory Manage Fault Status Registers. | 0xe000ed28 |
| NVIC_BUS_FAULT_STATUS | Bus Fault Status Register | 0xe000ed29 |
| NVIC_USAGE_FAULT_STATUS | Usage Fault Status Register | 0xe000ed2a |
| NVIC_HARD_FAULT_STATUS | Hard Fault Status Register | 0xe000ed2c |
| NVIC_DEBUG_FAULT_STATUS | Debug Fault Status Register | 0xe000ed30 |
| NVIC_MEMMAN_FAULT_ADD | Memory Manage Fault Address Register | 0xe000ed34 |
| NVIC_BUS_FAULT_ADD | Bus Fault Address Register | 0xe000ed38 |
| CORE_DBG_DBG_HLT_CS | Debug Halting Control and Status register | 0xe000edf0 |
| CORE_DBG_DBG_REG_SEL | Debug Core Register Selector Register | 0xe000edf4 |
| CORE_DBG_DBG_REG_DATA | Debug Core Register Data Register | 0xe000edf8 |
| CORE_DBG_EXC_MON_CTL | Debug Exception and Monitor Control register | 0xe000edfc |
| TPIU_SUPPORTED_SYNC_PRT_SZ | Supported Sync Port Sizes Register | 0xe0040000 |
| TPIU_CURRENT_SYNC_PRT_SZ | Current Sync Port Size Register | 0xe0040004 |
| TPIU_ASYNC_CLK_PRESCALER | Async Clock Prescaler Register | 0xe0040010 |
| TPIU_PROTOCOL | Selected Pin Protocol Register | 0xe00400f0 |
| TPIU_FORM_FLUSH_STAT | Formatter and Flush Status Register | 0xe0040300 |
| TPIU_FORM_FLUSH_CTRL | Formatter and Flush Control Register | 0xe0040304 |
| TPIU_TRIGGER | Integration test of the TRIGGER input. | 0xe0040ee8 |
| TPIU_ITETMDATA | Integration ETM Data | 0xe0040eec |
| TPIU_ITATBCTR2 | Integration Test Registers | 0xe0040ef0 |
| TPIU_ITATBCTR0 | Integration Test Registers | 0xe0040ef8 |
| TPIU_ITITMDATA | Integration ITM Data | 0xe0040efc |
| TPIU_ITCTRL | Integration Mode Control | 0xe0040f00 |
| TPIU_DEVID | TPIU Provided Function Register | 0xe0040fc8 |
| TPIU_DEVTTYPE | TPIU Device Type Identifier Register | 0xe0040fcc |

| Register Name | Purpose | Address |
|-----------------------|---|------------|
| TPIU_PID4 | TPIU Peripheral Identification Register 4 | 0xe0040fd0 |
| TPIU_PID5 | TPIU Peripheral Identification Register 5 | 0xe0040fd4 |
| TPIU_PID6 | TPIU Peripheral Identification Register 6 | 0xe0040fd8 |
| TPIU_PID7 | TPIU Peripheral Identification Register 7 | 0xe0040fdc |
| TPIU_PID0 | TPIU Peripheral Identification Register 0 | 0xe0040fe0 |
| TPIU_PID1 | TPIU Peripheral Identification Register 1 | 0xe0040fe4 |
| TPIU_PID2 | TPIU Peripheral Identification Register 2 | 0xe0040fe8 |
| TPIU_PID3 | TPIU Peripheral Identification Register 3 | 0xe0040fec |
| TPIU_CID0 | TPIU Component Identification Register 0 | 0xe0040ff0 |
| TPIU_CID1 | TPIU Component Identification Register 1 | 0xe0040ff4 |
| TPIU_CID2 | TPIU Component Identification Register 2 | 0xe0040ff8 |
| TPIU_CID3 | TPIU Component Identification Register 3 | 0xe0040ffc |
| ETM_CTL | ETM Control register | 0xe0041000 |
| ETM_CFG_CODE | ETM Configuration code register | 0xe0041004 |
| ETM_TRIG_EVENT | Trigger Event Register | 0xe0041008 |
| ETM_STATUS | ETM Status Register | 0xe0041010 |
| ETM_SYS_CFG | System Configuration Register | 0xe0041014 |
| ETM_TRACE_ENB_EVENT | Trace Enable Event Register | 0xe0041020 |
| ETM_TRACE_EN_CTRL1 | TraceEnable Control 1 Register | 0xe0041024 |
| ETM_FIFOFULL_LEVEL | FIFOFULL Level Register | 0xe004102c |
| ETM_SYNC_FREQ | Synchronization Frequency Register | 0xe00411e0 |
| ETM_ETM_ID | ETM ID Register | 0xe00411e4 |
| ETM_CFG_CODE_EXT | Configuration Code Extension Register | 0xe00411e8 |
| ETM_TR_SS_EMBICE_CTRL | Trace Start/Stop EmbeddedICE Control Register | 0xe00411f0 |
| ETM_CS_TRACE_ID | CoreSight Trace ID Register | 0xe0041200 |
| ETM_OS_LOCK_ACCESS | OS Lock Access Register | 0xe0041300 |
| ETM_OS_LOCK_STATUS | OS Lock Status Register | 0xe0041304 |
| ETM_PDSR | Device Power-Down Status Register | 0xe0041314 |
| ETM_ITMISCIN | Integration Test Miscellaneous Inputs | 0xe0041ee0 |
| ETM_ITTRIGOUT | Integration Test Trigger Out | 0xe0041ee8 |
| ETM_ITATBCTR2 | ETM Integration Test ATB Control 2 | 0xe0041ef0 |
| ETM_ITATBCTR0 | ETM Integration Test ATB Control 0 | 0xe0041ef8 |
| ETM_INT_MODE_CTRL | Integration Mode Control Register | 0xe0041f00 |
| ETM_CLM_TAG_SET | Claim Tag Set Register | 0xe0041fa0 |
| ETM_CLM_TAG_CLR | Claim Tag Clear Register | 0xe0041fa4 |
| ETM_LOCK_ACCESS | Lock Access Register | 0xe0041fb0 |
| ETM_LOCK_STATUS | Lock Status Register | 0xe0041fb4 |
| ETM_AUTH_STATUS | Authentication Status Register | 0xe0041fb8 |
| ETM_DEV_TYPE | Device Type Register | 0xe0041fcc |
| ETM_PID4 | ETM Peripheral Identification Register 4 | 0xe0041fd0 |
| ETM_PID5 | ETM Peripheral Identification Register 5 | 0xe0041fd4 |
| ETM_PID6 | ETM Peripheral Identification Register 6 | 0xe0041fd8 |

| Register Name | Purpose | Address |
|-------------------|--|------------|
| ETM_PID7 | ETM Peripheral Identification Register 7 | 0xe0041fdc |
| ETM_PID0 | ETM Peripheral Identification Register 0 | 0xe0041fe0 |
| ETM_PID1 | ETM Peripheral Identification Register 1 | 0xe0041fe4 |
| ETM_PID2 | ETM Peripheral Identification Register 2 | 0xe0041fe8 |
| ETM_PID3 | ETM Peripheral Identification Register 3 | 0xe0041fec |
| ETM_CID0 | ETM Component Identification Register 0 | 0xe0041ff0 |
| ETM_CID1 | ETM Component Identification Register 1 | 0xe0041ff4 |
| ETM_CID2 | ETM Component Identification Register 2 | 0xe0041ff8 |
| ETM_CID3 | ETM Component Identification Register 3 | 0xe0041ffc |
| ROM_TABLE_NVIC | NVIC | 0xe00ff000 |
| ROM_TABLE_DWT | DWT | 0xe00ff004 |
| ROM_TABLE_FPB | FPB | 0xe00ff008 |
| ROM_TABLE_ITM | ITM | 0xe00ff00c |
| ROM_TABLE_TPIU | TPIU | 0xe00ff010 |
| ROM_TABLE_ETM | ETM | 0xe00ff014 |
| ROM_TABLE_END | END | 0xe00ff018 |
| ROM_TABLE_MEMTYPE | MEMTYPE | 0xe00ff0cc |
| ROM_TABLE_PID4 | ROM Table Peripheral Identification Register 4 | 0xe00ffd0 |
| ROM_TABLE_PID5 | ROM Table Peripheral Identification Register 5 | 0xe00ffd4 |
| ROM_TABLE_PID6 | ROM Table Peripheral Identification Register 6 | 0xe00ffd8 |
| ROM_TABLE_PID7 | ROM Table Peripheral Identification Register 7 | 0xe00ffdc |
| ROM_TABLE_PID0 | ROM Table Peripheral Identification Register 0 | 0xe00ffe0 |
| ROM_TABLE_PID1 | ROM Table Peripheral Identification Register 1 | 0xe00ffe4 |
| ROM_TABLE_PID2 | ROM Table Peripheral Identification Register 2 | 0xe00ffe8 |
| ROM_TABLE_PID3 | ROM Table Peripheral Identification Register 3 | 0xe00ffec |
| ROM_TABLE_CID0 | ROM Table Component Identification Register 0 | 0xe00fff0 |
| ROM_TABLE_CID1 | ROM Table Component Identification Register 1 | 0xe00fff4 |
| ROM_TABLE_CID2 | ROM Table Component Identification Register 2 | 0xe00fff8 |
| ROM_TABLE_CID3 | ROM Table Component Identification Register 3 | 0xe00fffc |

1.3.1 FLASH_DATA[0..262143]

DATA

Reset: N/A

Register : Address

FLASH_DATA: 0x0-0x3FFFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|------------------|
| 7:0 | data[7:0] | (no description) |

1.3.2 SRAM_CODE64K[0..16383]

Code System Memory Bank

Reset: N/A

Register : Address

SRAM_CODE64K: 0x1FFF8000-0x1FFFBFFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DMAdata_CPUcode_sram | | | | | | | |

Code Storage SRAM The CODE segment is available in all SRAM variants of PSoC5. CPU code space mapped at 1FFF8000 -- 1FFFFFFF. Same physical space logically mapped at 20008000 -- 2000FFFF for DMA access. The other CODExxK segments are only available on PSoC5 variants with that much SRAM or larger. The Interrupt Vector Table, Interrupt Service Routines and other speed critical software should be located in this segment of RAM. Data variables can be placed here but performance will be sub-optimal due to the access conflict with fetching instructions on the C bus. The RAM is physically 32-bits wide and is byte addressable. The RAM is zero wait-states for code fetches but data fetches will be slower due to the conflict on the C bus.

| Bits | Name | Description |
|------|----------------------------|------------------|
| 7:0 | DMAdata_CPUcode_sram [7:0] | (no description) |

1.3.3 SRAM_CODE32K[0..8191]

Code System Memory Bank

Reset: N/A

Register : Address

SRAM_CODE32K: 0x1FFFC000-0x1FFDFFFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DMAdata_CPUcode_sram | | | | | | | |

Code Storage SRAM The CODE segment is available in all SRAM variants of PSoC5. CPU code space mapped at 1FFF8000 -- 1FFFFFFF Same physical space logically mapped at 20008000 -- 2000FFFF for DMA access The other CODExxK segments are only available on PSoC5 variants with that much SRAM or larger. The Interrupt Vector Table, Interrupt Service Routines and other speed critical software should be located in this segment of RAM. Data variables can be placed here but performance will be sub-optimal due to the access conflict with fetching instructions on the C bus. The RAM is physically 32-bits wide and is byte addressable. The RAM is zero wait-states for code fetches but data fetches will be slower due to the conflict on the C bus.

| Bits | Name | Description |
|------|-------------------------------|------------------|
| 7:0 | DMAdata_CPUcode_sram [7:0] | (no description) |

1.3.4 SRAM_CODE16K[0..4095]

Code System Memory Bank

Reset: N/A

Register : Address

SRAM_CODE16K: 0x1FFFE000-0x1FFFEFFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DMAdata_CPUcode_sram | | | | | | | |

Code Storage SRAM The CODE segment is available in all SRAM variants of PSoC5. CPU code space mapped at 1FFF8000 -- 1FFFFFFF. Same physical space logically mapped at 20008000 -- 2000FFFF for DMA access. The other CODExxK segments are only available on PSoC5 variants with that much SRAM or larger. The Interrupt Vector Table, Interrupt Service Routines and other speed critical software should be located in this segment of RAM. Data variables can be placed here but performance will be sub-optimal due to the access conflict with fetching instructions on the C bus. The RAM is physically 32-bits wide and is byte addressable. The RAM is zero wait-states for code fetches but data fetches will be slower due to the conflict on the C bus.

| Bits | Name | Description |
|------|----------------------------|------------------|
| 7:0 | DMAdata_CPUcode_sram [7:0] | (no description) |

1.3.5 SRAM_CODE[0..4095]

Code System Memory Bank

Reset: N/A

Register : Address

SRAM_CODE: 0x1FFFF000-0x1FFFFFFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DMAdata_CPUcode_sram | | | | | | | |

Code Storage SRAM The CODE segment is available in all SRAM variants of PSoC5. CPU code space mapped at 1FFF8000 -- 1FFFFFFF Same physical space logically mapped at 20008000 -- 2000FFFF for DMA access The other CODExxK segments are only available on PSoC5 variants with that much SRAM or larger. The Interrupt Vector Table, Interrupt Service Routines and other speed critical software should be located in this segment of RAM. Data variables can be placed here but performance will be sub-optimal due to the access conflict with fetching instructions on the C bus. The RAM is physically 32-bits wide and is byte addressable. The RAM is zero wait-states for code fetches but data fetches will be slower due to the conflict on the C bus.

| Bits | Name | Description |
|------|-------------------------------|------------------|
| 7:0 | DMAdata_CPUcode_sram [7:0] | (no description) |

1.3.6 SRAM_DATA[0..4095]

Data System Memory Bank

Reset: N/A

Register : Address

SRAM_DATA: 0x20000000-0x20000FFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CPU_DMA_data_sram | | | | | | | |

Data Storage SRAM, space is accessible by CPU and DMA The DATA segment is available in all SRAM variants of PSoC5. The other DATAxxK segments are only available on PSoC5 variants with that much SRAM or larger. The Stack pointer is normally located at the top of DATA SRAM and grows downward. All data should be placed in this segment of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the S bus. There is also a 1 clock wait state for all code fetches across the S bus. The RAM is physically 32-bits wide and is byte addressable.

| Bits | Name | Description |
|------|----------------------------|------------------|
| 7:0 | CPU_DMA_data_sram[7:0] | (no description) |

1.3.7 SRAM_DATA16K[0..4095]

Data System Memory Bank

Reset: N/A

Register : Address

SRAM_DATA16K: 0x20001000-0x20001FFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CPU_DMA_data_sram | | | | | | | |

Data Storage SRAM, space is accessible by CPU and DMA The DATA segment is available in all SRAM variants of PSoC5. The other DATAxK segments are only available on PSoC5 variants with that much SRAM or larger. The Stack pointer is normally located at the top of DATA SRAM and grows downward. All data should be placed in this segment of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the S bus. There is also a 1 clock wait state for all code fetches across the S bus. The RAM is physically 32-bits wide and is byte addressable.

| Bits | Name | Description |
|------|----------------------------|------------------|
| 7:0 | CPU_DMA_data_sram[7:0] | (no description) |

1.3.8 SRAM_DATA32K[0..8191]

Data System Memory Bank

Reset: N/A

Register : Address

SRAM_DATA32K: 0x20002000-0x20003FFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CPU_DMA_data_sram | | | | | | | |

Data Storage SRAM, space is accessible by CPU and DMA The DATA segment is available in all SRAM variants of PSoC5. The other DATAxxK segments are only available on PSoC5 variants with that much SRAM or larger. The Stack pointer is normally located at the top of DATA SRAM and grows downward. All data should be placed in this segment of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the S bus. There is also a 1 clock wait state for all code fetches across the S bus. The RAM is physically 32-bits wide and is byte addressable.

| Bits | Name | Description |
|------|----------------------------|------------------|
| 7:0 | CPU_DMA_data_sram[7:0] | (no description) |

1.3.9 SRAM_DATA64K[0..16383]

Data System Memory Bank

Reset: N/A

Register : Address

SRAM_DATA64K: 0x20004000-0x20007FFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CPU_DMA_data_sram | | | | | | | |

Data Storage SRAM, space is accessible by CPU and DMA The DATA segment is available in all SRAM variants of PSoC5. The other DATAxxK segments are only available on PSoC5 variants with that much SRAM or larger. The Stack pointer is normally located at the top of DATA SRAM and grows downward. All data should be placed in this segment of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the S bus. There is also a 1 clock wait state for all code fetches across the S bus. The RAM is physically 32-bits wide and is byte addressable.

| Bits | Name | Description |
|------|----------------------------|------------------|
| 7:0 | CPU_DMA_data_sram[7:0] | (no description) |

1.3.10 DMA_SRAM64K[0..16383]

Data System Memory Bank

Reset: N/A

Register : Address

DMA_SRAM64K: 0x20008000-0x2000BFFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DMA_data_sram | | | | | | | |

Data Storage SRAM, physically same as CODE space. This address space is logically mapped with different address, accessible by DMA. CPU code space mapped at 1FFF8000 -- 1FFFFFFF. Same physical space logically mapped at 20008000 -- 2000FFFF for DMA access. The other RAMxxK/CODExxK segments are only available on PSoC5 variants with that much SRAM or larger. All code may be placed in this segment of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the C bus. The RAM is physically 32-bits wide and is byte addressable.

| Bits | Name | Description |
|------|--------------------|------------------|
| 7:0 | DMA_data_sram[7:0] | (no description) |

1.3.11 DMA_SRAM32K[0..8191]

Data System Memory Bank

Reset: N/A

Register : Address

DMA_SRAM32K: 0x2000C000-0x2000DFFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DMA_data_sram | | | | | | | |

Data Storage SRAM, physically same as CODE space. This address space is logically mapped with different address, accessible by DMA. CPU code space mapped at 1FFF8000 -- 1FFFFFFF. Same physical space logically mapped at 20008000 -- 2000FFFF for DMA access. The other RAMxxK/CODExxK segments are only available on PSoC5 variants with that much SRAM or larger. All code may be placed in this segment of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the C bus. The RAM is physically 32-bits wide and is byte addressable.

| Bits | Name | Description |
|------|--------------------|------------------|
| 7:0 | DMA_data_sram[7:0] | (no description) |

@0x2000e000 + [0..4095 * 0x1]

1.3.12 DMA_SRAM16K[0..4095]

Data System Memory Bank

Reset: N/A

Register : Address

DMA_SRAM16K: 0x2000E000-0x2000EFFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DMA_data_sram | | | | | | | |

Data Storage SRAM, physically same as CODE space. This address space is logically mapped with different address, accessible by DMA. CPU code space mapped at 1FFF8000 -- 1FFFFFFF. Same physical space logically mapped at 20008000 -- 2000FFFF for DMA access. The other RAMxxK/CODExxK segments are only available on PSoC5 variants with that much SRAM or larger. All code may be placed in this segment of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the C bus. The RAM is physically 32-bits wide and is byte addressable.

| Bits | Name | Description |
|------|--------------------|------------------|
| 7:0 | DMA_data_sram[7:0] | (no description) |

1.3.13 DMA_SRAM[0..4095]

Data System Memory Bank

Reset: N/A

Register : Address

DMA_SRAM: 0x2000F000-0x2000FFFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DMA_data_sram | | | | | | | |

Data Storage SRAM, physically same as CODE space. This address space is logically mapped with different address, accessible by DMA. CPU code space mapped at 1FFF8000 -- 1FFFFFFF. Same physical space logically mapped at 20008000 -- 2000FFFF for DMA access. The other RAMxxK/CODExxK segments are only available on PSoC5 variants with that much SRAM or larger. All code may be placed in this segment of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the C bus. The RAM is physically 32-bits wide and is byte addressable.

| Bits | Name | Description |
|------|--------------------|------------------|
| 7:0 | DMA_data_sram[7:0] | (no description) |

1.3.14 CLKDIST_CR

Configuration Register CR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_CR: 0x40004000

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------|---------|---|---------|---|---------|---|
| SW Access:Reset | NA:0 | R/W:0 | R/W:00 | | R/W:00 | | R/W:00 | |
| HW Access | NA | R | R | | R | | R | |
| Name | | IMO2X_SRC | IMO_OUT | | ILO_OUT | | PLL_SRC | |

This register is used to configure the 4 main CLK sources. PLL_SRC - The source to the PLL reference clock input. ILO_OUT - ILO source to the clock distribution block. IMO_OUT - The source from IMO to clock distribution block. IMO2X_SRC - Source to IMO doubler. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

| Bits | Name | Description |
|------|--------------|---|
| 6 | IMO2X_SRC | Selects the external clock input source to Internal Oscillator. This bit controls a 2:1 mux that drives the external clock input to the s8intosc oscillator. The oscillator itself contains another mux allowing control if the external clock or the oscillator itself is the source clock to the system clock called IMO and to the IMO frequency doubling circuit. The clock selection in the oscillator is controlled by FASTCLK_IMO_CR.XCLKEN. Because this bit can induce clock glitches, it should only be changed when no downstream clock tree is configured to use the IMO clock source, or FASTCLK_IMO_CR.XCLKEN is low at the time it is changed. See Table 1-2. |
| 5:4 | IMO_OUT[1:0] | Select the IMO output source to clock distribution. This clock configuration feature is primarily intended for internal use only. Changing this field can cause clock glitches. This needs either to be expected or avoided. To avoid glitches all downstream clock trees will need to be configured to a different clock source when this field is written. See Table 1-3. |
| 3:2 | ILO_OUT[1:0] | Select the ILO output source to clock distribution. Any clock tree using this clock as its source must be disabled before writing this register bit to avoid potential glitches. See Table 1-1. |
| 1:0 | PLL_SRC[1:0] | Select the PLL reference clock input. Do not change the value in this field while the PLL is the currently selected clock source for the Master Mux or USB clock (if enabled) See Table 1-4. |

Table 1-1. Bit field encoding: ILO_OUTPUT_SEL_ENUM

| Value | Name | Description |
|-------|---------|---------------------------|
| 2'h0 | ILO100K | 100KHz output is selected |
| 2'h1 | ILO33K | 33KHz output is selected |
| 2'h2 | ILO1K | 1KHz output is selected |
| 2'h3 | RSVD | Reserved |

Table 1-2. Bit field encoding: IMO2X_INPUT_SEL_ENUM

| Value | Name | Description |
|-------|------|--|
| 1'b0 | DSI | Digital System Interconnect is used as a source to IMO doubler |

1.3.14 CLKDIST_CR (continued)

Table 1-2. Bit field encoding: IMO2X_INPUT_SEL_ENUM

| | | |
|------|------|--|
| 1'b1 | XTAL | External clock source is used as a source to IMO doubler |
|------|------|--|

Table 1-3. Bit field encoding: IMO_OUTPUT_SEL_ENUM

| Value | Name | Description |
|-------|-------|--------------------------------|
| 2'h0 | IMO | IMO is selected |
| 2'h1 | IMO2X | IMO Doubler output is selected |
| 2'h2 | IMO36 | IMO 36MHz output is selected |
| 2'h3 | RSVD | Reserved |

Table 1-4. Bit field encoding: PLL_INPUT_SEL_ENUM

| Value | Name | Description |
|-------|------|---|
| 2'h0 | IMO | IMO is selected |
| 2'h1 | XTAL | 33MHz XTAL is selected |
| 2'h2 | DSI | Digital System Interconnect is selected |
| 2'h3 | RSVD | Reserved |

1.3.15 CLKDIST_LD

LOAD Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_LD: 0x40004001

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|---------|-------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R/W | R/W | R/W |
| Name | | | | | | DISABLE | SYNC_EN | LOAD |

This register provides control of clock parameters while the clocks are running and does so without compromising the integrity of the clocks (glitch-free). In groups defined by the DMASK and AMASK registers, clocks can be loaded with new count values or loaded with new divide counts and started aligned together using this feature. Setting the LOAD bit immediately copies the values of the WRK0 and WRK1 registers into all divider divide registers (DCFG0/1 and ACFG0/1, BCFG0/1), which are not masked off. Setting the SYNC_EN bit forces a load and restart of all the dividers which are not masked off (excluding BUS_CLK). Using SYNC_EN restarts all affected dividers phase aligned. In order for the dividers to start phase aligned all the divide values must be integer multiples of one another. Upon setting the DISABLE register bit all dividers which are not masked off are disabled (Excluding BUS_CLK). This allows for local control of the clock trees. The SYNC_EN and LOAD bits, bits 1 and 0 respectively, in this register are cleared upon completion of loading and/or restarting. When changing configuration of any of the ACLK/DCLKs a value of 0x00 needs to be written to both WRK0 and WRK1 registers. Next a value of 0x07 has to be written to this register, LD. One has to poll this register, LD, for bits 1 and 0 (SYNC_EN and LOAD) to be cleared in order to start modifying clock tree configuration. This applies to all ACLK/DCLK configuration bits. The WRK0/1 and DMASK/AMASK register can be written in any order but both must be written before LOAD or SYNC_EN are written. The DMASK/AMASK register must be written before the DISABLE bit is written.

| Bits | Name | Description |
|------|---------|---|
| 2 | DISABLE | Locally disable all unmasked divders (Excluding BUS_CLK). See Table 1-5. |
| 1 | SYNC_EN | Load all unmasked dividers with a common shadow divider value and restart all unmasked dividers in phase. See Table 1-7. |
| 0 | LOAD | Load all unmasked dividers with a common shadow divider value. (does not restart them in phase) See Table 1-6. |

Table 1-5. Bit field encoding: DISABLE_ENUM

| Value | Name | Description |
|-------|-----------|-------------|
| 1'b0 | DISABLE_0 | Enable |
| 1'b1 | DISABLE_1 | Disable |

Table 1-6. Bit field encoding: LOAD_ENUM

| Value | Name | Description |
|-------|--------|--|
| 1'b0 | LOAD_0 | Do nothing |
| 1'b1 | LOAD_1 | Copy shadow value defined in CLKDIST_WRK0 and CLKDIST_WRK1 registers to all dividers selected in CLKDIST_MSK0 and CLKDIST_MSK1 registers |

1.3.15 CLKDIST_LD (continued)

Table 1-7. Bit field encoding: SYNC_SHADOW_ENUM

| Value | Name | Description |
|-------|--------|---|
| 1'b0 | SYNC_0 | Do nothing |
| 1'b1 | SYNC_1 | Enable all dividers selected in CLKDIST_MSK register (Excluding BUS_CLK) to start (or restart) in phase. NOTE: does not load the WRK register values. This bit only phase aligns all the selected dividers with their existing divide values. |

1.3.16 CLKDIST_WRK0

LSB Shadow Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_WRK0: 0x40004002

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DIV_VAL | | | | | | | |

This register is the low byte of a count value to be loaded in specified clock dividers defined by the A/DMASK registers. This register (with WRK1) holds a new count value to be atomically loaded, so that the 16 bits dividers can safely be updated dynamically. For information on how this feature is used, see the description in the LD register.

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | DIV_VAL[7:0] | Encoding including WRK1: 0x0000 source 0x0001 source / 2 0x0002 source / 3 0xfffe source / 65535 0xffff source / 65536 |

1.3.17 CLKDIST_WRK1

MSB Shadow Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_WRK1: 0x40004003

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DIV_VAL | | | | | | | |

This register is the high byte of a count value to be loaded in specified clock dividers defined by the A/DMASK registers. This register (with WRK0) holds a new count value to be atomically loaded, so that the 16 bits dividers can safely be updated dynamically. For information on how this feature is used, see the description in the LD register.

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | DIV_VAL[7:0] | Encoding including WRK0: 0x0000 source 0x0001 source / 2 0x0002 source / 3 0xfffe source / 65535 0xffff source / 65536 |

1.3.18 CLKDIST_MSTR0

Master clock (clk_sync_d) Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_MSTR0: 0x40004004

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DIV_VAL | | | | | | | |

This register holds the master source clock 8-bit divide value. This register can be written at any time, including while the divider is running. Due to a sampling anomaly in the HW, there is a small probability that the Master divider will divide by an incorrect value (not the past or new value) for one period before stabilizing on the divide value written.

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | DIV_VAL[7:0] | 0x00 source 0x01 source / 2 0x02 source / 3 0xfe source / 255 0xff source / 256 |

1.3.19 CLKDIST_MSTR1

Master (clk_sync_d) Configuration Register/CPU Divider Value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CLKDIST_MSTR1: 0x40004005

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|---------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | SRC_SEL | |

This register holds the master clock source configuration. The register can be altered at any time without compromising clock integrity.

| Bits | Name | Description |
|------|--------------|--------------------------------|
| 1:0 | SRC_SEL[1:0] | Master clock source selection. |

[See Table 1-8.](#)

Table 1-8. Bit field encoding: MASTER_SRC_SEL_ENUM

| Value | Name | Description |
|-------|------|-----------------------------|
| 2'h0 | IMO | imo output is selected |
| 2'h1 | PLL | pll output is selected |
| 2'h2 | XTAL | xtal_mhz output is selected |
| 2'h3 | DSI | dsi_c output is selected |

1.3.20 CLKDIST_BCFG0

CLK_BUS LSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_BCFG0: 0x40004006

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DIV_VAL | | | | | | | |

This register holds the LSB of the 16-bit divide value. It should only be written when the clock tree is disabled to avoid clock glitches. If the clock divider needs changed when the clock is running, this can be accomplished using the atomic load feature described in the LD register description.

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | DIV_VAL[7:0] | Encoding including BCFG1: 0x0000 source 0x0001 source / 2 0x0002 source / 3 0xfffe source / 65535 0xffff source / 65536 |

1.3.21 CLKDIST_BCFG1

CLK_BUS MSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_BCFG1: 0x40004007

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DIV_VAL | | | | | | | |

This register holds the MSB of the 16-bit divide value. It should only be written when the clock tree is disabled to avoid clock glitches. If the clock divider needs changed when the clock is running, this can be accomplished using the atomic load feature described in the LD register description.

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | DIV_VAL[7:0] | Encoding including BCFG0: 0x0000 source 0x0001 source / 2 0x0002 source / 3 0xfffe source / 65535 0xffff source / 65536 |

1.3.22 CLKDIST_BCFG2

CLK_BUS Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_BCFG2: 0x40004008

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|--------|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:000 | | |
| HW Access | R | R | R | R | R | NA | | |
| Name | MASK | SSS | EARLY | DUTY | SYNC | | | |

This register holds the configuraton values for the Bus Clock. The EARLY bit should never be used and should never be set HIGH. The DUTY bit should never be written when the divider is in use to avoid clock glitches. The SSS and SYNC_EN bits can only be safely written when clk_sync (output of MasterMux) is running at 12MHz or lower and a duty-cycle between 30/70 and 50/50 to avoid clock glitches. The MASK bit is used for inclusion/exclusion from atomic load operations. See the description of this feature in the LD register description. SSS takes presedence over SYNC_EN. Do not set SYNC_EN high when divider is dividing by 1, this halts BUSCLK and is unrecoverable. BUSCLK is phase-aligned (balanced) with the ACLKs/ DCLKs only when SSS or SYNC_EN is set HIGH.

| Bits | Name | Description |
|------|-------|---|
| 7 | MASK | Mask bits to enable shadow loads--0 disable, 1 enable. See LD register description. |
| 6 | SSS | Sync source same as output frequency. Used to bypass synchronization with delay matched path. Set this bit high when not dividing and balanced system clocks are desired. Only change when clk_sync is below 12MHz to avoid clock glitches. See Table 1-11. |
| 5 | EARLY | RESERVED - Do not set HIGH in any application. See Table 1-10. |
| 4 | DUTY | Force duty cycle to 50%. Only change this bit when divider is not in use to avoid clock glitches. See Table 1-9. |
| 3 | SYNC | Select output synchronization to master clock. Use to balance system clocks only when the divider is dividing by 2 or higher. Do no set this bit when divider is set to divide by 1 - this will halt BUSCLK. To avoid clock glitches first turn on SSS bit when making changes, then turn off SSS when changes complete. (SSS takes precedence over SYNC so doing this will protect the clock from any glitches related to changing SYNC). See Table 1-12. |

Table 1-9. Bit field encoding: DUTY_ENUM

| Value | Name | Description |
|-------|---------|--------------------------------------|
| 1'b0 | DISABLE | Disable 50% duty cycle. Pulse train. |
| 1'b1 | ENABLE | Enable 50% duty cycle clock output |

Table 1-10. Bit field encoding: EARLY_ENUM

| Value | Name | Description |
|-------|---------|--------------------------|
| 1'b0 | DISABLE | Disable early phase mode |
| 1'b1 | ENABLE | Enable early phase mode |

1.3.22 CLKDIST_BCFG2 (continued)

Table 1-11. Bit field encoding: SSS_ENUM

| Value | Name | Description |
|-------|---------|--------------------------------|
| 1'b0 | DISABLE | Sync source not same frequency |
| 1'b1 | ENABLE | Sync source is same frequency |

Table 1-12. Bit field encoding: SYNC_ENUM

| Value | Name | Description |
|-------|---------|-------------------------|
| 1'b0 | DISABLE | Disable synchronization |
| 1'b1 | ENABLE | Enable synchronization |

1.3.23 CLKDIST_UCFG

USB Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_UCFG: 0x40004009

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------|-------|-------|---------|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:00 | |
| HW Access | NA | | | R | R | R | R | |
| Name | | | | TMODE | GPIPE | DIV2 | SRC_SEL | |

This register holds the USB clock configuration parameters. Only change values in this register when the USB clock is disabled to avoid clock glitches.

| Bits | Name | Description |
|------|--------------|---|
| 4 | TMODE | Enable monitoring of clk_usb through DSI routing See Table 1-16. |
| 3 | GPIPE | Global DSI input pipeline configuration See Table 1-13. |
| 2 | DIV2 | USB clock divide source by two See Table 1-14. |
| 1:0 | SRC_SEL[1:0] | USB clock source selection. See Table 1-15. |

Table 1-13. Bit field encoding: CDSI_ENUM

| Value | Name | Description |
|-------|--------|------------------------|
| 1'b0 | BYPASS | Bypass pipeline stages |
| 1'b1 | ENABLE | Use pipeline stages |

Table 1-14. Bit field encoding: DIV2_ENUM

| Value | Name | Description |
|-------|---------|-----------------------|
| 1'b0 | DISABLE | Disable divide by two |
| 1'b1 | ENABLE | Enable divide by two |

Table 1-15. Bit field encoding: SRC_SEL_ENUM

| Value | Name | Description |
|-------|-------|--------------------------------|
| 2'h0 | IMO2X | imo2x output is selected |
| 2'h1 | IMO | imo output is selected |
| 2'h2 | PLL | pll output is selected |
| 2'h3 | DSI | dsi_glb_div output is selected |

Table 1-16. Bit field encoding: TMODE_ENUM

| Value | Name | Description |
|-------|---------|------------------------------------|
| 1'b0 | DISABLE | Disable clk_usb_test output to DSI |
| 1'b1 | ENABLE | Enable clk_usb_test output to DSI |

1.3.24 CLKDIST_DLY0

Delay block Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DLY0: 0x4000400A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------|---|-----------|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:00 | | R/W:00000 | | | | |
| HW Access | NA | R | | R | | | | |
| Name | | CTRIM | | FTRIM | | | | |

This register is used to trim the delay cell tap duration. This register should only be used when the delay cell is in trim mode (see DLY1 MODE bit).

| Bits | Name | Description |
|------|------------|--|
| 6:5 | CTRIM[1:0] | Course trim bits for delay block See Table 1-17. |
| 4:0 | FTRIM[4:0] | Fine trim bits for delay block 5'b00000 Lowest bias 5'bffff Highest bias |

Table 1-17. Bit field encoding: CTRIM_ENUM

| Value | Name | Description |
|-------|-------|-----------------------------|
| 2'b00 | ZERO | Highest bias setting |
| 2'b10 | TWO | Second highest bias setting |
| 2'b01 | ONE | Third highest bias setting |
| 2'b11 | THREE | Fourth highest bias setting |

1.3.25 CLKDIST_DLY1

Delay block Configuration Register

Reset: Reset Signals Listed Below

Register : Address

CLKDIST_DLY1: 0x4000400B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|-------|-------|-------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | EN | ISEL | MODE |

This register holds the configuration control for the clock delay cell. This cell is used to program delays between the system bus clock and each of the 4 individual analog clocks (ACLK). This is used to unalign analog and digital domain clock edges to reduce noise when the analog domain clocks. Normally the 5 domains are phase aligned for applications that need clock-edge-aligned interfaces. If clock-edge-aligned interfaces aren't needed and system noise is an issue, clock tree domains can be programmably skewed away from each other.

| Bits | Name | Description |
|------|------|--|
| 2 | EN | The <code>clk_sync_d</code> reference clock is sourced by the <code>clk0</code> output of the delay cell. This output can either be sourced from a 10-tap delay element or muxed directly (bypassed) from the delay cell's clock input (<code>clk_sync</code>). When bypassed (<code>EN=0</code>), the bus clock and all 4 analog clocks (<code>clk_a[]</code>) are balanced (clock-edge-aligned) if their skew delay registers are programmed to <code>0x0001</code> . (see <code>CLKDIST_ACFGx_CFG3</code>) If <code>EN=1</code> this enables the delay element on <code>clk0</code> and allows the system to program delays on <code>clk_sync_d</code> . The delay amount is identical to the ACLK channels but is not controlled with a register, but rather with customer controlled non-volatile bits that are loaded at system POR. In this mode the <code>clk0</code> has a inherent ~4ns delay, meaning <code>BUSCLK</code> lags the 4 ACLKs by ~4ns when all tap are programmed to <code>0x0001</code> . Thus, any values programmed into the <code>PHASE_DLY</code> fields of the <code>CLKDIST_ACFGx_CFG3</code> registers will skew the clocks relative to this ~4ns skew, as will changing the <code>clk0</code> delay via <code>CNVL</code> setting. Note that it is not allowed that the system be configured such that <code>clk_sync_d</code> lag any <code>clk_a[]</code> by less than ~4ns for any values of the programmable delay values. The HW will fail in these cases and SW should avoid doing this. See <code>ACFG3</code> register description for further details. This bit is cleared on wakeup from low power modes (sleep, hibernate, hibernate timer modes), user is expected to configure this bit to the required state. User must set the register bit <code>PM_ACT_CFG0[7]</code> to generate the delayed version of the clock. |
| 1 | ISEL | Reference current selection See Table 1-18. |
| 0 | MODE | Clock mode. Used to put the delay cell in normal more or trim mode. See Table 1-19. |

Reset Table

| resetsignal | field(s) |
|---|------------|
| System reset for retention flops [reset_all_retention] | MODE, ISEL |

1.3.25 CLKDIST_DLY1 (continued)

Reset Table

```

Domain reset for non- EN
retention          flops
[reset_all_nonretention
]

```

Table 1-18. Bit field encoding: ISEL_ENUM

| Value | Name | Description |
|-------|----------|---|
| 1'b0 | BANDGAP | Use bandgap reference |
| 1'b1 | INTERNAL | Use internal reference, this selection is for engineering purposes only |

Table 1-19. Bit field encoding: MODE_ENUM

| Value | Name | Description |
|-------|-------|--|
| 1'b0 | DELAY | Puts the cell in normal clock delay mode. This is mission mode and allows for programming of delays on the clock trees. See CLKDIST_ACFGx_CFG3 |
| 1'b1 | RING | This mode is used only for trimming. While in this mode the output of a ring oscillator is monitored and tuned to 40MHz. |

1.3.26 CLKDIST_DMASK

Digital Clock Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DMASK: 0x40004010

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DMASK | | | | | | | |

Mask picking which digital clocks are enabled for shadow loads. See LD register description for usage information.

| Bits | Name | Description |
|------|------------|--|
| 7:0 | DMASK[7:0] | Mask bits to enable shadow loads -- 0 = Disabled, 1 = Enabled MSK0 = DCLK0 MSK1 = DCLM1 : MSK7 = DCLK7 |

1.3.27 CLKDIST_AMASK

Analog Clock Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_AMASK: 0x40004014

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | AMASK | | | |

Mask picking which analog clocks are enabled for shadow loads. See LD register description for usage information.

| Bits | Name | Description |
|------|------------|--|
| 3:0 | AMASK[3:0] | Mask bits to enable shadow loads -- 0 = Disabled, 1 = Enabled MSK0 = ACLK0 : MSK3 = ACLK3 |

1.3.28 CLKDIST_DCFG[0..7]_CFG0

LSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DCFG0_CFG0: 0x40004080

CLKDIST_DCFG1_CFG0: 0x40004084

CLKDIST_DCFG2_CFG0: 0x40004088

CLKDIST_DCFG3_CFG0: 0x4000408C

CLKDIST_DCFG4_CFG0: 0x40004090

CLKDIST_DCFG5_CFG0: 0x40004094

CLKDIST_DCFG6_CFG0: 0x40004098

CLKDIST_DCFG7_CFG0: 0x4000409C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DIV_VAL | | | | | | | |

This register holds the LSB of the 16-bit divide value. Change this register only when the associated clock is disabled. See LD register for details.

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | DIV_VAL[7:0] | Encoding including BCFG1: 0x0000 source 0x0001 source / 2 0x0002 source / 3 0xffff source / 65535 0xffff source / 65536 |

1.3.29 CLKDIST_DCFG[0..7]_CFG1

MSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DCFG0_CFG1: 0x40004081

CLKDIST_DCFG1_CFG1: 0x40004085

CLKDIST_DCFG2_CFG1: 0x40004089

CLKDIST_DCFG3_CFG1: 0x4000408D

CLKDIST_DCFG4_CFG1: 0x40004091

CLKDIST_DCFG5_CFG1: 0x40004095

CLKDIST_DCFG6_CFG1: 0x40004099

CLKDIST_DCFG7_CFG1: 0x4000409D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DIV_VAL | | | | | | | |

This register holds the MSB of the 16-bit divide value. Change this register only when the associated clock is disabled. See LD register for details.

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | DIV_VAL[7:0] | Encoding including BCFG0: 0x0000 source 0x0001 source / 2 0x0002 source / 3 0xfffe source / 65535 0xffff source / 65536 |

1.3.30 CLKDIST_DCFG[0..7]_CFG2 Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DCFG0_CFG2: 0x40004082

CLKDIST_DCFG1_CFG2: 0x40004086

CLKDIST_DCFG2_CFG2: 0x4000408A

CLKDIST_DCFG3_CFG2: 0x4000408E

CLKDIST_DCFG4_CFG2: 0x40004092

CLKDIST_DCFG5_CFG2: 0x40004096

CLKDIST_DCFG6_CFG2: 0x4000409A

CLKDIST_DCFG7_CFG2: 0x4000409E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|---------|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | R | R | R | R | R | R | | |
| Name | PIPE | SSS | EARLY | DUTY | SYNC | SRC_SEL | | |

This register holds the 8-bit DCLK configuraton values. Only change these values when the associated clock is disabled to avoid clock glitches (See LD register for details). Clock is phase-aligned with BUSCLK only when clk_sync_d is the source and SSS or SYNC_EN are set HIGH. SSS takes presedence over SYNC_EN. Never set SYNC_EN=1 when dividing by 1, this halts the clock.

| Bits | Name | Description |
|------|--------------|---|
| 7 | PIPE | DSI input pipeline configuration See Table 1-22. |
| 6 | SSS | Sync source same as output frequency. Used to bypass synchronization with delay matched path. See Table 1-24. |
| 5 | EARLY | This bit in the configuration register can be used to set the early phase mode, with rising edge near the half-count of the divider. See Table 1-21. |
| 4 | DUTY | Force duty cycle to 50% See Table 1-20. |
| 3 | SYNC | Select output synchronization to master clock See Table 1-25. |
| 2:0 | SRC_SEL[2:0] | Clock source selection. See Table 1-23. |

Table 1-20. Bit field encoding: DUTY_ENUM

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.30 CLKDIST_DCFG[0..7]_CFG2 (continued)

Table 1-20. Bit field encoding: DUTY_ENUM

| Value | Name | Description |
|-------|---------|------------------------------------|
| 1'b0 | DISABLE | Disable 50% duty cycle |
| 1'b1 | ENABLE | Enable 50% duty cycle clock output |

Table 1-21. Bit field encoding: EARLY_ENUM

| Value | Name | Description |
|-------|---------|--------------------------|
| 1'b0 | DISABLE | Disable early phase mode |
| 1'b1 | ENABLE | Enable early phase mode |

Table 1-22. Bit field encoding: PIPE_ENUM

| Value | Name | Description |
|-------|--------|------------------------|
| 1'b0 | BYPASS | Bypass pipeline stages |
| 1'b1 | ENABLE | Use pipeline stages |

Table 1-23. Bit field encoding: SRC_SEL_ENUM

| Value | Name | Description |
|-------|------------|----------------------------------|
| 3'h0 | clk_sync_d | clk_sync_d output is selected |
| 3'h1 | imo | imo output is selected |
| 3'h2 | xtal_mhz | xtal_mhz output is selected |
| 3'h3 | ilo | ilo output is selected |
| 3'h4 | pll | pll output is selected |
| 3'h5 | xtal_khz | xtal_khz output is selected |
| 3'h6 | dsi_g | dsi_global[0] output is selected |
| 3'h7 | dsi_d | dsi_d output is selected |

Table 1-24. Bit field encoding: SSS_ENUM

| Value | Name | Description |
|-------|---------|--------------------------------|
| 1'b0 | DISABLE | Sync source not same frequency |
| 1'b1 | ENABLE | Sync source is same frequency |

Table 1-25. Bit field encoding: SYNC_ENUM

| Value | Name | Description |
|-------|---------|-------------------------|
| 1'b0 | DISABLE | Disable synchronization |
| 1'b1 | ENABLE | Enable synchronization |

1.3.31 CLKDIST_ACFG[0..3]_CFG0

LSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG0: 0x40004100

CLKDIST_ACFG1_CFG0: 0x40004104

CLKDIST_ACFG2_CFG0: 0x40004108

CLKDIST_ACFG3_CFG0: 0x4000410C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DIV_VAL | | | | | | | |

This register holds the LSB of the 16-bit divide value. Change this register only when the associated clock is disabled. See LD register for details.

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | DIV_VAL[7:0] | Encoding including BCFG1: 0x0000 source 0x0001 source / 2 0x0002 source / 3 0xfffe source / 65535 0xffff source / 65536 |

1.3.32 CLKDIST_ACFG[0..3]_CFG1

MSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG1: 0x40004101

CLKDIST_ACFG1_CFG1: 0x40004105

CLKDIST_ACFG2_CFG1: 0x40004109

CLKDIST_ACFG3_CFG1: 0x4000410D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DIV_VAL | | | | | | | |

This register holds the MSB of the 16-bit divide value. Change this register only when the associated clock is disabled. See LD register for details.

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | DIV_VAL[7:0] | Encoding including BCFG0: 0x0000 source 0x0001 source / 2 0x0002 source / 3 0xfffe source / 65535 0xffff source / 65536 |

1.3.33 CLKDIST_ACFG[0..3]_CFG2 Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG2: 0x40004102

CLKDIST_ACFG1_CFG2: 0x40004106

CLKDIST_ACFG2_CFG2: 0x4000410A

CLKDIST_ACFG3_CFG2: 0x4000410E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|---------|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | R | R | R | R | R | R | | |
| Name | PIPE | SSS | EARLY | DUTY | SYNC | SRC_SEL | | |

This register holds the 8-bit ACLK configuraton values. Only change these values when the associated clock is disabled to avoid clock glitches (See LD register for details). Clock is phase-aligned with BUSCLK only when clk_sync_a/d is the source and SSS or SYNC_EN are set HIGH. SSS takes presedence over SYNC_EN. Never set SYNC_EN=1 when dividing by 1, this halts the clock.

| Bits | Name | Description |
|------|--------------|---|
| 7 | PIPE | DSI input pipeline configuration See Table 1-28. |
| 6 | SSS | Sync source same as output frequency. Used to bypass synchronization with delay matched path. See Table 1-30. |
| 5 | EARLY | This bit in the configuration register can be used to set the early phase mode, with rising edge near the half-count of the divider. See Table 1-27. |
| 4 | DUTY | Force duty cycle to 50% See Table 1-26. |
| 3 | SYNC | Select output synchronization to master clock See Table 1-31. |
| 2:0 | SRC_SEL[2:0] | Clock source selection. See Table 1-29. |

Table 1-26. Bit field encoding: DUTY_ENUM

| Value | Name | Description |
|-------|---------|------------------------------------|
| 1'b0 | DISABLE | Disable 50% duty cycle |
| 1'b1 | ENABLE | Enable 50% duty cycle clock output |

Table 1-27. Bit field encoding: EARLY_ENUM

| Value | Name | Description |
|-------|---------|--------------------------|
| 1'b0 | DISABLE | Disable early phase mode |

1.3.33 CLKDIST_ACFG[0..3]_CFG2 (continued)

Table 1-27. Bit field encoding: EARLY_ENUM

| | | |
|------|--------|-------------------------|
| 1'b1 | ENABLE | Enable early phase mode |
|------|--------|-------------------------|

Table 1-28. Bit field encoding: PIPE_ENUM

| Value | Name | Description |
|-------|--------|------------------------|
| 1'b0 | BYPASS | Bypass pipeline stages |
| 1'b1 | ENABLE | Use pipeline stages |

Table 1-29. Bit field encoding: SRC_SEL_ENUM

| Value | Name | Description |
|-------|------------|----------------------------------|
| 3'h0 | clk_sync_a | clk_sync_a output is selected |
| 3'h1 | imo | imo output is selected |
| 3'h2 | xtal_mhz | xtal_mhz output is selected |
| 3'h3 | ilo | ilo output is selected |
| 3'h4 | pll | pll output is selected |
| 3'h5 | xtal_khz | xtal_khz output is selected |
| 3'h6 | dsi_g | dsi_global[0] output is selected |
| 3'h7 | dsi_a | dsi_a output is selected |

Table 1-30. Bit field encoding: SSS_ENUM

| Value | Name | Description |
|-------|---------|--------------------------------|
| 1'b0 | DISABLE | Sync source not same frequency |
| 1'b1 | ENABLE | Sync source is same frequency |

Table 1-31. Bit field encoding: SYNC_ENUM

| Value | Name | Description |
|-------|---------|-------------------------|
| 1'b0 | DISABLE | Disable synchronization |
| 1'b1 | ENABLE | Enable synchronization |

1.3.34 CLKDIST_ACFG[0..3]_CFG3

Analog clocks Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG3: 0x40004103

CLKDIST_ACFG1_CFG3: 0x40004107

CLKDIST_ACFG2_CFG3: 0x4000410B

CLKDIST_ACFG3_CFG3: 0x4000410F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | PHASE_DLY | | | |

This register holds the analog clocks delay configuration. This register should not be written when the associated clock tree is enabled to avoid clock glitches. See DLY1 for more information how to use this register. Note that due to a clock balancing problem in the HW that some delay values can produce jitter in the ACLKs. For details see TFC-358.

| Bits | Name | Description |
|------|----------------|--|
| 3:0 | PHASE_DLY[3:0] | Phase delay selection (1.0ns increments): 0x00 Clock Disabled 0x01 0 ns delay 0x02 1 ns delay ... 0x0a 9 ns delay 0x0b 10 ns delay 0x0c Clock Disabled 0x0d Clock Disabled 0x0e Clock Disabled 0x0f Clock Disabled |

1.3.35 FASTCLK_IMO_CR

Internal Main Oscillator Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_IMO_CR: 0x40004200

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------------|-----------|--------|-------|------------------|---------|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | R | R | R | R | R | R | | |
| Name | sel_fast_bia s | usbclk_on | xclken | f2xon | en_fast_bia s | f_range | | |

This register controls operation of the IMO.

Register Segment: 1

| Bits | Name | Description |
|------|---------------|--|
| 7 | sel_fast_bias | Select IMO reference source, possible frequency selections are 12,24 and 48MHz See Table 1-35. |
| 6 | usbclk_on | Configures IMO for higher precision for when the internal USB clock-locking function is being used. See Table 1-36. |
| 5 | xclken | External clock enable for the IMO and the IMO doubler. This bit selects if the Internal Oscillator or an external clock is the source of IMO and the input to the IMO Doubler. There are two choices for the external clock source, dsi and XTAL (see CLKDIST.CR.IMO2X_SRC). See Table 1-37. |
| 4 | f2xon | IMO Doubler enable See Table 1-33. |
| 3 | en_fast_bias | Enables fast wake bias circuitry. This must be set before selecting the fast wake bias as the IMO reference using sel_fast_bias. See Table 1-32. |
| 2:0 | f_range[2:0] | Frequency range setting for the IMO. Note that if sel_fast_bias and en_fast_bias are set OR the device is in boot OR wake from sleep/hibernate/hibernate-timer modes IMO will be forced to FIMO mode. During boot, device wakeup from sleep/hibernate/hibernate-timers mode frequency setting is overridden by the value in PWRSYS_WAKE_TR1.wake_imofreq. During other times if sel_fast_bias and en_fast_bias are set then IMO frequency setting is controlled by f_range configuration bits only. See PWRSYS_WAKE_TR1 for FIMO frequency table. See Table 1-34. |

Table 1-32. Bit field encoding: EN_FAST_BIAS

| Value | Name | Description |
|-------|--------------------------|--------------------------------|
| 1'b0 | EN_FAST_BIAS_DISAB LE | Disable fast wake bias circuit |

1.3.35 FASTCLK_IMO_CR (continued)

Table 1-32. Bit field encoding: EN_FAST_BIAS

| | | |
|------|--------------------|-------------------------------|
| 1'b1 | EN_FAST_BIAS_ENABL | Enable fast wake bias circuit |
| | E | |

Table 1-33. Bit field encoding: F2XON_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | F2XON_0 | Doubler disabled (IMOCLK2X = 0) |
| 1'b1 | F2XON_1 | Doubler enabled. Note: input freq range limited to 24 MHz max. |

Table 1-34. Bit field encoding: F_RANGE_ENUM

| Value | Name | Description |
|-------|-----------|---|
| 3'h0 | F_RANGE_0 | 12 MHz (normal) |
| 3'h1 | F_RANGE_1 | 6 MHz (12MHz if sel_fast_bias=1) |
| 3'h2 | F_RANGE_2 | 24 MHz |
| 3'h3 | F_RANGE_3 | 3 MHz (RESERVED in FIMO mode) |
| 3'h4 | F_RANGE_4 | 48 MHz |
| 3'h5 | F_RANGE_5 | 62 MHz center, 67 MHz peak (48MHz if sel_fast_bias=1) |
| 3'h6 | F_RANGE_6 | 72 MHz center, 80 Mhz peak (48MHz if sel_fast_bias=1) |
| 3'h7 | F_RANGE_7 | Reserved (48MHz if sel_fast_bias=1) |

Table 1-35. Bit field encoding: SEL_FAST_BIAS_ENUM

| Value | Name | Description |
|-------|--------------------|--|
| 1'b0 | SEL_FAST_BIAS_NOR | Select LVBG as IMO reference |
| | MAL | |
| 1'b1 | SEL_FAST_BIAS_FAST | Select fast wake bias as IMO reference |

Table 1-36. Bit field encoding: USBCLK_ON_ENUM

| Value | Name | Description |
|-------|-------------|---|
| 1'b0 | USBCLK_ON_0 | Normally used for non-USB modes, for lower IMO power |
| 1'b1 | USBCLK_ON_1 | USB clock-locking used; IMO runs at higher power for highest USB clock precision. |

Table 1-37. Bit field encoding: XCLKEN_ENUM

| Value | Name | Description |
|-------|----------|--|
| 1'b0 | XCLKEN_0 | IMO doubler runs from the IMOCLK |
| 1'b1 | XCLKEN_1 | IMO doubler runs from the selected 'external' clock. |

1.3.36 FASTCLK_XMHZ_CSR

External 4-25 MHz Crystal Oscillator Status and Control Register

Reset: Reset Signals Listed Below

Register : Address

FASTCLK_XMHZ_CSR: 0x40004210

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------|------|--------|-----------|---------|---------|-------|
| SW Access:Reset | RC:0 | R/W:0 | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | W | R | NA | R | R | R | R | R |
| Name | xerr | xprot | | xstart | xpump_dis | xfb_dis | xto_dis | en |

This register is used to enable and configure modes of the XMHZ oscillator, and to read error status. In the table above, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Register Segment: 1

| Bits | Name | Description |
|------|-----------|---|
| 7 | xerr | High output indicates oscillator failure. Only use this after start-up interval is completed. This can be used for status and failure recovery. |
| 6 | xprot | Enable External Crystal Oscillator (XMHZ) fault recovery circuitry See Table 1-40. |
| 4 | xstart | This INTERNAL bit selects the start-up mode for the oscillator. By default, the output is pulsed to initiate start-up. If a system clock is available at approximately the same frequency as the crystal, this signal can be selected to provide a faster start-up time. See Table 1-42. |
| 3 | xpump_dis | This bit disables the crystal oscillator voltage pumps. Recommended settings: 1 when VDDA > 2*VCCD (pump disabled) 0 when VDDA <= 2*VCCD (pump enabled) See Table 1-41. |
| 2 | xfb_dis | This bit disables an amplitude monitor on the oscillator signal. If the oscillator amplitude is too low, the XERR bit will be high. See Table 1-39. |
| 1 | xto_dis | This bit disables a watchdog monitor on the oscillator signal. Error output bit is asserted immediately after the oscillator is enabled and is de-asserted as soon as the output clock toggles See Table 1-43. |
| 0 | en | This bit enables the 4 - 25 MHz crystal oscillator circuit when set high. See Table 1-38. |

Reset Table

| resetsignal | field(s) |
|-------------|----------|
|-------------|----------|

1.3.36 FASTCLK_XMHZ_CSR (continued)

Reset Table

System reset for retention
 [reset_all_retention]

en, xto_dis, xfb_dis,
 flops xpump_dis, xstart,
 xprot

Domain reset for non-retention
 [reset_all_nonretention]

xerr
 flops
]

Table 1-38. Bit field encoding: EN_ENUM

| Value | Name | Description |
|-------|------|--|
| 1'b0 | EN_0 | disabled |
| 1'b1 | EN_1 | enabled. Note that the oscillator amplitude takes time to reach stable amplitude. This can be monitored with the XERR bit. |

Table 1-39. Bit field encoding: XFB_DIS_ENUM

| Value | Name | Description |
|-------|-----------|---|
| 1'b0 | XFB_DIS_0 | Feedback enabled - If oscillator has insufficient amplitude, XERR bit will be high. |
| 1'b1 | XFB_DIS_1 | Feedback disabled |

Table 1-40. Bit field encoding: XPROT_ENUM

| Value | Name | Description |
|-------|---------|----------------------------|
| 1'b0 | XPROT_0 | Fault Recovery not enabled |
| 1'b1 | XPROT_1 | Fault Recovery enabled |

Table 1-41. Bit field encoding: XPUMP_DIS_ENUM

| Value | Name | Description |
|-------|-------------|---|
| 1'b0 | XPUMP_DIS_0 | Pumps enabled - Use this setting if Vdd can be <3V. |
| 1'b1 | XPUMP_DIS_1 | Pumps disabled - Only use this if Vdd will be >3V when oscillator is enabled. |

Table 1-42. Bit field encoding: XSTART_ENUM

| Value | Name | Description |
|-------|----------|---|
| 1'b0 | XSTART_0 | Use internal single pulse |
| 1'b1 | XSTART_1 | Use a clock close to the target frequency to improve start-up time. |

Table 1-43. Bit field encoding: XTO_DIS_ENUM

| Value | Name | Description |
|-------|-----------|--|
| 1'b0 | XTO_DIS_0 | Watchdog enabled - Oscillator must achieve proper switching within the internal time window, or XERR will be set high. |
| 1'b1 | XTO_DIS_1 | Watchdog disabled |

1.3.37 FASTCLK_XMHZ_TST

External 4-25 MHz Crystal Oscillator Test Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_XMHZ_TST: 0x40004211

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | test | | | |

(no description)

Register Segment: 1

| Bits | Name | Description |
|------|-----------|------------------|
| 3:0 | test[3:0] | (no description) |

[See Table 1-44.](#)

Table 1-44. Bit field encoding: TEST_ENUM

| Value | Name | Description |
|-------|---------|--|
| 4'h0 | TEST_0 | Check the watch dog circuit |
| 4'h1 | TEST_1 | Trim current & test amplifier (production); Check startup pulses and watchdog (functional) |
| 4'h2 | TEST_2 | Check amplifier NMOS (functional) |
| 4'h3 | TEST_3 | Check feedback resistor (functional) |
| 4'h4 | TEST_4 | Check charge pump clock (functional) |
| 4'h5 | TEST_5 | Check charge pump clock and charge pump output (production) |
| 4'h6 | TEST_6 | Check charge pump output using external clock (functional) |
| 4'h7 | TEST_7 | High Impedance |
| 4'h8 | TEST_8 | Check feedback comparator output |
| 4'h9 | TEST_9 | Brings the dc portion of the amplitude detect out, vdc (functional) |
| 4'ha | TEST_10 | Brings the peak of the amplitude detect out, vmax (functional) |
| 4'hb | TEST_11 | Brings the amplitude of the amplitude detect block out, vamp (functional) |
| 4'hc | TEST_12 | Brings the selected feedback reference voltage, vrefout_fb, onto the test pin (functional) |
| 4'hd | TEST_13 | A buffered version of the clock divider output, clk_div is put onto the test_dig_out pin (production) with en_xtl[4:0]=00101 (FASTCLK_XMHZ_CSR=0x0B) Brings the selected watchdog reference voltage, vrefout_wd onto the test_out pin with en_xtl[4:0]=00111 (FASTCLK_XMHZ_CSR=0x09) |
| 4'he | TEST_14 | Allows an external voltage to be applied to the comparator (production) |
| 4'hf | TEST_15 | Checks that iadj counts down. Uses external clk to trigger counter (functional) |

1.3.38 FASTCLK_XMHZ_CFG0

External 4-25 MHz Crystal Oscillator Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_XMHZ_CFG0: 0x40004212

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|---|---|---|---|
| SW Access:Reset | NA:000 | | | R/W:00000 | | | | |
| HW Access | NA | | | R/W | | | | |
| Name | | | | xcfg | | | | |

(no description)

Register Segment: 1

| Bits | Name | Description |
|------|-----------|---|
| 4:0 | xcfg[4:0] | <p>Selects amplifier transconductance setting, which impacts -R for crystal oscillator startup; Settings are based on the external crystal's parallel resonant load capacitance specification (CL) and its shunt capacitance (C0);</p> <p>CL >= 15pF:</p> <p>C0 >= 3.5pF: Frequency <= 7.3MHz : xcfg = 5'h0E 7.3MHz < Frequency <= 13.2MHz : xcfg = 5'h13 Frequency > 13.2MHz : xcfg = 5'h19</p> <p>C0 < 3.5pF: Frequency <= 6.9MHz : xcfg = 5'h13 Frequency > 6.9MHz : xcfg = 5'h17</p> <p>CL < 15pF:</p> <p>Frequency <= 7.3MHz : xcfg = 5'h0A 7.3MHz < Frequency <= 12.9MHz : xcfg = 5'h0E Frequency > 12.9MHz : xcfg = 5'h13</p> |

1.3.39 FASTCLK_XMHZ_CFG1

External 4-25 MHz Crystal Oscillator Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_XMHZ_CFG1: 0x40004213

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|-------------|---|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | R/W:0000 | | | |
| HW Access | NA | R/W | | | R/W | | | |
| Name | | vref_sel_wd | | | vref_sel_fb | | | |

(no description)

Register Segment: 1

| Bits | Name | Description |
|------|------------------|--|
| 6:4 | vref_sel_wd[2:0] | Selects reference level for watchdog (vrefout_wd); NOTE: vref_sel_fb must be greater than or equal to the binary value of vref_sel_wd. Valid settings are: 5 for XOSC freq < 16 MHz 3 for 16 MHz <= XOSC freq <= 25 MHz See Table 1-46. |
| 3:0 | vref_sel_fb[3:0] | Selects reference level for feedback (vrefout_fb); NOTE: vref_sel_fb must be greater than or equal to the binary value of vref_sel_wd See Table 1-45. |

Table 1-45. Bit field encoding: VREF_SEL_FB_ENUM

| Value | Name | Description |
|-------|----------------|-------------|
| 4'h0 | VREF_SEL_FB_0 | 139 mV |
| 4'h1 | VREF_SEL_FB_1 | 185 mV |
| 4'h2 | VREF_SEL_FB_2 | 231 mV |
| 4'h3 | VREF_SEL_FB_3 | 277 mV |
| 4'h4 | VREF_SEL_FB_4 | 323 mV |
| 4'h5 | VREF_SEL_FB_5 | 370 mV |
| 4'h6 | VREF_SEL_FB_6 | 416 mV |
| 4'h7 | VREF_SEL_FB_7 | 462 mV |
| 4'h8 | VREF_SEL_FB_8 | 508 mV |
| 4'h9 | VREF_SEL_FB_9 | 554 mV |
| 4'ha | VREF_SEL_FB_10 | 601 mV |
| 4'hb | VREF_SEL_FB_11 | 647 mV |
| 4'hc | VREF_SEL_FB_12 | 693 mV |
| 4'hd | VREF_SEL_FB_13 | 739 mV |
| 4'he | VREF_SEL_FB_14 | 786 mV |
| 4'hf | VREF_SEL_FB_15 | 832 mV |

Table 1-46. Bit field encoding: VREF_SEL_WD_ENUM

| Value | Name | Description |
|-------|---------------|-------------|
| 3'h0 | VREF_SEL_WD_0 | 46 mV |
| 3'h1 | VREF_SEL_WD_1 | 92 mV |
| 3'h2 | VREF_SEL_WD_2 | 139 mV |

1.3.39 FASTCLK_XMHZ_CFG1 (continued)

Table 1-46. Bit field encoding: VREF_SEL_WD_ENUM

| | | |
|------|---------------|--------|
| 3'h3 | VREF_SEL_WD_3 | 185 mV |
| 3'h4 | VREF_SEL_WD_4 | 231 mV |
| 3'h5 | VREF_SEL_WD_5 | 277 mV |
| 3'h6 | VREF_SEL_WD_6 | 323 mV |
| 3'h7 | VREF_SEL_WD_7 | 370 mV |

1.3.40 FASTCLK_PLL_CFG0

PLL Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_CFG0: 0x40004220

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|--------|---|--------|---|---|-------|
| SW Access:Reset | R/W:01 | | R/W:01 | | NA:000 | | | R/W:0 |
| HW Access | R | | R | | NA | | | R |
| Name | wait | | delay | | | | | en |

This register provides status and control for the PLL.

Register Segment: 1

| Bits | Name | Description |
|------|------------|--|
| 7:6 | wait[1:0] | Lock detect wait time before declaring lock. PLL must show minimal phase error for this many cycles of the PFD input clock before lock is declared. See Table 1-49. |
| 5:4 | delay[1:0] | Lock detect delay time -- approximate delay time before sampling PFD output for lock detection. See Table 1-47. |
| 0 | en | Enable PLL See Table 1-48. |

Table 1-47. Bit field encoding: DELAY_ENUM

| Value | Name | Description |
|-------|-----------|----------------------|
| 2'h0 | DELAY_3NS | 3 ns delay (nominal) |
| 2'h1 | DELAY_5NS | 5 ns delay |
| 2'h2 | DELAY_7NS | 7 ns delay |
| 2'h3 | DELAY_8NS | 8 ns delay |

Table 1-48. Bit field encoding: PLL_EN_ENUM

| Value | Name | Description |
|-------|----------------|--------------|
| 1'b0 | PLL_EN_DISABLE | PLL Disabled |
| 1'b1 | PLL_EN_ENABLE | PLL Enabled |

Table 1-49. Bit field encoding: WAIT_ENUM

| Value | Name | Description |
|-------|--------|---|
| 2'h0 | WAIT_0 | 7 PFD-clock periods (PFD clock period = 1 us if PFD input clock is 1 MHz) |
| 2'h1 | WAIT_1 | 15 PFD-clock periods |
| 2'h2 | WAIT_2 | 23 PFD-clock periods |
| 2'h3 | WAIT_3 | 31 PFD-clock periods |

1.3.41 FASTCLK_PLL_CFG1

PLL Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_CFG1: 0x40004221

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---|---|-------|---|----------|---|
| SW Access:Reset | NA:0 | R/W:100 | | | NA:00 | | R/W:10 | |
| HW Access | NA | R | | | NA | | R | |
| Name | | icpsel | | | | | vco_gain | |

This register sets trim levels and test modes in the PLL.

Register Segment: 1

| Bits | Name | Description |
|------|---------------|---|
| 6:4 | icpsel[2:0] | Charge Pump current select. This bit-field should be set to 0x01 for all configurations. See Table 1-50. |
| 1:0 | vco_gain[1:0] | VCO loop gain. Gain doesn't begin effect the VCO frequency characteristics untill freq>60MHz. Effect of gain setting is provided at 25C, Vctrl=0.925V. See Table 1-51. |

Table 1-50. Bit field encoding: PLL_ICPSEL_ENUM

| Value | Name | Description |
|-------|--------------|-------------|
| 3'h0 | PLL_ICPSEL_0 | 1uA |
| 3'h1 | PLL_ICPSEL_1 | 2uA |
| 3'h2 | PLL_ICPSEL_2 | 3uA |
| 3'h3 | PLL_ICPSEL_3 | 4uA |
| 3'h4 | PLL_ICPSEL_4 | 5uA |
| 3'h5 | PLL_ICPSEL_5 | 6uA |
| 3'h6 | PLL_ICPSEL_6 | 7uA |
| 3'h7 | PLL_ICPSEL_7 | 1uA |

Table 1-51. Bit field encoding: PLL_VCO_GAIN_ENUM

| Value | Name | Description |
|-------|----------------|-------------|
| 2'h0 | PLL_VCO_GAIN_0 | RESERVED |
| 2'h1 | PLL_VCO_GAIN_1 | RESERVED |
| 2'h2 | PLL_VCO_GAIN_2 | 456 MHz/V |
| 2'h3 | PLL_VCO_GAIN_3 | RESERVED |

1.3.42 FASTCLK_PLL_P

PLL P-Counter Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_P: 0x40004222

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000100 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | p | | | | | | | |

This register sets the P-Counter value, an 8-bit feedback divider

Register Segment: 1

| Bits | Name | Description |
|------|--------|--|
| 7:0 | p[7:0] | P-Counter divide value. Settings less than 8 do not give valid outputs. Valid range is 8 - 255, but this must still give a divided frequency of 1 - 3 MHz (PLLOUT / P); this is the limit of the implementation. Set the P-Counter to legal value before enabling PLL. $f_{out} = f_{in} \cdot (P/Q)$ |

[See Table 1-52.](#)

Table 1-52. Bit field encoding: P_ENUM

| Value | Name | Description |
|-------|----------|-----------------------------------|
| 8'h08 | P_DIV8 | Divide by 8 (minimum valid value) |
| 8'h09 | P_DIV9 | Divide by 9 |
| 8'h0A | P_DIV10 | Divide by 10 |
| 8'h0f | P_DIV15 | Divide by 15 |
| 8'hfe | P_DIV254 | Divide by 254 |
| 8'hff | P_DIV255 | Divide by 255 |

1.3.43 FASTCLK_PLL_Q

PLL Q-Counter Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_Q: 0x40004223

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0011 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | q | | | |

This register sets the Q-Counter value, a 4-bit divider on the input clock to the PLL.

Register Segment: 1

| Bits | Name | Description |
|------|--------|---|
| 3:0 | q[3:0] | Q-Counter divide value. qrt-The Q divider (Reference) input Freq range is: 1-48MHz. The Q divider output Freq (and PFD input Freq) must be between 1-3MHz. $f_{out} = f_{in} * (P/Q)$ |

[See Table 1-53.](#)

Table 1-53. Bit field encoding: Q_ENUM

| Value | Name | Description |
|-------|---------|--------------|
| 4'h0 | Q_DIV1 | Divide by 1 |
| 4'h1 | Q_DIV2 | Divide by 2 |
| 4'h2 | Q_DIV3 | Divide by 3 |
| 4'h3 | Q_DIV4 | Divide by 4 |
| 4'h4 | Q_DIV5 | Divide by 5 |
| 4'h5 | Q_DIV6 | Divide by 6 |
| 4'h6 | Q_DIV7 | Divide by 7 |
| 4'h7 | Q_DIV8 | Divide by 8 |
| 4'h8 | Q_DIV9 | Divide by 9 |
| 4'h9 | Q_DIV10 | Divide by 10 |
| 4'ha | Q_DIV11 | Divide by 11 |
| 4'hb | Q_DIV12 | Divide by 12 |
| 4'hc | Q_DIV13 | Divide by 13 |
| 4'hd | Q_DIV14 | Divide by 14 |
| 4'he | Q_DIV15 | Divide by 15 |
| 4'hf | Q_DIV16 | Divide by 16 |

1.3.44 FASTCLK_PLL_TST

PLL Test Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_TST: 0x40004224

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|---|---|
| SW Access:Reset | NA:00000 | | | | | R/W:000 | | |
| HW Access | NA | | | | | R | | |
| Name | | | | | | test | | |

(no description)

Register Segment: 1

| Bits | Name | Description |
|------|-----------|--|
| 2:0 | test[2:0] | Test Modes for the PLL. See Table 1-54. |

Table 1-54. Bit field encoding: PLL_TEST_ENUM

| Value | Name | Description |
|--------|--------------------|--|
| 3'b000 | PLL_TEST_NORMAL | Normal Operation with fast lock pre-charge |
| 3'b001 | PLL_TEST_PFD_DISAB | PFD Disable Test (Loop filter leakage test, free-running VCO test) |
| 3'b010 | PLL_TEST_VCTRL_INT | V_CTRL Internal Test Mode (Disables PFD, $F_{OUT}=F_{OFFSET}+K_{VCO}*I_{CP}*(R_L+R_S)$) |
| 3'b011 | PLL_TEST_VCTRL_EX | V_CTRL External Test Mode (Disables PFD, Shorts V_CTRL to external test pin) |
| 3'b100 | PLL_TEST_SENSE | Sense P Counter outputs, Sense Lock Detect Phase Error |
| 3'b101 | PLL_TEST_NORMAL_S | Normal operation without fast lock pre-charge |
| 3'b110 | PLL_TEST_NORMAL_P | Normal operation with fast lock circuit and with runaway detect |
| 3'b111 | PLL_TEST_CP_CURRE | Charge Pump Current Test Mode (Disables PFD, Forces Pump UP in CP, Shorts V_CTRL to external test pin) |

1.3.45 FASTCLK_PLL_SR

PLL Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

FASTCLK_PLL_SR: 0x40004225

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|-------|---------|
| SW Access:Reset | NA:000000 | | | | | | RC:0 | RC:0 |
| HW Access | NA | | | | | | W | W |
| Name | | | | | | | ilock | lockdet |

(no description)

Register Segment: 1

| Bits | Name | Description |
|------|---------|---|
| 1 | ilock | Instantaneous lock signal |
| 0 | lockdet | Lock Status Flag. If lock is acquired this flag will stay set (regardless of whether lock is subsequently lost) until it is read. Upon reading it will clear. If lock is still true then the bit will simply set again. If lock happens to be false when the clear on read occurs then the bit will stay cleared until the next lock event. |

1.3.46 SLOWCLK_ILO_CR0

Internal Low-speed Oscillator Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SLOWCLK_ILO_CR0: 0x40004300

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|---------|------|---------|-------|------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:1 | NA:0 | R/W:1 | R/W:1 | NA:0 |
| HW Access | NA | | R | R | NA | R | R | NA |
| Name | | | div3en | pd_mode | | en_100k | en_1k | |

This register controls operation of the ILO output clocks.

Register Segment: 0

| Bits | Name | Description |
|------|---------|---|
| 5 | div3en | Divide-by-3 enable for 100 kHz output See Table 1-55. |
| 4 | pd_mode | Power down mode for ILO See Table 1-56. |
| 2 | en_100k | Enables 100kHz ILO clock output when set. When clear, clock output is low. |
| 1 | en_1k | Enables 1kHz ILO clock output when set. This bit is forced on when PM.WDT_CFG.wdr_en bit is set. When clear, clock output is low. |

Table 1-55. Bit field encoding: DIV3EN_ENUM

| Value | Name | Description |
|-------|----------|--------------------------------------|
| 1'b0 | DIV3EN_0 | CLK33K disabled |
| 1'b1 | DIV3EN_1 | CLK33K enabled, divides CLK100K by 3 |

Table 1-56. Bit field encoding: PD_MODE_ENUM

| Value | Name | Description |
|-------|-----------|--|
| 1'b0 | PD_MODE_0 | Faster start-up, internal bias left on |
| 1'b1 | PD_MODE_1 | Slower start-up, internal bias off |

1.3.47 SLOWCLK_ILO_CR1

Internal Low-speed Oscillator Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SLOWCLK_ILO_CR1: 0x40004301

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|----------|----------|-----------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R/W | R | R |
| Name | | | | | | freq_sel | bias_opt | dis_turbo |

This register controls non-standard features of the ILO.

Register Segment: 0

| Bits | Name | Description |
|------|-----------|---|
| 2 | freq_sel | Frequency select for CLK100K See Table 1-59. |
| 1 | bias_opt | Alternate bias for ILO See Table 1-57. |
| 0 | dis_turbo | Start-up speed control See Table 1-58. |

Table 1-57. Bit field encoding: BIAS_OPT_ENUM

| Value | Name | Description |
|-------|------------|------------------------------|
| 1'b0 | BIAS_OPT_0 | sub-threshold bias (default) |
| 1'b1 | BIAS_OPT_1 | Use saturated bias |

Table 1-58. Bit field encoding: DIS_TURBO_ENUM

| Value | Name | Description |
|-------|-------------|-----------------------------|
| 1'b0 | DIS_TURBO_0 | Turbo enabled (recommended) |
| 1'b1 | DIS_TURBO_1 | Turbo disabled |

Table 1-59. Bit field encoding: FREQ_SEL_ENUM

| Value | Name | Description |
|-------|------------|-----------------------------|
| 1'b0 | FREQ_SEL_0 | CLK100K defaults to 100 kHz |
| 1'b1 | FREQ_SEL_1 | CLK100K defaults to 32 kHz |

1.3.48 SLOWCLK_X32_CR

External 32kHz Crystal Oscillator Control Register

Reset: Reset Signals Listed Below

Register : Address

SLOWCLK_X32_CR: 0x40004308

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|----------|----------|------|-------|-------|-------|
| SW Access:Reset | NA:00 | | R:0 | R:U | NA:0 | R/W:1 | R/W:0 | R/W:0 |
| HW Access | NA | | W | W | NA | R | R | R |
| Name | | | ana_stat | dig_stat | | pdb | lpm | x32en |

This register controls operation of the 32K Crystal Oscillator, and provides status on the oscillator's stability.

| Bits | Name | Description |
|------|----------|---|
| 5 | ana_stat | Indicates oscillator status, using internal analog measurement. See Table 1-60. |
| 4 | dig_stat | Indicates oscillator status, using test against a reference clock. The ILO's CLK33K must be enabled for this function to operate. See Table 1-61. |
| 2 | pdb | Power switch enable (active-low powerdown) for 32K crystal oscillator. When enabling the X32, it is recommended to set this bit first, then set en=1 in a separate bus cycle. The X32 is automatically powered down during hibernate modes. |
| 1 | lpm | Power setting for 32K crystal oscillator. This setting only takes effect in sleep modes. During active modes, the oscillator always runs in high power mode. See Table 1-62. |
| 0 | x32en | 32K Crystal Oscillator Enable See Table 1-63. |

Reset Table

| resetsignal | field(s) |
|---|-----------------|
| N/A | dig_stat |
| System reset for retention flops [reset_all_retention] | x32en, lpm, pdb |
| Domain reset for non-retention flops [reset_all_nonretention] | ana_stat |

Table 1-60. Bit field encoding: ANA_STAT_ENUM

| Value | Name | Description |
|-------|------------|-----------------------|
| 1'b0 | ANA_STAT_0 | oscillator not stable |
| 1'b1 | ANA_STAT_1 | oscillator stable |

1.3.48 SLOWCLK_X32_CR (continued)

Table 1-61. Bit field encoding: DIG_STAT_ENUM

| Value | Name | Description |
|-------|------------|-----------------------|
| 1'b0 | DIG_STAT_0 | oscillator not stable |
| 1'b1 | DIG_STAT_1 | oscillator stable |

Table 1-62. Bit field encoding: LPM_ENUM

| Value | Name | Description |
|-------|-------|--|
| 1'b0 | LPM_0 | High Power Mode |
| 1'b1 | LPM_1 | Low Power Mode (Only applies in chip sleep mode) |

Table 1-63. Bit field encoding: X32EN_ENUM

| Value | Name | Description |
|-------|----------|---------------------------------|
| 1'b0 | X32_EN_0 | Oscillator disabled, power down |
| 1'b1 | X32_EN_1 | Oscillator enabled |

1.3.49 SLOWCLK_X32_CFG

External 32kHz Crystal Oscillator Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SLOWCLK_X32_CFG: 0x40004309

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|--------|---|---|--------|---|-------|---------|
| SW Access:Reset | R/W:0 | NA:000 | | | R/W:01 | | R/W:0 | R/W:0 |
| HW Access | R | NA | | | R | | R | R |
| Name | lp_allow | | | | lp | | test | xrefclk |

This register provides options for configuring the 32kHz Crystal Oscillator block. These options are normally only used for testing or factory calibration.

| Bits | Name | Description |
|------|----------|--|
| 7 | lp_allow | Low power oscillator mode configuration. See Table 1-66. |
| 3:2 | lp[1:0] | GM Setting for LPM=1. See Table 1-64. |
| 1 | test | Enables a test mode to bring the internal current reference out. See Table 1-65. |
| 0 | xrefclk | Allows external clock to be driving into the crystal oscillator input, normally for test. See Table 1-67. |

Table 1-64. Bit field encoding: LP_ENUM

| Value | Name | Description |
|-------|--------|------------------------------------|
| 2'b00 | LP_MIN | Lowest power setting |
| 2'b01 | LP_LOW | Default setting, Low Power setting |
| 2'b10 | LP_MED | Medium power setting |
| 2'b11 | LP_MAX | Highest power setting |

Table 1-65. Bit field encoding: TEST_ENUM

| Value | Name | Description |
|-------|--------|---|
| 1'b0 | TEST_0 | Normal operation |
| 1'b1 | TEST_1 | Enables ref current x1000 to come to a pad for test |

Table 1-66. Bit field encoding: X32_CFG_ENUM

| Value | Name | Description |
|-------|--------|---|
| 1'b0 | LP_OFF | Low power oscillator mode allowed only in sleep mode. |
| 1'b1 | LP_ON | Low power oscillator mode allowed in active mode. |

Table 1-67. Bit field encoding: XREFCLK_ENUM

| Value | Name | Description |
|-------|-----------|---|
| 1'b0 | XREFCLK_0 | Normal operation |
| 1'b1 | XREFCLK_1 | Signal at crystal input assumed to be a clock, which is driven to the crystal output pad and to the internal CLK32K |

1.3.50 SLOWCLK_X32_TST

External 32kHz Crystal Oscillator Test Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SLOWCLK_X32_TST: 0x4000430A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:01011111 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | test | | | | | | | |

This register provides for DFT options for the 32kHz external crystal oscillator block.

| Bits | Name | Description |
|------|-----------|--|
| 7:0 | test[7:0] | Test bits -- leave high for normal operation |

1.3.51 BOOST_CR0

Boost Control 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR0: 0x40004320

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|--------|---|-----------|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:11 | | R/W:00100 | | | | |
| HW Access | R/W | R/W | | R/W | | | | |
| Name | thump | mode | | vsel | | | | |

Boost output voltage and mode control register.

Register Segment: 1

| Bits | Name | Description |
|------|-----------|--|
| 7 | thump | Generate a 1us pulse on 0->1 transition |
| 6:5 | mode[1:0] | Boost mode select. See Table 1-68. |
| 4:0 | vsel[4:0] | Boost voltage selection See Table 1-69. |

Table 1-68. Bit field encoding: mode_enum

| Value | Name | Description |
|-------|--------------|--------------|
| 2'b11 | MODE_ACTIVE | Active mode |
| 2'b01 | MODE_STANDBY | Standby mode |
| 2'b10 | MODE_10 | Reserved |
| 2'b00 | MODE_00 | Reserved |

Table 1-69. Bit field encoding: vsel_enum

| Value | Name | Description |
|----------|------------|---|
| 5'b00000 | VSEL_OFF | Off (0V) |
| 5'b00001 | VSEL_1P60V | 1.60V |
| 5'b00010 | VSEL_1P70V | 1.70V |
| 5'b00011 | VSEL_1P80V | 1.80V (Default when {Vint1,Vint0} == 2'b01) |
| 5'b00100 | VSEL_1P90V | 1.90V |
| 5'b00101 | VSEL_2P00V | 2.00V |
| 5'b00110 | VSEL_2P10V | 2.10V |
| 5'b00111 | VSEL_2P20V | 2.20V |
| 5'b01000 | VSEL_2P30V | 2.30V |
| 5'b01001 | VSEL_2P40V | 2.40V |
| 5'b01010 | VSEL_2P50V | 2.50V |
| 5'b01011 | VSEL_2P60V | 2.60V |
| 5'b01100 | VSEL_2P70V | 2.70V (Default when {Vint1,Vint0} == 2'b10) |
| 5'b01101 | VSEL_2P80V | 2.80V |
| 5'b01110 | VSEL_2P90V | 2.90V |
| 5'b01111 | VSEL_3P00V | 3.00V |
| 5'b10000 | VSEL_3P10V | 3.10V |
| 5'b10001 | VSEL_3P20V | 3.20V |

1.3.51 BOOST_CR0 (continued)

Table 1-69. Bit field encoding: vsel_enum

| | | |
|----------|------------|---|
| 5'b10010 | VSEL_3P30V | 3.30V (Default when {Vint1,Vint0} == 2'b11) |
| 5'b10011 | VSEL_3P40V | 3.40V |
| 5'b10100 | VSEL_3P50V | 3.50V |
| 5'b10101 | VSEL_3P60V | 3.60V |
| 5'b10110 | VSEL_4P00V | 4.00V - Schottky diode req'd |
| 5'b10111 | VSEL_4P25V | 4.25V - Schottky diode req'd |
| 5'b11000 | VSEL_4P50V | 4.50V - Schottky diode req'd |
| 5'b11001 | VSEL_4P75V | 4.75V - Schottky diode req'd |
| 5'b11010 | VSEL_5P00V | 5.00V - Schottky diode req'd |
| 5'b11011 | VSEL_5P25V | 5.25V - Schottky diode req'd |
| 5'b11100 | VSEL_0x1C | Reserved |
| 5'b11101 | VSEL_0x1D | Reserved |
| 5'b11110 | VSEL_0x1E | Reserved |
| 5'b11111 | VSEL_0x1F | Reserved |

1.3.52 BOOST_CR1

Boost Control 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR1: 0x40004321

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---------|---------|--------|---|
| SW Access:Reset | R/W:0000 | | | | R/W:1 | R/W:0 | R/W:01 | |
| HW Access | R/W | | | | R/W | R/W | R/W | |
| Name | tst | | | | boosten | extmode | clk | |

Boost test, clock, and mode control register.

Register Segment: 1

| Bits | Name | Description |
|------|----------|--|
| 7:4 | tst[3:0] | Test mode for IV char of drive transistors. Setting tst[0] also inhibits discontinuous operation. See Table 1-71. |
| 3 | boosten | When set, enables boost operation. For PSoC5 devices to wake-up from low power modes because of boost under voltage event, it is must that BOOST_CR4[0] boost_ie is set. |
| 2 | extmode | Reserved |
| 1:0 | clk[1:0] | Boost clock frequency See Table 1-70. |

Table 1-70. Bit field encoding: clk_enum

| Value | Name | Description |
|-------|------------|-------------|
| 2'b00 | RSVD00 | Reserved |
| 2'b01 | CLK_400KHZ | 400 KHz |
| 2'b10 | RSVD10 | Reserved |
| 2'b11 | CLK_EXT | External |

Table 1-71. Bit field encoding: tst_enum

| Value | Name | Description |
|---------|-------------|------------------|
| 4'b0000 | TST_OFF | Test mode off |
| 4'b0111 | TST_ST_PMOS | PMOS on (strong) |
| 4'b0110 | TST_WE_PMOS | PMOS on (weak) |
| 4'b0101 | TST_ST_NMOS | NMOS on (strong) |
| 4'b0100 | TST_WE_NMOS | NMOS on (weak) |

1.3.53 BOOST_CR2

Boost Control 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR2: 0x40004322

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|----------|-------|---------|---------|--------|-------|-------|
| SW Access:Reset | R:0 | R:1 | R:0 | R:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | disc | boosting | equal | bucking | erefsel | limoff | eqoff | enatm |

Boost configuration and status register. The lower 4 bits are advanced configuration and the upper 4 bits are status.

Register Segment: 1

| Bits | Name | Description |
|------|----------|---|
| 7 | disc | When set, boost converter is operating in discontinuous mode |
| 6 | boosting | When set, converter is boosting ($V_{in} < V_{sel}$) |
| 5 | equal | When set, converter is bypassed ($V_{in}=V_{sel}$). V_{in} connected to V_{out} |
| 4 | bucking | When set, converter is bucking. This is always 0 for boost only converters. |
| 3 | erefsel | When set, selects external reference See Table 1-72. |
| 2 | limoff | When set, turns off skip cycle current limiter |
| 1 | eqoff | When set, disables auto battery connect to output when $V_{in}=V_{sel}$ |
| 0 | enatm | When set, enables automatic standby regulator |

Table 1-72. Bit field encoding: BOOST_EREFSSEL_ENUM

| Value | Name | Description |
|-------|-----------------------------|--|
| 1'b0 | BOOST_EREFSSEL_INT ERNAL | Select internal reference |
| 1'b1 | BOOST_EREFSSEL_EXT ERNAL | Select external 800mv precision reference (vref_800mv) |

1.3.54 BOOST_CR3

Boost Control 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR3: 0x40004323

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | pwm | | | | | | | |

Boost PWM value (not written during normal operation).

Register Segment: 1

| Bits | Name | Description |
|------|----------|--|
| 7:0 | pwm[7:0] | PWM value should not be written during normal operation. |

1.3.55 BOOST_SR

Boost Status

Reset: N/A

Register : Address

BOOST_SR: 0x40004324

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-----|-----|------|-----|-----|
| SW Access:Reset | R:U | R:U | R:U | R:U | R:U | R:U | R:U | R:U |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | ready | start | nobat | ov | vhi | vnom | vlo | uv |

Boost status, including window comparator results.

| Bits | Name | Description |
|------|-------|---|
| 7 | ready | When set, internal circuits have been initialized |
| 6 | start | When set, converter is in startup mode |
| 5 | nobat | When set, battery input is grounded (no battery present) |
| 4 | ov | Output above overvoltage limit when 1, below limit when 0 |
| 3 | vhi | Output is above vhigh limit when 1, below limit when 0 |
| 2 | vnom | Output is above nominal when 1, below nominal when 0 |
| 1 | vlo | Output is above vlow limit when 1, below limit when 0 |
| 0 | uv | Output is above undervoltage limit when 1, below limit when 0 |

1.3.56 BOOST_CR4

Boost Control Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR4: 0x40004325

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|---------|----------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | clk_ilo | clk_eco | boost_ie |

Boost interrupt control register.

| Bits | Name | Description |
|------|----------|--|
| 2 | clk_ilo | When set, 32k ILO is connected to boost external clock instead of 32k crystal oscillator. To prevent collision, user needs to make sure that crystal oscillator source is turned off |
| 1 | clk_eco | When set, 32k crystal oscillator is connected to boost external clock instead of 32k ILO. To prevent collision, user needs to make sure that clk_ilo source is turned off. |
| 0 | boost_ie | When set, a boost undervoltage condition is propagated to the interrupt controller via the PM interrupt line. When clear, the interrupt condition is masked. |

1.3.57 BOOST_SR2

Boost Status Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_SR2: 0x40004326

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|-----------|
| SW Access:Reset | NA:0000000 | | | | | | | RC:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | boost_int |

Boost interrupt status register.

| Bits | Name | Description |
|------|-----------|--|
| 0 | boost_int | When set, a boost undervoltage event has occurred. The setting of limact_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field) |

1.3.58 PWRSYS_CR0

Power System Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_CR0: 0x40004330

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|----------|----------|--------|---|---|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | NA | | R | R | NA | | | R |
| Name | | | ext_vccd | ext_vcca | | | | rbbnw_dis |

This register controls the voltage regulators.

Register Segment: 0

| Bits | Name | Description |
|------|-----------|--|
| 5 | ext_vccd | When set, the core digital (vccd) pin is driven with an externally regulated voltage. This disables the internal LDO-D regulator. If both LDO's are disabled, the BREF will be automatically disabled, too. The BREF must be manually enabled before re-enabling either LDO. |
| 4 | ext_vcca | When set, the core analog (vcca) pin is driven with an externally regulated voltage. This disables the internal LDO-A regulator. If both LDO's are disabled, the BREF will be automatically disabled, too. The BREF must be manually enabled before re-enabling either LDO. |
| 0 | rbbnw_dis | When set, disables the nwell reverse biasing during low power modes. Nwell reverse biasing is always disabled during active/standby modes. |

1.3.59 PWRSYS_CR1

Power System Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_CR1: 0x40004331

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------------|----------|----------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | i2creg_backup | ldoa_dis | ldoa_iso |

This register controls the voltage regulators.

Register Segment: 1

| Bits | Name | Description |
|------|---------------|--|
| 2 | i2creg_backup | When set, enables the I2C regulator backup. The I2C backup regulator enables the I2C logic to wake the chip from sleep mode on an I2C address match. |
| 1 | ldoa_dis | When set, disables the analog LDO regulator. This bit will not be set unless the ldoa_iso field is already set. Attempts to set this field while simultaneously clearing ldoa_iso will be ignored. |
| 0 | ldoa_iso | When set, prepares the system to disable the LDO-A. In this mode, the LV reference (bandgap) is supplied by the digital LDO. Also, outputs of vcca are isolated from the rest of the system. Note that this mode can result in degraded accuracy, as described in the Power Modes chapter. Once set, cannot be cleared unless ldoa_dis is already clear. |

1.3.60 PM_TW_CFG0

Timewheel Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_TW_CFG0: 0x40004380

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ftw_interval | | | | | | | |

This register controls settings for the fast timewheel. If using low power active (LPA) mode, the fast timewheel must be used to program the burst period.

Register Segment: 1

| Bits | Name | Description |
|------|-------------------|--|
| 7:0 | ftw_interval[7:0] | Sets the fast timewheel interval. The fast timewheel is programmed using a 8-bit terminal count (N-1) and is clocked by the ILO at 100 kHz. When the terminal count is reached, the timewheel automatically resets and begins counting again. This value can only be changed when {PM.TW_CFG2}.ftw_en is clear. After enabling, the duration before the first event is between 1 and 2 additional cycles, depending on synchronization with the ILO clock. Additional events occur periodically with a period of (1+ftw_interval). |

1.3.61 PM_TW_CFG1

Timewheel Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_TW_CFG1: 0x40004381

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|--------------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:1001 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | ctw_interval | | | |

This register controls settings for the central timewheel.

Register Segment: 1

| Bits | Name | Description |
|------|-------------------|---|
| 3:0 | ctw_interval[3:0] | Sets the central timewheel interval. The period is based on the ILO running at 1 kHz. When the interval is reached, it is automatically restarted. The first interval can range from 1 to (period + 1) ms. Additional intervals occur at the nominal period. This value can only be changed when {TW_CFG2}.ctw_en is clear. |

[See Table 1-73.](#)

Table 1-73. Bit field encoding: ctw_interval_enum

| Value | Name | Description |
|---------|----------------|--|
| 4'b0000 | CTW_1_TICK | not presently supported ==> is same as CTW_2_TICKS |
| 4'b0001 | CTW_2_TICKS | 2 CTW ticks ==> 2ms (nominal) |
| 4'b0010 | CTW_4_TICKS | 4 CTW ticks ==> 4ms (nominal) |
| 4'b0011 | CTW_8_TICKS | 8 CTW ticks ==> 8ms (nominal) |
| 4'b0100 | CTW_16_TICKS | 16 CTW ticks ==> 16ms (nominal) |
| 4'b0101 | CTW_32_TICKS | 32 CTW ticks ==> 32ms (nominal) |
| 4'b0110 | CTW_64_TICKS | 64 CTW ticks ==> 64ms (nominal) |
| 4'b0111 | CTW_128_TICKS | 128 CTW ticks ==> 128ms (nominal) |
| 4'b1000 | CTW_256_TICKS | 256 CTW ticks ==> 256ms (nominal) |
| 4'b1001 | CTW_512_TICKS | 512 CTW ticks ==> 512ms (nominal) |
| 4'b1010 | CTW_1024_TICKS | 1024 CTW ticks ==> 1024ms (nominal) |
| 4'b1011 | CTW_2048_TICKS | 2048 CTW ticks ==> 2048ms (nominal) |
| 4'b1100 | CTW_4096_TICKS | 4096 CTW ticks ==> 4096ms (nominal) |

1.3.62 PM_TW_CFG2

Timewheel Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_TW_CFG2: 0x40004382

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-----------|-----------|--------|--------|--------|--------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R | R | R | R | R | R |
| Name | | | onepps_ie | onepps_en | ctw_ie | ctw_en | ftw_ie | ftw_en |

This register controls settings for the central and fast timewheels.

Register Segment: 1

| Bits | Name | Description |
|------|-----------|---|
| 5 | onepps_ie | When set and one pulse-per-second is enabled, an interrupt is issued when the pulse occurs. If onepps_en is not enabled, no interrupt is generated. |
| 4 | onepps_en | When set, the system returns to the active global power mode once every second. The 32 kHz external crystal oscillator must be enabled to use the one pulse-per-second function. For PSoC5 devices to wake-up from low power modes with onepps interrupt, it is must that onepps_ie is set. |
| 3 | ctw_ie | When set and the central timewheel is enabled, an interrupt is issued when the central timewheel reaches the selected interval. If ctw_en is not enabled, no interrupt is generated. |
| 2 | ctw_en | When set, the system returns to the active global power mode when the central timewheel reaches the interval selected in {PM.TW_CFG1}.ctw_interval. The ILO 1 kHz clock source must be enabled to use the central timewheel. For PSoC5 devices to wake-up from low power modes with ctw interrupt, it is must that ctw_ie is set. |
| 1 | ftw_ie | When set and the fast timewheel is enabled, an interrupt is issued when it reaches the terminal count. If ftw_en is not enabled, no interrupt is generated. This bit is ignored when LPA is enabled, and no interrupts are issued. |
| 0 | ftw_en | When set, the system returns to the active global power mode when the fast timewheel reaches the terminal count selected in {PM.TW_CFG0}.ftw_interval. This bit should be set when using Low Power Active (lpa) mode, since the fast timewheel is usually used to control the LPA burst period. The ILO 100 kHz clock source must be enabled to use the fast timewheel. |

1.3.63 PM_WDT_CFG

Watchdog Timer Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WDT_CFG: 0x40004383

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|------------|---|--------|-------|---|--------------|---|
| SW Access:Reset | R/W:0 | R/W:01 | | R/W:0 | NA:00 | | R/W:01 | |
| HW Access | R | R | | R | NA | | R | |
| Name | ctw_reset | wdt_lpmode | | wdr_en | | | wdt_interval | |

This register controls the watchdog timer (WDT) settings.

Register Segment: 0

| Bits | Name | Description |
|------|-------------------|---|
| 7 | ctw_reset | When a one is written to this field, the free-running central timewheel counter is reset to 0 and held there. Firmware must then write a zero to exit the reset state. Since the central timewheel is used for many timing tasks (including buzz timing and WDT), care must be taken when resetting it. It is generally recommended to reset it only once when the watchdog is enabled, to ensure that first watchdog period is full. Cannot be changed after the watchdog is enabled. |
| 6:5 | wdt_lpmode[1:0] | If the Watchdog-Timer (WDT) is enabled, these 2 bits are used to define how the WDT behaves when the part enters Sleep/Idle/Hibtimers (low power) mode. By default (wdt_lpmode is left 01), the system will automatically use the longest WDT interval when Sleep/Idle/Hibtimers mode is entered - so SW isn't burdened with waking just to feed the WDT. This is true regardless of the value programmed in the wdt_interval register. Upon wakeup, the interval will remain at the highest setting until the WDT is fed the first time by the user. A feeding at this point will cause the interval to automatically return to the normal setting (value in wdt_interval). If this field is set to NOCHANGE ('00'), the system does not change the interval and does not feed the WDT when entering Sleep/Idle/Hibtimers mode. If DISABLED (wdt_lpmode=11), the WDT is turned off when Sleep/Idle/Hibtimers mode is entered and remains disabled until the first feeding by the user after Active mode is reentered. This field cannot be changed once {PM.WDT_CFG}.wdr_en is set. See Table 1-75. |
| 4 | wdr_en | When set, enables the watchdog reset (WDR) using the current WDT settings. Once enabled, the WDT cannot be disabled except by a reset. Setting this bit automatically enables the ILO 1 kHz clock source. |
| 1:0 | wdt_interval[1:0] | Selects the central timewheel taps that control the WDT period. The accuracy of the intervals are dependent upon the accuracy of the oscillator used. A watchdog reset (WDR) may be issued at any time within the selected interval, so software should be programmed to service the WDT before the lower bound is reached (two tap periods). A WDR is always issued within three tap periods. Once {PM.WDT_CFG}.wdr_en is set, the watchdog interval cannot be changed. See Table 1-74. |

Table 1-74. Bit field encoding: wdt_interval_enum

| Value | Name | Description |
|-------|---------------|---------------------------------|
| 2'b00 | WDT_2_TICKS | 2 CTW ticks ==> 4ms - 6ms |
| 2'b01 | WDT_16_TICKS | 16 CTW ticks ==> 32ms - 48ms |
| 2'b10 | WDT_128_TICKS | 128 CTW ticks ==> 256ms - 384ms |

1.3.63 PM_WDT_CFG (continued)

Table 1-74. Bit field encoding: wdt_interval_enum

| | | |
|-------|----------------|------------------------------------|
| 2'b11 | WDT_1024_TICKS | 1024 CTW ticks ==> 2.048s - 3.072s |
|-------|----------------|------------------------------------|

Table 1-75. Bit field encoding: wdt_lpmode_enum

| Value | Name | Description |
|-------|------------------------|--|
| 2'b00 | WDT_LPMODE_NOCHANGE | WDT does not change behavior when Sleep/Idle Mode/Hibtimers is entered |
| 2'b01 | WDT_LPMODE_MAXINTERVAL | WDT automatically switches to max interval when Sleep/Idle/Hibtimers Mode is entered |
| 2'b10 | WDT_LPMODE_RESERVED | Reserved (acts the same as NOCHANGE) |
| 2'b11 | WDT_LPMODE_DISABLED | WDT is disabled when Sleep/Idle/Hibtimers Mode is entered |

1.3.64 PM_WDT_CR

Watchdog Timer Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WDT_CR: 0x40004384

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/WOC:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | wdt_clear | | | | | | | |

This register is used to feed the watchdog timer (WDT).

Register Segment: 1

| Bits | Name | Description |
|------|----------------|--|
| 7:0 | wdt_clear[7:0] | Any write to this field feeds the WDT. After each feeding, there are at least two entire watchdog timer tap periods before a WDR occurs. Always reads as zero. |

1.3.65 PM_INT_SR

Power Manager Interrupt Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_INT_SR: 0x40004390

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------------|------------|---------|---------|
| SW Access:Reset | NA:0000 | | | | RC:0 | RC:0 | RC:0 | RC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | limact_int | onepps_int | ctw_int | ftw_int |

This register indicates which interrupts occurred since the last read of the register. All bits are automatically cleared on read. If an interrupt gets generated at the same time as a clear, the bit will remain set (which causes another interrupt).

| Bits | Name | Description |
|------|------------|--|
| 3 | limact_int | When set, a limited active ready event has occurred. The setting of limact_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field) |
| 2 | onepps_int | When set, a onepps event has occurred. The setting of onepps_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field) |
| 1 | ctw_int | When set, a central timewheel event has occurred. The setting of ctw_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field) |
| 0 | ftw_int | When set, a fast timewheel event has occurred. The setting of ftw_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field) |

1.3.66 PM_MODE_CFG0

Power Mode Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_MODE_CFG0: 0x40004391

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | lpa_cycles | | | | | | | |

This register controls settings for the low power modes.

Register Segment: 1

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | lpa_cycles[7:0] | A setting of N causes (N+1) cycles to execute during each burst |

1.3.67 PM_MODE_CFG1

Power Mode Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_MODE_CFG1: 0x40004392

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|------|---------|--------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | NA:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | NA | R | R |
| Name | | | | | limact_ie | | lpa_fie | lpa_en |

This register controls settings for the low power modes.

Register Segment: 1

| Bits | Name | Description |
|------|-----------|---|
| 3 | limact_ie | Setting this bit will issue an interrupt when the system can return from limited active to fully active mode. To reliably generate the interrupt, this bit should be set prior to entering idle mode. |
| 1 | lpa_fie | When clear, interrupts are held off until next burst. This increases average interrupt latency, as compared to an active mode baseline design with identical throughput. When set, interrupts return the system to active mode, the on-time counter is reset, and the system will execute at least N cycles. |
| 0 | lpa_en | When set, LPA mode is enabled. LPA mode is compatible with all global power modes. If standby mode is specified, it is interpreted as an early return to standby, and the LPA scheduler will wake the system on the original schedule. If idle, sleep, or hibernate modes are specified, LPA is temporarily paused and resumed upon wakeup. Clearing this bit immediately disables LPA. |

1.3.68 PM_MODE_CSR

Power Mode Control/Status Register

Reset: Reset Signals Listed Below

Register : Address

PM_MODE_CSR: 0x40004393

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|-----------------|------------------|------------|-------------------|---------|---|---|
| SW Access:Reset | R/WC:1 | R:0 | R:0 | R/WOC:0 | R:1 | R/W:000 | | |
| HW Access | W | W | W | R | W | R/W | | |
| Name | nonret_rst | limact_mod e | test_domain s | reactivate | pwrup_puls e_q | lp_mode | | |

This register controls settings for the global power mode.

Register Segment: 1

| Bits | Name | Description |
|------|---------------|---|
| 7 | nonret_rst | Persistent status bit that indicates a non-retention reset occurred for some chip registers. This bit is preset high by any chip reset, and it is cleared whenever the register is written. When the system automatically resets non-retention registers (such as when returning from low power modes or a reactivation), this field is set high to indicate some register state has changed. Sticky (whole field) |
| 6 | limact_mode | When set, the chip is in limited active mode. Some subsystems and domains are unavailable in this mode. A reactivation is required to return the chip to active mode. |
| 5 | test_domains | When set, domains in PM_AVAIL_CR* react immediately, even if they are part of the delayed activation class. The sequencer is not used, and only power to the domain is immediately enabled. Isolation is not removed and the PM_AVAIL_SR* status bits do not reflect the actual state until a reactivation. State retention is not guaranteed. A normal reactivation is required to restore the system to normal function. This is a diagnostic feature that is not intended for customer usage, and this bit can only be changed in test mode. |
| 4 | reactivate | Setting this bit reactivates subsystems with pending availability. This is used to transition from limited active to active mode or to initiate the delayed activation procedure after change(s) to PM_AVAIL* register(s). The reactivation process simulates a transition from sleep to active mode. During the simulated transition, user clocks are stopped. After completion, the system is in active mode regardless of the LP_MODE setting. This bit always reads as zero. |
| 3 | pwrup_pulse_q | When set, indicates that the chip is internally waiting for the hibernate/sleep regulator to stabilize. The chip will ignore LP requests for idle, sleep, and hibernate modes until the regulator is stable. |
| 2:0 | lp_mode[2:0] | Sets the global power mode. Although technically illegal, 3'b111 is same as MODE_HIBTIMERS. 3'b101 is reserved for hibernate+reboot. |

[See Table 1-76.](#)

Reset Table

| resetsignal | field(s) |
|-------------|----------|
|-------------|----------|

1.3.68 PM_MODE_CSR (continued)

Reset Table

System reset for retention flops
 [reset_all_retention] lp_mode[2:0], pwrup_pulse_q, reactivate, test_domains, limact_mode

Domain reset for non-retention flops
 [reset_all_nonretention] nonret_rst
]

Table 1-76. Bit field encoding: mode_enum

| Value | Name | Description |
|--------|----------------|----------------------|
| 3'b000 | MODE_ACTIVE | Active mode |
| 3'b001 | MODE_STANDBY | Standby mode |
| 3'b010 | MODE_IDLE | Idle mode |
| 3'b011 | MODE_SLEEP | Sleep mode |
| 3'b100 | MODE_HIBERNATE | Hibernate mode |
| 3'b110 | MODE_HIBTIMERS | Hibernate+timewheels |

1.3.69 PM_USB_CR0

USB Power Mode Control Register 0

Reset: Reset Signals Listed Below

Register : Address

PM_USB_CR0: 0x40004394

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------------------|--------------|----------------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:1 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | fsusbio_pd_pullup_n | fsusbio_pd_n | fsusbio_ref_en |

This register controls settings for USB low power mode.

Register Segment: 1

| Bits | Name | Description |
|------|---------------------|--|
| 2 | fsusbio_pd_pullup_n | USB IO pad pullup enable. When set, the USBIO pad pullups can be used. When clear, the pullups are forced off. The pullups cannot be enabled until the appropriate supply is available. For example, if the USB regulator is configured, it must be stable before enabling the pullup or it may result in output glitches. The general guideline is to wait at least 2us after setting fsusbio_pd_n=1 before setting this field. This requirement is in addition to the reference settling time (if applicable). |
| 1 | fsusbio_pd_n | USB IO pad enable. When set, the USBIO pads can be used. When clear, the USBIO pads latch their previous settings and powerdown. This field must be high to use the pads for USB or GPIO modes. If USB is unavailable (wounded) the pads will ignore this setting and will remain disabled. |
| 0 | fsusbio_ref_en | USB IO pad receiver and regulator reference enable. The reference is required when using the USBIO pins for USB signaling. It is used by the differential receiver and USB regulator. The reference is NOT required when using the USBIO pins for GPIO signaling. Before enabling USB signaling in {USB_CR0}, enable this bit and allow the reference to settle. Settling time is max(1us after enabling, 40us after power restored). Power loss occurs during reset or when entering a deep low power mode (idle, sleep, or hibernate). Power is considered restored when reset deasserts or when the core supply reaches the PRES threshold after a wakeup. This field is retained so that if the core supply is kept up (eg. idle or sleep), the delay can be measured from the wakeup event. |

Reset Table

| resetsignal | field(s) |
|---|---------------------------------|
| System reset for retention flops [reset_all_retention] | fsusbio_ref_en, fsusbio_pd_n |
| Domain reset for non-retention flops [reset_all_nonretention] | fsusbio_pd_pullup_n |

1.3.70 PM_WAKEUP_CFG0

Power Mode Wakeup Mask Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WAKEUP_CFG0: 0x40004398

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|----------------|------------|----------|----------|-----------|---------|----------|
| SW Access:Reset | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | mask_sleep | mask_clkp m | mask_boost | mask_cpu | mask_i2c | mask_picu | mask_tc | mask_int |

This register masks the power mode wakeup sources.

Register Segment: 1

| Bits | Name | Description |
|------|------------|--|
| 7 | mask_sleep | When set, the PM CTW and PM 1PPS (RTC) can return the chip to active mode. |
| 6 | mask_clkpm | When set, the PM FTW can return the chip to active mode. |
| 5 | mask_boost | When set, boost undervoltage can return the chip to active mode. |
| 4 | mask_cpu | When set, a CPU bus transaction can return the chip to active mode. |
| 3 | mask_i2c | When set, I2C can return the chip to active mode. |
| 2 | mask_picu | When set, the PICU can return the chip to active mode. |
| 1 | mask_tc | When set, the Test Controller can return the chip to active mode. |
| 0 | mask_int | When set, on-chip interrupts can return the chip to active mode. |

1.3.71 PM_WAKEUP_CFG1

Power Mode Wakeup Mask Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WAKEUP_CFG1: 0x40004399

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| SW Access:Reset | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | mask_cmp7 | mask_cmp6 | mask_cmp5 | mask_cmp4 | mask_cmp3 | mask_cmp2 | mask_cmp1 | mask_cmp0 |

This register masks the power mode wakeup sources.

Register Segment: 1

| Bits | Name | Description |
|------|-----------|--|
| 7 | mask_cmp7 | Reserved for comparator 7 |
| 6 | mask_cmp6 | Reserved for comparator 6 |
| 5 | mask_cmp5 | Reserved for comparator 5 |
| 4 | mask_cmp4 | Reserved for comparator 4 |
| 3 | mask_cmp3 | When set, comparator 3 can return the chip to active mode. |
| 2 | mask_cmp2 | When set, comparator 2 can return the chip to active mode. |
| 1 | mask_cmp1 | When set, comparator 1 can return the chip to active mode. |
| 0 | mask_cmp0 | When set, comparator 0 can return the chip to active mode. |

1.3.72 PM_WAKEUP_CFG2

Power Mode Wakeup Mask Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WAKEUP_CFG2: 0x4000439A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|----------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:1 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | mask_lcd |

This register masks the power mode wakeup sources.

Register Segment: 1

| Bits | Name | Description |
|------|----------|---|
| 0 | mask_lcd | When set, LCD can return the chip to active mode. |

1.3.73 PM_ACT_CFG0

Active Power Mode Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG0: 0x400043A0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|-----------------|-----------|--------|------------|--------|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:1 | R/W:0 | NA:000 | | |
| HW Access | R | R | R | R | R | NA | | |
| Name | en_delay | en_udbarra y | en_imo36m | en_imo | en_clk_spc | | | |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|-------------|--|
| 7 | en_delay | Global enable for clkdist delay line. For Aclk's to be running this bit must be set, When this bit is LOW Aclk's can't toggle. |
| 6 | en_udbarray | Global enable for UDB array. |
| 5 | en_imo36m | Enable IMO SPC clock source. This also internally enables the IMO, since it is required for the 36MHz IMO to function. |
| 4 | en_imo | Enable IMO clock source. Any wakeup event will set this bit. |
| 3 | en_clk_spc | Enable clk_spc. This also internally enables the 36MHz IMO (similar to en_imo36m), since this is required for the SPC to function. |

1.3.74 PM_ACT_CFG1

Active Power Mode Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG1: 0x400043A1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_clk_a | | | |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|---------------|-------------------|
| 3:0 | en_clk_a[3:0] | Enable clk_a[3:0] |

1.3.75 PM_ACT_CFG2

Active Power Mode Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG2: 0x400043A2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | en_clk_d | | | | | | | |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|---------------|-------------------|
| 7:0 | en_clk_d[7:0] | Enable clk_d[7:0] |

1.3.76 PM_ACT_CFG3

Active Power Mode Configuration Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG3: 0x400043A3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_timer | | | |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|---------------|------------------------|
| 3:0 | en_timer[3:0] | Enable timer/counters. |

1.3.77 PM_ACT_CFG4

Active Power Mode Configuration Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG4: 0x400043A4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_opamp | | | |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|---------------|-------------------------------------|
| 3:0 | en_opamp[3:0] | Enable analog linear output buffer. |

1.3.78 PM_ACT_CFG5

Active Power Mode Configuration Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG5: 0x400043A5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|------|--------|------|--------|------|----------|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | en_emif | | en_lcd | | en_i2c | | en_fsusb |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|----------|---|
| 6 | en_emif | Enable EMIF |
| 4 | en_lcd | Enable LCD. |
| 2 | en_i2c | Enable I2C block(s). Populated subsystems are counted from the LSB. |
| 0 | en_fsusb | Enable FS-USB. |

1.3.79 PM_ACT_CFG6

Active Power Mode Configuration Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG6: 0x400043A6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|--------|--------|---|---|--------|
| SW Access:Reset | NA:000 | | | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | NA | | | R | NA | | | R |
| Name | | | | en_dfb | | | | en_can |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|--------|---|
| 4 | en_dfb | Enable DFB(s). Populated subsystems are counted from the LSB. |
| 0 | en_can | Enable CAN block(s). Populated subsystems are counted from the LSB. |

1.3.80 PM_ACT_CFG7

Active Power Mode Configuration Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG7: 0x400043A7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_cmp | | | |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|-------------|---|
| 3:0 | en_cmp[3:0] | Enable comparator(s). Populated subsystems are counted from the LSB, for example bit 0 corresponds to comparator 0. |

1.3.81 PM_ACT_CFG8

Active Power Mode Configuration Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG8: 0x400043A8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_dac | | | |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|-------------|---|
| 3:0 | en_dac[3:0] | Enable DAC block(s). Populated subsystems are counted from the LSB. |

1.3.82 PM_ACT_CFG9

Active Power Mode Configuration Register 9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG9: 0x400043A9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_swcap | | | |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|---------------|---|
| 3:0 | en_swcap[3:0] | Enable switchcap block(s). Populated subsystems are counted from the LSB, for example bit 0 corresponds to switchcap block 0. |

1.3.83 PM_ACT_CFG10

Active Power Mode Configuration Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG10: 0x400043AA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|----------------|--------|---|---|--------|
| SW Access:Reset | NA:000 | | | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | NA | | | R | NA | | | R |
| Name | | | | en_dsm_channel | | | | en_dec |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|----------------|--|
| 4 | en_dsm_channel | Enable delta-sigma modulator ADC channel. Note: set the appropriate enables in the analog interface prior to setting this global enable for the channel. |
| 0 | en_dec | Enable decimator(s). Populated subsystems are counted from the LSB. |

1.3.84 PM_ACT_CFG11

Active Power Mode Configuration Register 11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG11: 0x400043AB

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|------------|-------|---|--------|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | NA:00 | | R/W:00 | |
| HW Access | NA | | R | R | NA | | R | |
| Name | | | en_refbufr | en_refbufl | | | en_sar | |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|-------------|---|
| 5 | en_refbufr | Enable RIGHT analog reference buffer (refbufr) |
| 4 | en_refbufl | Enable LEFT analog reference buffer (refbufl) |
| 1:0 | en_sar[1:0] | Enable SAR(s). Populated subsystems are counted from the LSB. |

1.3.85 PM_ACT_CFG12

Active Power Mode Configuration Register 12

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG12: 0x400043AC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------|----------|---|---|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:1111 | | | |
| HW Access | NA | | | R | R | | | |
| Name | | | | en_ee | en_fm | | | |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|------------|--|
| 4 | en_ee | Enable EEPROM. Re-enabling an EEPROM macro takes 5us. During this time, the EE will not acknowledge a PHUB request. |
| 3:0 | en_fm[3:0] | Enable flash. Active flash macros consume current, but re-enabling a disabled flash macro takes 5us. If the CPU attempts to fetch out of the macro during that time, it will be stalled. This bit allows the flash to be enabled even if the CPU is disabled, which allows a quicker return to code execution. To avoid a deadlock where the CPU attempts to fetch out of a disabled macro, the flash macro will ignore this bit if the CPU is enabled in user mode. During test mode, the flash CAN be turned off independently from the CPU. |

1.3.86 PM_ACT_CFG13

Active Power Mode Configuration Register 13

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG13: 0x400043AD

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---------|-----------|----------|
| SW Access:Reset | NA:0000 | | | | R/W:1 | R/W:1 | R/W:1 | R/W:1 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | en_ports | en_picu | en_sysmem | en_anaif |

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|-----------|--|
| 3 | en_ports | Enable ports. This must be enabled to read/write registers in the port logic. |
| 2 | en_picu | Enable PICU. This must be enabled to read/write registers in the PICU. Configured wakeups will continue to function if the PICU is disabled, but the interface must be enabled to clear the interrupt condition. |
| 1 | en_sysmem | Enable SYSTEMEM. This must be enabled to read/write the SYSTEMEM. |
| 0 | en_anaif | Enable analog interface. This must be enabled to read/write registers in the analog interface. |

1.3.87 PM_STBY_CFG0

Standby Power Mode Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG0: 0x400043B0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|-----------------|-----------|--------|------------|--------|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:000 | | |
| HW Access | R | R | R | R | R | NA | | |
| Name | en_delay | en_udbarra y | en_imo36m | en_imo | en_clk_spc | | | |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|-------------|--|
| 7 | en_delay | Global enable for clkdist delay line. For Aclk's to be running this bit must be set, When this bit is LOW Aclk's can't toggle. |
| 6 | en_udbarray | Global enable for UDB array. |
| 5 | en_imo36m | Enable IMO SPC clock source. This also internally enables the IMO, since it is required for the 36MHz IMO to function. |
| 4 | en_imo | Enable IMO clock source. Any wakeup event will set this bit. |
| 3 | en_clk_spc | Enable clk_spc. This also internally enables the 36MHz IMO (similar to en_imo36m), since this is required for the SPC to function. |

1.3.88 PM_STBY_CFG1

Standby Power Mode Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG1: 0x400043B1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_clk_a | | | |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|---------------|-------------------|
| 3:0 | en_clk_a[3:0] | Enable clk_a[3:0] |

1.3.89 PM_STBY_CFG2

Standby Power Mode Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG2: 0x400043B2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | en_clk_d | | | | | | | |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|---------------|-------------------|
| 7:0 | en_clk_d[7:0] | Enable clk_d[7:0] |

1.3.90 PM_STBY_CFG3

Standby Power Mode Configuration Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG3: 0x400043B3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_timer | | | |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|---------------|------------------------|
| 3:0 | en_timer[3:0] | Enable timer/counters. |

1.3.91 PM_STBY_CFG4

Standby Power Mode Configuration Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG4: 0x400043B4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_opamp | | | |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|---------------|-------------------------------------|
| 3:0 | en_opamp[3:0] | Enable analog linear output buffer. |

1.3.92 PM_STBY_CFG5

Standby Power Mode Configuration Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG5: 0x400043B5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|------|--------|------|--------|------|----------|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | en_emif | | en_lcd | | en_i2c | | en_fsusb |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|----------|---|
| 6 | en_emif | Enable EMIF |
| 4 | en_lcd | Enable LCD. |
| 2 | en_i2c | Enable I2C block(s). Populated subsystems are counted from the LSB. |
| 0 | en_fsusb | Enable FS-USB. |

1.3.93 PM_STBY_CFG6

Standby Power Mode Configuration Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG6: 0x400043B6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|--------|--------|---|---|--------|
| SW Access:Reset | NA:000 | | | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | NA | | | R | NA | | | R |
| Name | | | | en_dfb | | | | en_can |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|--------|---|
| 4 | en_dfb | Enable DFB(s). Populated subsystems are counted from the LSB. |
| 0 | en_can | Enable CAN block(s). Populated subsystems are counted from the LSB. |

1.3.94 PM_STBY_CFG7

Standby Power Mode Configuration Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG7: 0x400043B7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_cmp | | | |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|-------------|---|
| 3:0 | en_cmp[3:0] | Enable comparator(s). Populated subsystems are counted from the LSB, for example bit 0 corresponds to comparator 0. |

1.3.95 PM_STBY_CFG8

Standby Power Mode Configuration Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG8: 0x400043B8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_dac | | | |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|-------------|---|
| 3:0 | en_dac[3:0] | Enable DAC block(s). Populated subsystems are counted from the LSB. |

1.3.96 PM_STBY_CFG9

Standby Power Mode Configuration Register 9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG9: 0x400043B9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | en_swcap | | | |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|---------------|---|
| 3:0 | en_swcap[3:0] | Enable switchcap block(s). Populated subsystems are counted from the LSB, for example bit 0 corresponds to switchcap block 0. |

1.3.97 PM_STBY_CFG10

Standby Power Mode Configuration Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG10: 0x400043BA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|----------------|--------|---|---|--------|
| SW Access:Reset | NA:000 | | | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | NA | | | R | NA | | | R |
| Name | | | | en_dsm_channel | | | | en_dec |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|----------------|--|
| 4 | en_dsm_channel | Enable delta-sigma modulator ADC channel. Note: set the appropriate enables in the analog interface prior to setting this global enable for the channel. |
| 0 | en_dec | Enable decimator(s). Populated subsystems are counted from the LSB. |

1.3.98 PM_STBY_CFG11

Standby Power Mode Configuration Register 11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG11: 0x400043BB

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|------------|-------|---|--------|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | NA:00 | | R/W:00 | |
| HW Access | NA | | R | R | NA | | R | |
| Name | | | en_refbufr | en_refbufl | | | en_sar | |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|-------------|---|
| 5 | en_refbufr | Enable RIGHT analog reference buffer (refbufr) |
| 4 | en_refbufl | Enable LEFT analog reference buffer (refbufl) |
| 1:0 | en_sar[1:0] | Enable SAR(s). Populated subsystems are counted from the LSB. |

1.3.99 PM_STBY_CFG12

Standby Power Mode Configuration Register 12

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG12: 0x400043BC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------|----------|---|---|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0000 | | | |
| HW Access | NA | | | R | R | | | |
| Name | | | | en_ee | en_fm | | | |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|------------|--|
| 4 | en_ee | Enable EEPROM. Re-enabling an EEPROM macro takes 5us. During this time, the EE will not acknowledge a PHUB request. |
| 3:0 | en_fm[3:0] | Enable flash. Active flash macros consume current, but re-enabling a disabled flash macro takes 5us. If the CPU attempts to fetch out of the macro during that time, it will be stalled. This bit allows the flash to be enabled even if the CPU is disabled, which allows a quicker return to code execution. To avoid a deadlock where the CPU attempts to fetch out of a disabled macro, the flash macro will ignore this bit if the CPU is enabled in user mode. During test mode, the flash CAN be turned off independently from the CPU. |

1.3.100 PM_STBY_CFG13

Standby Power Mode Configuration Register 13

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG13: 0x400043BD

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---------|-----------|----------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:1 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | en_ports | en_picu | en_sysmem | en_anaif |

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

| Bits | Name | Description |
|------|-----------|--|
| 3 | en_ports | Enable ports. This must be enabled to read/write registers in the port logic. |
| 2 | en_picu | Enable PICU. This must be enabled to read/write registers in the PICU. Configured wakeups will continue to function if the PICU is disabled, but the interface must be enabled to clear the interrupt condition. |
| 1 | en_sysmem | Enable SYSTEMEM. This must be enabled to read/write the SYSTEMEM. |
| 0 | en_anaif | Enable analog interface. This must be enabled to read/write registers in the analog interface. |

1.3.101 PM_AVAIL_CR0

Power Mode Available Subsystem Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR0: 0x400043C0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:1111 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | avail_fm | | | |

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

| Bits | Name | Description |
|------|---------------|---|
| 3:0 | avail_fm[3:0] | Each set bit requests a flash macro be available. Reactivation is delayed. Macro 0 can only be disabled during test_mode. |

1.3.102 PM_AVAIL_CR1

Power Mode Available Subsystem Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR1: 0x400043C1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|--------------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:1111 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | avail_sysmem | | | |

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

| Bits | Name | Description |
|------|-------------------|--|
| 3:0 | avail_sysmem[3:0] | Each set bit requests a sysmem macro be available. Reactivation is delayed. Populated subsystems are counted from the LSB. |

1.3.103 PM_AVAIL_CR2

Power Mode Available Subsystem Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR2: 0x400043C2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|--------|---|---|----------|
| SW Access:Reset | NA:000 | | | R/W:1 | NA:000 | | | R/W:1 |
| HW Access | NA | | | R | NA | | | R |
| Name | | | | avail_udb | | | | avail_ee |

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

| Bits | Name | Description |
|------|-----------|--|
| 4 | avail_udb | Each set bit requests a UDB bank be available. Reactivation is delayed. If user needs UDB never clear this bit. If user clears this bit, then user has to reconfigure the UDB. |
| 0 | avail_ee | Each set bit requests a EEPROM macro be available. Reactivation is delayed. |

1.3.104 PM_AVAIL_CR3

Power Mode Available Subsystem Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR3: 0x400043C3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------------------|--------|---|---|-----------|
| SW Access:Reset | NA:000 | | | R/W:1 | NA:000 | | | R/W:1 |
| HW Access | NA | | | R | NA | | | R |
| Name | | | | avail_sysmemtrace | | | | avail_dfb |

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

| Bits | Name | Description |
|------|-------------------|---|
| 4 | avail_sysmemtrace | Each set bit requests a trace memory be available. Reactivation is delayed. |
| 0 | avail_dfb | Each set bit requests a DFB be available. Reactivation is delayed. |

1.3.105 PM_AVAIL_CR4

Power Mode Available Subsystem Control Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR4: 0x400043C4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|------|------------|------|-----------|
| SW Access:Reset | NA:000 | | | R/W:1 | NA:0 | R/W:1 | NA:0 | R/W:1 |
| HW Access | NA | | | R | NA | R | NA | R |
| Name | | | | avail_i2c | | avail_main | | avail_spc |

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

| Bits | Name | Description |
|------|------------|---|
| 4 | avail_i2c | When set, requests I2C be available. Reactivation is delayed. |
| 2 | avail_main | When set, requests main domain be available. Can only be disabled in test mode. There is no isolation from main to UDB, so also disable avail_udb to avoid static current. Reactivation is delayed. |
| 0 | avail_spc | When set, requests SPC be available. Reactivation is delayed. |

1.3.106 PM_AVAIL_CR5

Power Mode Available Subsystem Control Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR5: 0x400043C5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|-------------------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:1 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | avail_dsm_channel |

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

| Bits | Name | Description |
|------|-------------------|---|
| 0 | avail_dsm_channel | Each set bit requests a delsig channel be available. Reactivation is immediate. |

1.3.107 PM_AVAIL_CR6

Power Mode Available Subsystem Control Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR6: 0x400043C6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|--------------------|-------|---|-------------------|-------------------|
| SW Access:Reset | NA:000 | | | R/W:1 | NA:00 | | R/W:1 | R/W:1 |
| HW Access | NA | | | R | NA | | R | R |
| Name | | | | avail_anami sc2 | | | avail_anapu mp | avail_anami sc |

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

| Bits | Name | Description |
|------|----------------|--|
| 4 | avail_anamisc2 | When set, requests miscellaneous analog (group 2) be available. This register is a placeholder and presently has no fanout. Reactivation is immediate. |
| 1 | avail_anapump | When set, requests analog pump be available. Reactivation is immediate. |
| 0 | avail_anamisc | When set, requests miscellaneous analog be available. Reactivation is immediate. |

1.3.108 PM_AVAIL_SR0

Power Mode Available Subsystem Status Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR0: 0x400043D0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R:1111 | | | |
| HW Access | NA | | | | W | | | |
| Name | | | | | avail_fm | | | |

This register indicates whether a subsystem is available or not.

| Bits | Name | Description |
|------|---------------|--|
| 3:0 | avail_fm[3:0] | Each set bit indicates an available flash macro. |

1.3.109 PM_AVAIL_SR1

Power Mode Available Subsystem Status Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR1: 0x400043D1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|--------------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R:1111 | | | |
| HW Access | NA | | | | W | | | |
| Name | | | | | avail_sysmem | | | |

This register indicates whether a subsystem is available or not.

| Bits | Name | Description |
|------|-------------------|--|
| 3:0 | avail_sysmem[3:0] | Each set bit requests a sysmem macro be available. Reactivation is delayed. Populated subsystems are counted from the LSB. |

1.3.110 PM_AVAIL_SR2

Power Mode Available Subsystem Status Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR2: 0x400043D2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|--------|---|---|----------|
| SW Access:Reset | NA:000 | | | R:1 | NA:000 | | | R:1 |
| HW Access | NA | | | W | NA | | | W |
| Name | | | | avail_udb | | | | avail_ee |

This register indicates whether a subsystem is available or not.

| Bits | Name | Description |
|------|-----------|---|
| 4 | avail_udb | Each set bit indicates an available UDB bank. |
| 0 | avail_ee | Each set bit indicates an available EEPROM macro. |

1.3.111 PM_AVAIL_SR3

Power Mode Available Subsystem Status Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR3: 0x400043D3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------------------|--------|---|---|-----------|
| SW Access:Reset | NA:000 | | | R:1 | NA:000 | | | R:1 |
| HW Access | NA | | | W | NA | | | W |
| Name | | | | avail_sysmemtrace | | | | avail_dfb |

This register indicates whether a subsystem is available or not.

| Bits | Name | Description |
|------|-------------------|---|
| 4 | avail_sysmemtrace | Each set bit indicates an available trace memory. |
| 0 | avail_dfb | Each set bit indicates an available DFB. |

1.3.112 PM_AVAIL_SR4

Power Mode Available Subsystem Status Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR4: 0x400043D4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|------|------------|------|-----------|
| SW Access:Reset | NA:000 | | | R:1 | NA:0 | R:1 | NA:0 | R:1 |
| HW Access | NA | | | W | NA | W | NA | W |
| Name | | | | avail_i2c | | avail_main | | avail_spc |

This register indicates whether a subsystem is available or not.

| Bits | Name | Description |
|------|------------|-------------------------------------|
| 4 | avail_i2c | When set, I2C is available. |
| 2 | avail_main | When set, main domain is available. |
| 0 | avail_spc | When set, SPC is available. |

1.3.113 PM_AVAIL_SR5

Power Mode Available Subsystem Status Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR5: 0x400043D5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|-------------------|
| SW Access:Reset | NA:0000000 | | | | | | | R:1 |
| HW Access | NA | | | | | | | W |
| Name | | | | | | | | avail_dsm_channel |

This register indicates whether a subsystem is available or not.

| Bits | Name | Description |
|------|-------------------|---|
| 0 | avail_dsm_channel | Each set bit indicates an available detsig channel. |

1.3.114 PM_AVAIL_SR6

Power Mode Available Subsystem Status Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR6: 0x400043D6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|--------------------|-------|---|-------------------|-------------------|
| SW Access:Reset | NA:000 | | | R:1 | NA:00 | | R:1 | R:1 |
| HW Access | NA | | | W | NA | | W | W |
| Name | | | | avail_anami sc2 | | | avail_anapu mp | avail_anami sc |

This register indicates whether a subsystem is available or not.

| Bits | Name | Description |
|------|----------------|--|
| 4 | avail_anamisc2 | When set, miscellaneous analog (group 2) is available. |
| 1 | avail_anapump | When set, analog pump is available. |
| 0 | avail_anamisc | When set, miscellaneous analog is available. |

1.3.115 PICU[0..15]_INTTYPE[0..7]

Port Interrupt Control Type Register

Reset: System reset for always on flops [reset_all_alwayson]

Register : Address

| | |
|-----------------------------|-----------------------------|
| PICU0_INTTYPE0: 0x40004500 | PICU0_INTTYPE1: 0x40004501 |
| PICU0_INTTYPE2: 0x40004502 | PICU0_INTTYPE3: 0x40004503 |
| PICU0_INTTYPE4: 0x40004504 | PICU0_INTTYPE5: 0x40004505 |
| PICU0_INTTYPE6: 0x40004506 | PICU0_INTTYPE7: 0x40004507 |
| PICU1_INTTYPE0: 0x40004508 | PICU1_INTTYPE1: 0x40004509 |
| PICU1_INTTYPE2: 0x4000450A | PICU1_INTTYPE3: 0x4000450B |
| PICU1_INTTYPE4: 0x4000450C | PICU1_INTTYPE5: 0x4000450D |
| PICU1_INTTYPE6: 0x4000450E | PICU1_INTTYPE7: 0x4000450F |
| PICU2_INTTYPE0: 0x40004510 | PICU2_INTTYPE1: 0x40004511 |
| PICU2_INTTYPE2: 0x40004512 | PICU2_INTTYPE3: 0x40004513 |
| PICU2_INTTYPE4: 0x40004514 | PICU2_INTTYPE5: 0x40004515 |
| PICU2_INTTYPE6: 0x40004516 | PICU2_INTTYPE7: 0x40004517 |
| PICU3_INTTYPE0: 0x40004518 | PICU3_INTTYPE1: 0x40004519 |
| PICU3_INTTYPE2: 0x4000451A | PICU3_INTTYPE3: 0x4000451B |
| PICU3_INTTYPE4: 0x4000451C | PICU3_INTTYPE5: 0x4000451D |
| PICU3_INTTYPE6: 0x4000451E | PICU3_INTTYPE7: 0x4000451F |
| PICU4_INTTYPE0: 0x40004520 | PICU4_INTTYPE1: 0x40004521 |
| PICU4_INTTYPE2: 0x40004522 | PICU4_INTTYPE3: 0x40004523 |
| PICU4_INTTYPE4: 0x40004524 | PICU4_INTTYPE5: 0x40004525 |
| PICU4_INTTYPE6: 0x40004526 | PICU4_INTTYPE7: 0x40004527 |
| PICU5_INTTYPE0: 0x40004528 | PICU5_INTTYPE1: 0x40004529 |
| PICU5_INTTYPE2: 0x4000452A | PICU5_INTTYPE3: 0x4000452B |
| PICU5_INTTYPE4: 0x4000452C | PICU5_INTTYPE5: 0x4000452D |
| PICU5_INTTYPE6: 0x4000452E | PICU5_INTTYPE7: 0x4000452F |
| PICU6_INTTYPE0: 0x40004530 | PICU6_INTTYPE1: 0x40004531 |
| PICU6_INTTYPE2: 0x40004532 | PICU6_INTTYPE3: 0x40004533 |
| PICU6_INTTYPE4: 0x40004534 | PICU6_INTTYPE5: 0x40004535 |
| PICU6_INTTYPE6: 0x40004536 | PICU6_INTTYPE7: 0x40004537 |
| PICU12_INTTYPE0: 0x40004560 | PICU12_INTTYPE1: 0x40004561 |
| PICU12_INTTYPE2: 0x40004562 | PICU12_INTTYPE3: 0x40004563 |
| PICU12_INTTYPE4: 0x40004564 | PICU12_INTTYPE5: 0x40004565 |
| PICU12_INTTYPE6: 0x40004566 | PICU12_INTTYPE7: 0x40004567 |

1.3.115 PICU[0..15]_INTTYPE[0..7] (continued)

Register : Address

| | |
|-----------------------------|-----------------------------|
| PICU15_INTTYPE0: 0x40004578 | PICU15_INTTYPE1: 0x40004579 |
| PICU15_INTTYPE2: 0x4000457A | PICU15_INTTYPE3: 0x4000457B |
| PICU15_INTTYPE4: 0x4000457C | PICU15_INTTYPE5: 0x4000457D |
| PICU15_INTTYPE6: 0x4000457E | PICU15_INTTYPE7: 0x4000457F |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|---------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | INTTYPE | |

This register configures the type of interrupt for a pin. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

| Bits | Name | Description |
|------|--------------|---|
| 1:0 | INTTYPE[1:0] | This field configures the type of interrupt type enabled. |

[See Table 1-77.](#)

Table 1-77. Bit field encoding: INTTYPE_ENUM

| Value | Name | Description |
|-------|--------------|---|
| 2'b00 | DISABLE | Disable Interrupts for pin. |
| 2'b01 | RISING_EDGE | Enable Rising Edge Interrupts for pin. |
| 2'b10 | FALLING_EDGE | Enable Falling Edge Interrupts for pin. |
| 2'b11 | CHANGE_MODE | Enable Both Edge Interrupts for pin. |

@0x40004580 + [0..15 * 0x1]

1.3.116 PICU[0..15]_INTSTAT

Port Interrupt Control Status Register

Reset: System reset for always on flops [reset_all_alwayson]

Register : Address

| | |
|----------------------------|----------------------------|
| PICU0_INTSTAT: 0x40004580 | PICU1_INTSTAT: 0x40004581 |
| PICU2_INTSTAT: 0x40004582 | PICU3_INTSTAT: 0x40004583 |
| PICU4_INTSTAT: 0x40004584 | PICU5_INTSTAT: 0x40004585 |
| PICU6_INTSTAT: 0x40004586 | PICU12_INTSTAT: 0x4000458C |
| PICU15_INTSTAT: 0x4000458F | |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | RC:0 | RC:0 | RC:0 | RC:0 | RC:0 | RC:0 | RC:0 | RC:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | STAT7 | STAT6 | STAT5 | STAT4 | STAT3 | STAT2 | STAT1 | STAT0 |

This register provides information on the recently posted interrupts.

| Bits | Name | Description |
|------|--------------------------|---|
| 7 | Interrupt Status {STAT7} | Pin 7 Interrupt Status See Table 1-78. |
| 6 | Interrupt Status {STAT6} | Pin 6 Interrupt Status See Table 1-78. |
| 5 | Interrupt Status {STAT5} | Pin 5 Interrupt Status See Table 1-78. |
| 4 | Interrupt Status {STAT4} | Pin 4 Interrupt Status See Table 1-78. |
| 3 | Interrupt Status {STAT3} | Pin 3 Interrupt Status See Table 1-78. |
| 2 | Interrupt Status {STAT2} | Pin 2 Interrupt Status See Table 1-78. |
| 1 | Interrupt Status {STAT1} | Pin 1 Interrupt Status See Table 1-78. |
| 0 | Interrupt Status {STAT0} | Pin 0 Interrupt Status See Table 1-78. |

Table 1-78. Bit field encoding: INTSTAT_ENUM

| Value | Name | Description |
|-------|-------------|------------------------------------|
| 1'b1 | INT_PENDING | Indicates an interrupt is pending. |
| 1'b0 | NO_INT | Indicates no interrupt is pending. |

1.3.117 PICU[0..15]_SNAP

Port Interrupt Control Snap Shot Register

Reset: System reset for always on flops [reset_all_alwayson]

Register : Address

PICU0_SNAP: 0x40004590

PICU1_SNAP: 0x40004591

PICU2_SNAP: 0x40004592

PICU3_SNAP: 0x40004593

PICU4_SNAP: 0x40004594

PICU5_SNAP: 0x40004595

PICU6_SNAP: 0x40004596

PICU12_SNAP: 0x4000459C

PICU15_SNAP: 0x4000459F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | SNAPSHOT | | | | | | | |

This register provides information on the state of input pins at recent read to Status register. An exception is this register will not be updated when status register is read with DISABLE_COR or CORD bit in MLOGIC.DEBUG register set

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | SNAPSHOT[7:0] | Contains input pin values at recent read to status register |

@0x400045a0 + [0..15 * 0x1]

1.3.118 PICU[0..15]_DISABLE_COR

Disable Status Register Clear on Read Feature

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

- PICU0_DISABLE_COR: 0x400045A0
- PICU1_DISABLE_COR: 0x400045A1
- PICU2_DISABLE_COR: 0x400045A2
- PICU3_DISABLE_COR: 0x400045A3
- PICU4_DISABLE_COR: 0x400045A4
- PICU5_DISABLE_COR: 0x400045A5
- PICU6_DISABLE_COR: 0x400045A6
- PICU12_DISABLE_COR: 0x400045AC
- PICU15_DISABLE_COR: 0x400045AF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|-----------------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | DISABLE_C OR |

This register is provided to disable the clear on read feature of Status Register. Either this register bit or CORD bit in MLOGIC.DEBUG register can disable the clear on read feature of status register. The interrupt will be cleared when both DISABLE_COR is 1'b0, CORD bit in MLOGIC.DEBUG register is 1'b0 and there is a status register read. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

| Bits | Name | Description |
|------|-------------|--|
| 0 | DISABLE_COR | 1'b0: Status Register is Clear On Read. 1'b1: Disable the Clear on Read feature of Status Register. |

1.3.119 DAC[0..3]_TR

DAC Block Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_TR: 0x40004608

DAC1_TR: 0x40004609

DAC2_TR: 0x4000460A

DAC3_TR: 0x4000460B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | tr | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|--------------------|
| 7:0 | tr[7:0] | 8 Calibration bits |

1.3.120 NPUMP_DSM_TR0

Delta Sigma Modulator (DSM) Negative Pump Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NPUMP_DSM_TR0: 0x40004610

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|----------------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | npump_dsm_trim | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------------------|--|
| 1:0 | npump_dsm_trim[1:0] | Delta Sigma Modulator (DSM) Negative Pump Trim |

1.3.121 NPUMP_SC_TR0

Switched Cap Negative Pump Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NPUMP_SC_TR0: 0x40004611

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|---------------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | npump_sc_trim | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------------|---------------------------------|
| 1:0 | npump_sc_trim[1:0] | Switched Cap Negative Pump Trim |

1.3.122 NPUMP_OPAMP_TR0

Analog Linear Output Buffer (OPAMP) Negative Pump Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NPUMP_OPAMP_TR0: 0x40004612

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|------------------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | npump_opamp_trim | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------------|--|
| 1:0 | npump_opamp_trim[1:0] | Analog Linear Output Buffer (OPAMP) Negative Pump Trim |

1.3.123 SAR[0..1]_TR0

SAR trim register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_TR0: 0x40004614

SAR1_TR0: 0x40004616

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|----------|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:000 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | trimunit | cap_trim | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------------|---|
| 3 | trimunit | trim See Table 1-80. |
| 2:0 | cap_trim[2:0] | Capacitance Trim See Table 1-79. |

Table 1-79. Bit field encoding: SAR_CAP_TRIM_ENUM

| Value | Name | Description |
|-------|----------------|---|
| 3'h0 | SAR_CAP_TRIM_0 | decrease attenuation capacitor by 0 |
| 3'h1 | SAR_CAP_TRIM_1 | decrease attenuation capacitor by 0.5 LSB |
| 3'h2 | SAR_CAP_TRIM_2 | decrease attenuation capacitor by 2*0.5 LSB = 1 LSB |
| 3'h3 | SAR_CAP_TRIM_3 | decrease attenuation capacitor by 3*0.5 LSB = 1.5 LSB |
| 3'h4 | SAR_CAP_TRIM_4 | decrease attenuation capacitor by 4*0.5 LSB = 2 LSB |
| 3'h5 | SAR_CAP_TRIM_5 | decrease attenuation capacitor by 5*0.5 LSB = 2.5 LSB |
| 3'h6 | SAR_CAP_TRIM_6 | decrease attenuation capacitor by 6*0.5 LSB = 3.0 LSB |
| 3'h7 | SAR_CAP_TRIM_7 | decrease attenuation capacitor by 7*0.5 LSB = 3.5 LSB |

Table 1-80. Bit field encoding: SAR_TRIMUNIT_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------|
| 1'b0 | SAR_TRIMUNIT_0 | default attenuation cap |
| 1'b1 | SAR_TRIMUNIT_1 | Increase by 6fF |

1.3.124 OPAMP[0..3]_TR0

Analog Output Buffer Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_TR0: 0x40004620

OPAMP1_TR0: 0x40004622

OPAMP2_TR0: 0x40004624

OPAMP3_TR0: 0x40004626

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------------|---|---|---|---|
| SW Access:Reset | NA:000 | | | R/W:00000 | | | | |
| HW Access | NA | | | R | | | | |
| Name | | | | offset_trim | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------------|--|
| 4:0 | offset_trim[4:0] | Offset Trim: 420uV typical step size; +/- 6.8mV offset trimmable range |

1.3.125 OPAMP[0..3]_TR1

Analog Output Buffer Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_TR1: 0x40004621

OPAMP1_TR1: 0x40004623

OPAMP2_TR1: 0x40004625

OPAMP3_TR1: 0x40004627

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|------------------------------|
| 7:0 | RSVD[7:0] | Reserved for OPAMP expansion |

1.3.126 CMP[0..3]_TR0

Comparator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_TR0: 0x40004630

CMP1_TR0: 0x40004632

CMP2_TR0: 0x40004634

CMP3_TR0: 0x40004636

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|---|---|---|---|
| SW Access:Reset | NA:000 | | | R/W:00000 | | | | |
| HW Access | NA | | | R | | | | |
| Name | | | | trimA | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 4:0 | trimA[4:0] | Sets the trim value to be added to the P-type load for offset calibration |

[See Table 1-81.](#)

Table 1-81. Bit field encoding: TRIMA_ENUM

| Value | Name | Description |
|-------|------------------|--|
| 5'h0 | TRIMA_0 | Does not add any offset. |
| 5'h1 | TRIMA_POS_SIDE_1 | Adds offset of ~1mV to the positive side |
| 5'h2 | TRIMA_POS_SIDE_2 | Adds offset of ~2mV to the positive side |
| 5'h3 | TRIMA_POS_SIDE_3 | Adds offset of ~3mV to the positive side |
| 5'h4 | TRIMA_POS_SIDE_4 | Adds offset of ~4mV to the positive side |
| 5'h5 | TRIMA_POS_SIDE_5 | Adds offset of ~5mV to the positive side |
| 5'h6 | TRIMA_POS_SIDE_6 | Adds offset of ~6mV to the positive side |
| 5'h7 | TRIMA_POS_SIDE_7 | Adds offset of ~7mV to the positive side |
| 5'h8 | TRIMA_POS_SIDE_8 | Adds offset of ~8mV to the positive side |
| 5'h10 | TRIMA_NEG_SIDE_1 | Adds offset of 0mV to the negative side |
| 5'h11 | TRIMA_NEG_SIDE_2 | Adds offset of ~1mV to the negative side |
| 5'h12 | TRIMA_NEG_SIDE_3 | Adds offset of ~2mV to the negative side |
| 5'h13 | TRIMA_NEG_SIDE_4 | Adds offset of ~3mV to the negative side |
| 5'h14 | TRIMA_NEG_SIDE_5 | Adds offset of ~4mV to the negative side |
| 5'h15 | TRIMA_NEG_SIDE_6 | Adds offset of ~5mV to the negative side |
| 5'h16 | TRIMA_NEG_SIDE_7 | Adds offset of ~6mV to the negative side |
| 5'h17 | TRIMA_NEG_SIDE_8 | Adds offset of ~7mV to the negative side |
| 5'h18 | TRIMA_NEG_SIDE_9 | Adds offset of ~8mV to the negative side |

1.3.127 CMP[0..3]_TR1

Comparator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_TR1: 0x40004631

CMP1_TR1: 0x40004633

CMP2_TR1: 0x40004635

CMP3_TR1: 0x40004637

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|---|---|---|---|
| SW Access:Reset | NA:000 | | | R/W:00000 | | | | |
| HW Access | NA | | | R | | | | |
| Name | | | | trimB | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 4:0 | trimB[4:0] | Sets the trim value to be added to the N-type load for offset calibration |

[See Table 1-82.](#)

Table 1-82. Bit field encoding: TRIMB_ENUM

| Value | Name | Description |
|-------|------------------|--|
| 5'h0 | TRIMB_0 | Does not add any offset. |
| 5'h1 | TRIMB_NEG_SIDE_1 | Adds offset of ~1mV to the negative side |
| 5'h2 | TRIMB_NEG_SIDE_2 | Adds offset of ~2mV to the negative side |
| 5'h3 | TRIMB_NEG_SIDE_3 | Adds offset of ~3mV to the negative side |
| 5'h4 | TRIMB_NEG_SIDE_4 | Adds offset of ~4mV to the negative side |
| 5'h5 | TRIMB_NEG_SIDE_5 | Adds offset of ~5mV to the negative side |
| 5'h6 | TRIMB_NEG_SIDE_6 | Adds offset of ~6mV to the negative side |
| 5'h7 | TRIMB_NEG_SIDE_7 | Adds offset of ~7mV to the negative side |
| 5'h8 | TRIMB_NEG_SIDE_8 | Adds offset of ~8mV to the negative side |
| 5'h10 | TRIMB_9 | Does not add any offset |
| 5'h11 | TRIMB_POS_SIDE_1 | Adds offset of ~1mV to the positive side |
| 5'h12 | TRIMB_POS_SIDE_2 | Adds offset of ~2mV to the positive side |
| 5'h13 | TRIMB_POS_SIDE_3 | Adds offset of ~3mV to the positive side |
| 5'h14 | TRIMB_POS_SIDE_4 | Adds offset of ~4mV to the positive side |
| 5'h15 | TRIMB_POS_SIDE_5 | Adds offset of ~5mV to the positive side |
| 5'h16 | TRIMB_POS_SIDE_6 | Adds offset of ~6mV to the positive side |
| 5'h17 | TRIMB_POS_SIDE_7 | Adds offset of ~7mV to the positive side |
| 5'h18 | TRIMB_POS_SIDE_8 | Adds offset of ~8mV to the positive side |

1.3.128 PWRSYS_HIB_TR0

Hibernate Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_HIB_TR0: 0x40004680

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:1111 | | | | R/W:0000 | | | |
| HW Access | R | | | | R | | | |
| Name | trim | | | | biasg | | | |

This register trims the hibernate regulator, which generates the vpwrka supply.

Register Segment: 0

| Bits | Name | Description |
|------|------------|---|
| 7:4 | trim[3:0] | Hibernate regulator trim. |
| 3:0 | biasg[3:0] | Hibernate regulator biasg tweak trim. During powerup hib/slp holdoff specified in PWRSYS_SLP_TR, this trim is internally forced to 4'b0001 until the hib/slp powerup holdoff is finished. This register can be written and will readback normally during the force condition (ie the force condition will not be seen during readback). After the force condition ends, the contents of this register will be applied to the hib/slp regulator. |

1.3.129 PWRSYS_HIB_TR1

Hibernate Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_HIB_TR1: 0x40004681

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|----------|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0 | R/W:000 | | | R/W:1011 | | | |
| HW Access | R | R | | | R | | | |
| Name | dis_hibernate | rbb_trim | | | enleg | | | |

This register trims the hibernate regulator and reverse body bias generator.

Register Segment: 0

| Bits | Name | Description |
|------|---------------|---|
| 7 | dis_hibernate | Setting this bit will disable hibernate mode. |
| 6:4 | rbb_trim[2:0] | Reverse body bias generator trim. |
| 3:0 | enleg[3:0] | Each set bit enables a current leg of the hibernate regulator for the keepalive supply. |

1.3.130 PWRSYS_I2C_TR

I2C Regulator Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_I2C_TR: 0x40004682

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---|---|-------|---|--------|---|
| SW Access:Reset | NA:0 | R/W:000 | | | NA:00 | | R/W:11 | |
| HW Access | NA | R | | | NA | | R | |
| Name | | restrim | | | | | trim | |

This register trims the I2C regulator.

Register Segment: 0

| Bits | Name | Description |
|------|--------------|-------------------------------------|
| 6:4 | restrim[2:0] | I2C regulator series resistor trim. |
| 1:0 | trim[1:0] | I2C regulator trim. |

1.3.131 PWRSYS_SLP_TR

Sleep Regulator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_SLP_TR: 0x40004683

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|---|--------|----------|---|---|---|
| SW Access:Reset | R/W:111 | | | R/W:0 | R/W:0011 | | | |
| HW Access | R | | | R | R | | | |
| Name | hibslp_holdoff | | | bypass | trim | | | |

This register trims the sleep regulator.

Register Segment: 0

| Bits | Name | Description |
|------|---------------------|---|
| 7:5 | hibslp_holdoff[2:0] | Number of 1kHz ILO clocks before the hibernate/sleep regulator is ready after a chip reset. Before it is ready, the system will ignore power mode requests except active and standby. It also overrides trim settings for the hibernate/sleep regulator. See Table 1-83. |
| 4 | bypass | When set, disables the sleep regulator and shorts vccd to vpwrslp. The bypass is internally shorted until hibslp_holdoff expires. |
| 3:0 | trim[3:0] | Sleep regulator trim. |

Table 1-83. Bit field encoding: holdoff_enum

| Value | Name | Description |
|--------|----------|------------------------------|
| 3'b000 | HOLDOFF0 | 0 clocks => disables holdoff |
| 3'b001 | HOLDOFF1 | 1 clocks => 0-1ms |
| 3'b010 | HOLDOFF2 | 2 clocks => 1-2ms |
| 3'b011 | HOLDOFF3 | 3 clocks => 2-3ms |
| 3'b100 | HOLDOFF4 | 4 clocks => 3-4ms |
| 3'b101 | HOLDOFF5 | 5 clocks => 4-5ms |
| 3'b110 | HOLDOFF6 | 6 clocks => 5-6ms |
| 3'b111 | HOLDOFF7 | 7 clocks => 6-7ms |

1.3.132 PWRSYS_BUZZ_TR

Power Mode Buzz Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_BUZZ_TR: 0x40004684

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0011 | | | | R/W:0011 | | | |
| HW Access | R | | | | R | | | |
| Name | idle_buzz | | | | slp_buzz | | | |

This register trims the settings for system sampling (buzzing).

Register Segment: 0

| Bits | Name | Description |
|------|----------------|---|
| 7:4 | idle_buzz[3:0] | Sets the buzz rate for digital and analog LDOs during idle mode See Table 1-84. |
| 3:0 | slp_buzz[3:0] | Sets the buzz rate for digital and analog LDOs during sleep mode See Table 1-84. |

Table 1-84. Bit field encoding: psoc3pwrmgr_pwrsys_trim_buzz_enum

| Value | Name | Description |
|---------|----------------|-------------------------|
| 4'b0000 | BUZZ_2_TICKS | 2 CTW ticks ==> 2ms |
| 4'b0001 | BUZZ_4_TICKS | 4 CTW ticks ==> 4ms |
| 4'b0010 | BUZZ_8_TICKS | 8 CTW ticks ==> 8ms |
| 4'b0011 | BUZZ_16_TICKS | 16 CTW ticks ==> 16ms |
| 4'b0100 | BUZZ_32_TICKS | 32 CTW ticks ==> 32ms |
| 4'b0101 | BUZZ_64_TICKS | 64 CTW ticks ==> 64ms |
| 4'b0110 | BUZZ_128_TICKS | 128 CTW ticks ==> 128ms |
| 4'b0111 | BUZZ_256_TICKS | 256 CTW ticks ==> 256ms |
| 4'b1000 | BUZZ_512_TICKS | 512 CTW ticks ==> 512ms |

1.3.133 PWRSYS_WAKE_TR0

Power Mode Wakeup Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_WAKE_TR0: 0x40004685

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:01111111 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | wake_to_interval | | | | | | | |

This register configures the settings for waking up the chip from low power modes.

Register Segment: 0

| Bits | Name | Description |
|------|-----------------------|---|
| 7:0 | wake_to_interval[7:0] | Sets the timeout time to wait until releasing the ignore_pres* conditioning for the PRES-A/D. The timeout time is wake_precent*wake_to_interval IMO cycles running at wake_imofreq. |

1.3.134 PWRSYS_WAKE_TR1

Power Mode Wakeup Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_WAKE_TR1: 0x40004686

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------------|------|-------------|---|---|--------------|---|---|
| SW Access:Reset | R/W:1 | NA:0 | R/W:000 | | | R/W:000 | | |
| HW Access | R | NA | R | | | R | | |
| Name | en_early_powerup | | wake_precnt | | | wake_imofreq | | |

This register configures the settings for waking up the chip from low power modes.

Register Segment: 0

| Bits | Name | Description |
|------|-------------------|---|
| 7 | en_early_powerup | Enable early powerup of flash and BG systems. When set, the flash and BG systems are powered up early for a normal wakeup from hibernate, sleep, and idle modes. This allows their internal supplies to ramp with the core supply, and enables them to stabilize approximately 5us more quickly once the supply is good. This bit must be set to achieve the wake time specs. |
| 5:3 | wake_precnt[2:0] | Sets the wakeup precount value for the timeout counter {PWRSYS.WAKE_TR0} and holdoff counter {PWRSYS.WAKE_TR3}. Wakeup timing is spec'd at 12MHz. If a different wake_imofreq is used, the correct divide ratio should be set here (eg to compensate for 24MHz, set 3'b001). |
| 2:0 | wake_imofreq[2:0] | Sets the IMO frequency used during chip wakeup from a low power mode. |

[See Table 1-85.](#)

Table 1-85. Bit field encoding: fimo_freq_enum

| Value | Name | Description |
|--------|--------------|-------------|
| 3'b000 | FIMO_12MHZ | 12 MHz |
| 3'b001 | FIMO_RSVD001 | RESERVED |
| 3'b010 | FIMO_24MHZ | UNSUPPORTED |
| 3'b011 | FIMO_RSVD011 | RESERVED |
| 3'b100 | FIMO_48MHZ | UNSUPPORTED |
| 3'b101 | FIMO_RSVD101 | RESERVED |
| 3'b110 | FIMO_RSVD110 | RESERVED |
| 3'b111 | FIMO_RSVD111 | RESERVED |

1.3.135 PWRSYS_BREF_TR

Boot Reference Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_BREF_TR: 0x40004687

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------------|-------|---|----------------------|-----------------------|-------------|--------------------|--------------------|
| SW Access:Reset | R/W:1 | NA:00 | | R/W:1 | R/W:0 | R/W:1 | R/W:1 | R/W:0 |
| HW Access | R | NA | | R | R | R | R | R |
| Name | bref_manua l | | | bref_force_t urbo | bref_testmo de_reg | bref_en_reg | bref_outen_ reg | bref_refsw_ reg |

This registers configures the power system boot reference..

Register Segment: 0

| Bits | Name | Description |
|------|-------------------|---|
| 7 | bref_manual | This bit must be written low in the manufacturing trim portion of the test program. When set the other fields in this register allow manual bootref control, which is for RMP and char purposes only. When clear, the power manager will automatically switch the bootref output between the bootref voltage itself and the LVBG after resets and wakeups. When clear, at power up and wakeup, the power manager forces the LDO and LPCOMP references to be the boot reference till device wakes-up (meaning untill CPU starts running on wakeup). bootref is disabled while device wakeup when this bit is set AND device is in externally regulated VCCA and VCCD mode AND PWRSYS_WAKE_TR2[2] is set At the above configuration regular LPCOMPs are used to detect power good during Hibernate and Hibernate timers mode. Since reference is disabled, device can't wakeup from hibernate and hibernate timer modes. Make sure PWRSYS_WAKE_TR2[2] is cleared during Hibertnate, Hibernate Timers mode |
| 4 | bref_force_turbo | reserved This bit is no longer used inside the power system. It remains for RMP. The original purpose is: When bref_manual is set, this enables turbo startup for the internal boot reference. |
| 3 | bref_testmode_reg | When bref_manual is set, this puts the bootref in testmode. |
| 2 | bref_en_reg | When bref_manual is set, this fields enables the internal boot reference. This field must be set whenever either LDO is on. |
| 1 | bref_outen_reg | When bref_manual is set, this fields enables the output stage of the LDO reference selector. This field must be set prior to selecting the BREF source using bref_refsw_reg. |
| 0 | bref_refsw_reg | When bref_manual is set, this fields controls the power system reference source. Using the LVBG reference improves PSRR. See Table 1-86. |

Table 1-86. Bit field encoding: bref_refsw_enum

| Value | Name | Description |
|-------|------|-----------------------------|
| 1'b0 | BREF | BREF (boot reference) |
| 1'b1 | LVBG | LVBG (low voltage band gap) |

1.3.136 PWRSYS_BG_TR

Bandgap Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_BG_TR: 0x40004688

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------------|------|-----------|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:00000 | | | | |
| HW Access | NA | R | NA | R | | | | |
| Name | | trimbuf_fine | | inl_ctl | | | | |

Bandgap Trim

Register Segment: 0

| Bits | Name | Description |
|------|--------------|---|
| 6 | trimbuf_fine | Current Bandgap - nonlinear current control (fine tuning) |
| 4:0 | inl_ctl[4:0] | Current Bandgap - nonlinear current control |

1.3.137 PWRSYS_WAKE_TR2

Power Mode Wakeup Trim Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_WAKE_TR2: 0x40004689

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------------------|---------------------|---------------------|---------------------|---------------------|---------|
| SW Access:Reset | NA:00 | | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 |
| HW Access | NA | | R | R | R | R | R | R |
| Name | | | use_early_s hort | use_vccd_b ackup | use_vcca_b ackup | use_vccdclk _det | use_bgwku p_fast | en_buzz |

This register configures the settings for waking up the chip from low power modes.

Register Segment: 0

| Bits | Name | Description |
|------|------------------|---|
| 5 | use_early_short | Enable early shorting between vccd/vnwell/vpwrao/vpwrka. When set, the shorts will be applied at the wakeup event for sleep and idle modes. If clear or a wakeup from hibernate mode, shorts will be applied at the powergood event. Note that if early shorting is used, it is critical that vccd be at a valid voltage (>1.2V) for proper logic retention. If it is not, then state loss can occur including WDT failure. If using internal regulation, it is recommended to set use_vccd_backup and use_vcca_backup to ensure that the supply is valid. This bit is in a protected register segment to avoid accidental corruption. This bit must be set to achieve the wake time specs when using internal regulation for vccd. |
| 4 | use_vccd_backup | Enable replica regulated vccd supply. When using internal regulation for vccd, this bit enables a backup regulator that keeps vccd during sleep and idle modes. When clear, buzzing should be enabled to ensure that vccd remains high enough to meet the wake time requirement. If the buzzing approach is used, it is highly recommended to use the LPCOMP powergood detection scheme (use_vccdclk_det=0), since it is robust if vccd droops. This bit must be set to achieve the wake time specs when using the internal regulation for vccd. If the chip is configured for external vccd supply using {PWRSYS_CR0}.ext_vccd, then this bit is ignored. |
| 3 | use_vcca_backup | Enable replica regulated vcca supply. When using internal regulation for vcca, this bit enables a backup regulator that keeps vcca during sleep and idle modes. When clear, buzzing should be enabled to ensure that vcca remains high enough to meet the wake time requirement. If the buzzing approach is used, it is highly recommended to use the LPCOMP powergood detection scheme (use_vccdclk_det=0), since it is robust if vcca droops. This bit must be set to achieve the wake time specs when using the internal regulation for vcca. If the chip is configured for external vcca supply using {PWRSYS_CR0}.ext_vcca, then this bit is ignored. |
| 2 | use_vccdclk_det | Enable alternate powergood detector. When set, a faster powergood detector is used during wakeup from sleep only, during other times LPCOMPs are used. When clear, the LPCOMPs are used. Make sure this bit is never set during externally regulated device low power modes Hibernate and Hibernate timers, because bootref is disabled during wakeup. The alternate powergood detector is faster, but it relies on valid vccd and vcca supplies. It is recommended to use it with the replica regulators (use_vccd_backup and use_vcca_backup) or external supplies. The LPCOMP detector is slower but is robust to droops on vcca and vccd. This bit must be set to achieve the wake time specs. |
| 1 | use_bgwku_p_fast | Enable fast BG wakeup. This bit must be set to achieve the wake time specs. |

1.3.137 PWRSYS_WAKE_TR2 (continued)

| | | |
|---|---------|--|
| 0 | en_buzz | Enable buzz wakeups. Buzzing wakes the regulators (if configured) and performs periodic voltage supervision. |
|---|---------|--|

1.3.138 PWRSYS_WAKE_TR3

Power Mode Wakeup Trim Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_WAKE_TR3: 0x4000468A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:01011111 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | wake_ho_interval | | | | | | | |

This register configures the settings for waking up the chip from low power modes.

Register Segment: 0

| Bits | Name | Description |
|------|-----------------------|--|
| 7:0 | wake_ho_interval[7:0] | Sets the holdoff time to wait until sampling PRES-A/D. The holdoff time is wake_precent*wake_ho_interval IMO cycles running at wake_imofreq. |

1.3.139 ILO_TR0

Internal Low-speed Oscillator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ILO_TR0: 0x40004690

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:1000 | | | | R/W:1000 | | | |
| HW Access | R | | | | R | | | |
| Name | tr_100k | | | | tr_1k | | | |

This register is used to trim the frequency of the ILO output clocks.

Register Segment: 0

| Bits | Name | Description |
|------|--------------|--|
| 7:4 | tr_100k[3:0] | Trim setting for 100 kHz output See Table 1-87. |
| 3:0 | tr_1k[3:0] | Trim setting for 1 kHz output See Table 1-88. |

Table 1-87. Bit field encoding: TR_100K_ENUM

| Value | Name | Description |
|---------|-------------|-------------------|
| 4'b0000 | TR_100K_MIN | Minimum Frequency |
| 4'b1111 | TR_100K_MAX | Maximum Frequency |

Table 1-88. Bit field encoding: TR_1K_ENUM

| Value | Name | Description |
|---------|-----------|-------------------|
| 4'b0000 | TR_1K_MIN | Minimum Frequency |
| 4'b1111 | TR_1K_MAX | Maximum Frequency |

1.3.140 ILO_TR1

Internal Low-speed Oscillator Coarse Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ILO_TR1: 0x40004691

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|----------|--------|---|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:10 | |
| HW Access | NA | | | | | R | R | |
| Name | | | | | | ct_range | ctrim | |

This register is used to trim the frequency of the ILO output clocks.

Register Segment: 0

| Bits | Name | Description |
|------|------------|---|
| 2 | ct_range | Coarse Trim Range select for ILO See Table 1-90. |
| 1:0 | ctrim[1:0] | Coarse Trim Setting for ILO See Table 1-89. |

Table 1-89. Bit field encoding: CTRIM_ENUM

| Value | Name | Description |
|-------|---------|--|
| 2'h0 | CTRIM_0 | Full Resistor (lowest current, lowest frequency) |
| 2'h1 | CTRIM_1 | 3/4 * R |
| 2'h2 | CTRIM_2 | 1/2 * R |
| 2'h3 | CTRIM_3 | 1/4 * R (highest current, highest frequency) |

Table 1-90. Bit field encoding: CT_RANGE_ENUM

| Value | Name | Description |
|-------|------------|---------------------|
| 1'b0 | CT_RANGE_0 | Normal range |
| 1'b1 | CT_RANGE_1 | Lower current range |

1.3.141 X32_TR

32 kHz Watch Crystal Oscillator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

X32_TR: 0x40004698

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---|---------|---|
| SW Access:Reset | NA:00000 | | | | | | R/W:101 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | xgm | |

(no description)

| Bits | Name | Description |
|------|----------|--|
| 2:0 | xgm[2:0] | Amplifier GM setting, applies to both High and Low power modes |

[See Table 1-91.](#)

Table 1-91. Bit field encoding: XGM_ENUM

| Value | Name | Description |
|--------|-------------|-------------------------|
| 3'b000 | XGM_MAX | Highest current setting |
| 3'b101 | XGM_DEFAULT | Default setting |
| 3'b111 | XGM_MIN | Lowest current setting |

1.3.142 IMO_TR0

Internal Main Oscillator Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_TR0: 0x400046A0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:111 | | | NA:00000 | | | | |
| HW Access | R/W | | | NA | | | | |
| Name | imo_lsb | | | | | | | |

This register contains the frequency trim for the IMO. For each frequency range, a separate factory trim should be loaded into this register. It is recommended that the user not change the value of this register. When changing frequency ranges, the new trim value should be applied at the lowest frequency range. For example, when switching to a high range, first apply the trim value of the higher range, then switch the IMO to that range. If switching to a lower range, change the range first and then apply the new trim value.

Register Segment: 1

| Bits | Name | Description |
|------|--------------|--|
| 7:5 | imo_lsb[2:0] | These are the 3 LSB of the IMO frequency trim. Normally these are not changed by the user, and are only modified by the hardware during USB clock-locking. These bits are locked from user write when USB Oscillator locking is enabled. |

[See Table 1-92.](#)

Table 1-92. Bit field encoding: IMO_LSB_ENUM

| Value | Name | Description |
|--------|-------------|---------------|
| 3'b000 | IMO_LSB_MIN | minimum value |
| 3'b111 | IMO_LSB_MAX | maximum value |

1.3.143 IMO_TR1

Internal Main Oscillator Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_TR1: 0x400046A1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:10011101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | imo_trim | | | | | | | |

IMO Trim for 48 MHz frequency setting

Register Segment: 1

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | imo_trim[7:0] | Frequency trim (8 MSbits) for the IMO. 8 MSbits of the trim. The factory trim only uses these 8 bits; the 3 LSBs (IMO_LSB[2:0]) are normally only used during USB operation. These bits are locked from user write when USB Oscillator locking is enabled. |

[See Table 1-93.](#)

Table 1-93. Bit field encoding: IMO_TRIM_ENUM

| Value | Name | Description |
|-------|--------------|-------------------|
| 8'h00 | IMO_TRIM_MIN | Minimum frequency |
| 8'hff | IMO_TRIM_MAX | Maximum frequency |

1.3.144 IMO_GAIN

Internal Main Oscillator Gain Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_GAIN: 0x400046A2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:001111 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | gain | | | | | |

This register contains the gain trim for the IMO. This is normally set with a factory trim and not modified by the user.

Register Segment: 1

| Bits | Name | Description |
|------|-----------|--|
| 5:0 | gain[5:0] | Gain trim for the IMO. This controls the kHz/step of the trim setting in the IMO_TR register. See Table 1-94. |

Table 1-94. Bit field encoding: GAIN_ENUM

| Value | Name | Description |
|-------|----------|--------------|
| 6'h00 | GAIN_MAX | Maximum Gain |
| 6'h3F | GAIN_MIN | Minimum Gain |

1.3.145 IMO_C36M

Internal Main Oscillator 36 MHz clock control register {INTERNAL}

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_C36M: 0x400046A3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | tr36 | | | |

This register controls operation of the 36 Mhz output of the IMO.

Register Segment: 1

| Bits | Name | Description |
|------|-----------|---|
| 3:0 | tr36[3:0] | Frequency trim for the 36 MHz SPC clock. This value should not be changed by the user. See Table 1-95. |

Table 1-95. Bit field encoding: TR36_ENUM

| Value | Name | Description |
|-------|----------|-------------------|
| 4'h0 | TR36_MIN | Minimum frequency |
| 4'hf | TR36_MAX | Maximum frequency |

1.3.146 IMO_TR2

Internal Main Oscillator Trim Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_TR2: 0x400046A4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|------|------------|---|---|---|---|---|
| SW Access:Reset | R/W:0 | NA:0 | R/W:000110 | | | | | |
| HW Access | R | NA | R | | | | | |
| Name | pll_trim | | fimo_trim | | | | | |

This register contains the frequency trim for the IMO during fastwake mode.

Register Segment: 1

| Bits | Name | Description |
|------|----------------|--|
| 7 | pll_trim | PLL trim |
| 5:0 | fimo_trim[5:0] | Frequency trim for the IMO in fastwake mode (FIMO). This value should not be changed by the user. Reset default value for bits 5:4 will be overwritten by NVLatch bits during boot |

[See Table 1-96.](#)

Table 1-96. Bit field encoding: FIMO_TRIM_ENUM

| Value | Name | Description |
|-------|---------------|-------------------|
| 6'h00 | FIMO_TRIM_MIN | Minimum frequency |
| 6'h3f | FIMO_TRIM_MAX | Maximum frequency |

1.3.147 XMHZ_TR

External 4-25 MHz Crystal Oscillator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

XMHZ_TR: 0x400046A8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | iref | | | |

(no description)

Register Segment: 1

| Bits | Name | Description |
|------|-----------|---|
| 3:0 | iref[3:0] | This bit adjusts the output current of the oscillator circuit. The value is selected to match the output external crystal characteristics. See Table 1-97. |

Table 1-97. Bit field encoding: IREF_ENUM

| Value | Name | Description |
|-------|--------|-------------------|
| 4'h0 | IREF_0 | 13 unit resistors |
| 4'h1 | IREF_1 | 14 unit resistors |
| 4'h2 | IREF_2 | 15 unit resistors |
| 4'h3 | IREF_3 | 16 unit resistors |
| 4'h4 | IREF_4 | 17 unit resistors |
| 4'h5 | IREF_5 | 18 unit resistors |
| 4'h6 | IREF_6 | 19 unit resistors |
| 4'h7 | IREF_7 | 20 unit resistors |
| 4'h8 | IREF_8 | 21 unit resistors |
| 4'h9 | IREF_9 | 22 unit resistors |
| 4'ha | IREF_A | 23 unit resistors |
| 4'hb | IREF_B | 24 unit resistors |
| 4'hc | IREF_C | 25 unit resistors |
| 4'hd | IREF_D | 26 unit resistors |
| 4'he | IREF_E | 27 unit resistors |
| 4'hf | IREF_F | 28 unit resistors |

1.3.148 DLY

Delay block Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DLY: 0x400046C0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------|---|-----------|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:00 | | R/W:00000 | | | | |
| HW Access | NA | R | | R | | | | |
| Name | | CTRIM | | FTRIM | | | | |

This register is used to trim the delay cell tap duration. This register should only be used when the delay cell is in trim mode (see DLY1 MODE bit). **User Defined Properties:** unique_name_space=1

| Bits | Name | Description |
|------|------------|--|
| 6:5 | CTRIM[1:0] | Course trim bits for delay block See Table 1-98. |
| 4:0 | FTRIM[4:0] | Fine trim bits for delay block 5'b00000 Lowest bias 5'bffff Highest bias |

Table 1-98. Bit field encoding: CTRIM_ENUM

| Value | Name | Description |
|-------|-------|-----------------------------|
| 2'b00 | ZERO | Highest bias setting |
| 2'b10 | TWO | Second highest bias setting |
| 2'b01 | ONE | Third highest bias setting |
| 2'b11 | THREE | Fourth highest bias setting |

1.3.149 MLOGIC_WNDG_CFG0

MLogic Wounding Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_WNDG_CFG0: 0x400046E0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|---|---|----------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R/W:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | wounding_sram | | | | wounding_flash | | | |

This register sets the various wounding values for the part. This register can be read at any time, but may only be written when the BOOT bit (MLOGIC.CPU.SCR[2]) is set.

| Bits | Name | Description |
|------|---------------------|--|
| 7:4 | wounding_sram[3:0] | SRAM wounding register See Table 1-100. |
| 3:0 | wounding_flash[3:0] | Flash wounding register See Table 1-99. |

Table 1-99. Bit field encoding: flash_enum

| Value | Name | Description |
|---------|----------------|---------------------|
| 4'b0000 | RESERVED | Reserved |
| 4'b0001 | RESERVED1 | Reserved |
| 4'b0010 | RESERVED2 | Reserved |
| 4'b0011 | RESERVED3 | Reserved |
| 4'b0100 | WND_FLASH_8M | 8 Megabytes Flash |
| 4'b0101 | WND_FLASH_4M | 4 Megabytes Flash |
| 4'b0110 | WND_FLASH_2M | 2 Megabytes Flash |
| 4'b0111 | WND_FLASH_1M | 1 Megabytes Flash |
| 4'b1000 | WND_FLASH_512K | 512 Kilobytes Flash |
| 4'b1001 | WND_FLASH_256K | 256 Kilobytes Flash |
| 4'b1010 | WND_FLASH_128K | 128 Kilobytes Flash |
| 4'b1011 | WND_FLASH_64K | 64 Kilobytes Flash |
| 4'b1100 | WND_FLASH_32K | 32 Kilobytes Flash |
| 4'b1101 | WND_FLASH_16K | 16 Kilobytes Flash |
| 4'b1110 | WND_FLASH_8K | 8 Kilobytes Flash |
| 4'b1111 | WND_FLASH_4K | 4 Kilobytes Flash |

Table 1-100. Bit field encoding: sram_enum

| Value | Name | Description |
|---------|---------------|-----------------------|
| 4'b0000 | WND_SRAM_8M | 8 Megabytes of SRAM |
| 4'b0001 | WND_SRAM_4M | 4 Megabytes of SRAM |
| 4'b0010 | WND_SRAM_2M | 2 Megabytes of SRAM |
| 4'b0011 | WND_SRAM_1M | 1 Megabytes of SRAM |
| 4'b0100 | WND_SRAM_512K | 512 Kilobytes of SRAM |
| 4'b0101 | WND_SRAM_256K | 256 Kilobytes of SRAM |
| 4'b0110 | WND_SRAM_128K | 128 Kilobytes of SRAM |
| 4'b0111 | WND_SRAM_64K | 64 Kilobytes of SRAM |
| 4'b1000 | WND_SRAM_32K | 32 Kilobytes of SRAM |

1.3.149 MLOGIC_WNDG_CFG0 (continued)

Table 1-100. Bit field encoding: sram_enum

| | | |
|---------|---------------|----------------------|
| 4'b1001 | WND_SRAM_16K | 16 Kilobytes of SRAM |
| 4'b1010 | WND_SRAM_8K | 8 Kilobytes of SRAM |
| 4'b1011 | WND_SRAM_4K | 4 Kilobytes of SRAM |
| 4'b1100 | WND_SRAM_2K | 2 Kilobytes of SRAM |
| 4'b1101 | WND_SRAM_1K | 1 Kilobytes of SRAM |
| 4'b1110 | WND_SRAM_512B | 512 bytes of SRAM |
| 4'b1111 | WND_SRAM_256B | 256 bytes of SRAM |

1.3.150 MLOGIC_WNDG_CFG1

MLogic Wounding Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_WNDG_CFG1: 0x400046E1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|-------|---|--------------|------------------|---|---|
| SW Access:Reset | R:00 | | NA:00 | | R:0 | R:000 | | |
| HW Access | R/W | | NA | | R/W | R/W | | |
| Name | wounding_can | | | | wounding_usb | wounding_eeeprom | | |

This register sets the various wounding values for the part. This register can be read at any time, but may only be written when the BOOT bit (MLOGIC.CPU.SCR[2]) is set.

| Bits | Name | Description |
|------|-----------------------|---|
| 7:6 | wounding_can[1:0] | CAN Wounding. See Table 1-101. |
| 3 | wounding_usb | USB enable/disable |
| 2:0 | wounding_eeeprom[2:0] | EEPROM wounding See Table 1-102. |

Table 1-101. Bit field encoding: can_enum

| Value | Name | Description |
|-------|---------|----------------------------|
| 2'b00 | ALL_CAN | All CAN blocks enabled |
| 2'b01 | TWO_CAN | CAN blocks 0 and 1 enabled |
| 2'b10 | ONE_CAN | CAN block 0 enabled |
| 2'b11 | NO_CAN | All CAN blocks disabled |

Table 1-102. Bit field encoding: eeeprom_enum

| Value | Name | Description |
|--------|-----------------|--------------------|
| 3'b000 | RESERVED | Reserved |
| 3'b001 | RESERVED1 | Reserved |
| 3'b010 | WND_EEPROM_8K | 8 Kilobytes EEPROM |
| 3'b011 | WND_EEPROM_4K | 4 Kilobytes EEPROM |
| 3'b100 | WND_EEPROM_2K | 2 Kilobytes EEPROM |
| 3'b101 | WND_EEPROM_1K | 1 Kilobyte EEPROM |
| 3'b110 | WND_EEPROM_512B | 512 Bytes EEPROM |
| 3'b111 | WND_EEPROM_256B | 256 Bytes EEPROM |

1.3.151 MLOGIC_DMPSTR

Dumpster Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_DMPSTR: 0x400046E2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dumpster | | | | | | | |

(no description)

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | dumpster[7:0] | Dummy register used to pad the manufacturing configuration table. If the MFGCFG table has less than 63 data/address pairs, the remaining pairs write to this register to ensure nothing configured incorrectly |

1.3.152 MLOGIC_SEG_CR

Segment Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_SEG_CR: 0x400046E4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:10110100 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | segment_control | | | | | | | |

(no description)

| Bits | Name | Description |
|------|----------------------|--|
| 7:0 | segment_control[7:0] | Segment Control, controls write access to the segment register. When 0xB5 is written the lock on the Segment Configuration is removed. When 0xB4 is written, the Segment Configuration bits are locked and may only be read. Writing any other value triggers a reset. |

1.3.153 MLOGIC_SEG_CFG0

Segment Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_SEG_CFG0: 0x400046E5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|--------|----------------|--------|----------------|--------|----------------|--------|
| SW Access:Reset | R/WOSET:0 | R/W:0 | R/WOSET:0 | R/W:0 | R/WOSET:0 | R/W:0 | R/WOSET:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | lock_protect_3 | lock_3 | lock_protect_2 | lock_2 | lock_protect_1 | lock_1 | lock_protect_0 | lock_0 |

(no description)

| Bits | Name | Description |
|------|----------------|----------------------|
| 7 | lock_protect_3 | Segment Lock Protect |
| 6 | lock_3 | Segment Lock |
| 5 | lock_protect_2 | Segment Lock Protect |
| 4 | lock_2 | Segment Lock |
| 3 | lock_protect_1 | Segment Lock Protect |
| 2 | lock_1 | Segment Lock |
| 1 | lock_protect_0 | Segment Lock Protect |
| 0 | lock_0 | Segment Lock |

1.3.154 MLOGIC_DEBUG

MLOGIC Debug Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_DEBUG: 0x400046E8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------------|-------------|-------|-------------|------------|---------------|------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:0 |
| HW Access | NA | R | R | R | R | R | R | NA |
| Name | | allow_rst_hrd | dis_dbg_prt | CORD | swv_clk_sel | swv_clk_en | dis_sw_d_list | |

(no description)

| Bits | Name | Description |
|------|---------------|--|
| 6 | allow_rst_hrd | Allows XRES to generate a hard reset during JTAG and SWD mode. This bit should not be set at the same time as dis_dbg_prt. Both bits set together will not allow the debug port to be reclaimed without a port acquire |
| 5 | dis_dbg_prt | Disable Debug Port, removes port overrides of debug port so that the JTAG/SWD pins can be used as GPIOs. This bit should not be set at the same time as allow_rst_hrd. Both bits set together will not allow the debug port to be reclaimed without a port acquire |
| 4 | CORD | 0x0: Reading RC registers clears the values in them. 0x1: Clear on Read Disabled. Values in RC registers are not cleared when read. |
| 3 | swv_clk_sel | Serial Wire Viewer (SWV) trace clock select. When set to '0' SWD clock is used for trace clock. When set to '1' clk_cpu/2 is used for trace clock |
| 2 | swv_clk_en | Serial Wire View (SWV) clock enable. When set to '1' the clocks for SWV are enabled. This bit must be set to '1' to use SWV |
| 1 | dis_sw_d_list | Disable SWD Listening of the Test Controller, forces the SWDO from the CM3's DAP to always be the output in SWD mode. |

1.3.155 MLOGIC_CPU_SCR_CPU_SCR

System Status and Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_CPU_SCR_CPU_SCR: 0x400046EA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----|------|-------|----------|
| SW Access:Reset | NA:0000 | | | | R:0 | R:1 | R:0 | R:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R |
| Name | | | | | wol | boot | tmode | RESERVED |

(no description)

| Bits | Name | Description |
|------|----------|--|
| 3 | wol | Write Once Latch Status |
| 2 | boot | Boot. Cleared by the Checksum block upon completion of the boot process. |
| 1 | tmode | Test Mode Status |
| 0 | RESERVED | Reserved |

1.3.156 MLOGIC_REV_ID

Silicon Revision ID

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_REV_ID: 0x400046EC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | revision_id | | | | | | | |

(no description)

MLOGIC Silicon Revision

| Bits | Name | Description |
|------|------------------|---|
| 7:0 | revision_id[7:0] | Silicon Revision ID is an unmistakable electrical identifier of a particular JTAG ID. The JTAG ID code can remain unchanged across multiple silicon revisions. The Silicon Revision ID is under complete control of Cypress and can be revised without affecting the JTAG ID. Revision 0x00: Panther-LP Revision ** Revision 0x01: Panther-LP Revision *A with identical ESD/latchup performance as Revision **, meeting JEDEC 2kV standard Revision 0x02: Panther-LP Revision *A with improved ESD/latchup performance as Revision **, meeting JEDEC 2kV and Cypress 2.2kV standards |

1.3.157 RESET_IPOR_CR0

Imprecise Power On Reset Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR0: 0x400046F0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | code | | | | | | | |

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Register Segment: 0

| Bits | Name | Description |
|------|-----------|--|
| 7:0 | code[7:0] | Write 0xD4 to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset. |

1.3.158 RESET_IPOR_CR1

Imprecise Power On Reset Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR1: 0x400046F1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | code | | | | | | | |

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Register Segment: 0

| Bits | Name | Description |
|------|-----------|--|
| 7:0 | code[7:0] | Write 0xAA to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset. |

1.3.159 RESET_IPOR_CR2

Imprecise Power On Reset Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR2: 0x400046F2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | code | | | | | | | |

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Register Segment: 0

| Bits | Name | Description |
|------|-----------|--|
| 7:0 | code[7:0] | Write 0x56 to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset. |

0x400046f3

1.3.160 RESET_IPOR_CR3

Imprecise Power On Reset Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR3: 0x400046F3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | code | | | | | | | |

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Register Segment: 0

| Bits | Name | Description |
|------|-----------|--|
| 7:0 | code[7:0] | Write 0xC9 to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset. |

1.3.161 RESET_CR0

LVI Set Point Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR0: 0x400046F4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0000 | | | | R/W:0000 | | | |
| HW Access | R | | | | R | | | |
| Name | lvia | | | | lvid | | | |

This register sets the trip points for the low voltage interrupt (LVI).

Please reference voltage monitors on the device datasheet for voltage trip levels.

Register Segment: 1

| Bits | Name | Description |
|------|-----------|--|
| 7:4 | lvia[3:0] | When LVI-A is enabled, these 4 bits select the trip point of the detector. |
| 3:0 | lvid[3:0] | When LVI-D is enabled, these 4 bits select the trip point of the detector. |

1.3.162 RESET_CR1

Reset System Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR1: 0x400046F5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|--------------|---------|---------|---------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | vmon_hvi_sel | en_hvia | en_lvia | en_lvid |

This register enables circuits in the reset subsystem.

Register Segment: 1

| Bits | Name | Description |
|------|--------------|---|
| 3 | vmon_hvi_sel | When set to 1, this bit enables the vmon to look at the VDDD. When this bit is cleared to 0, the vmon looks at the VDDA. |
| 2 | en_hvia | When set to 1, enables the high-voltage-interrupt feature on the external analog supply. When this bit is set, there is a possible glitch on the output. To account for this glitch the user must mask the interrupt prior to setting this bit, then clear the status register immediately after this bit is set. Only then this circuit is ready for use. |
| 1 | en_lvia | Enables the low-voltage-interrupt or reset feature on the external analog supply. When this bit is set to 1 along with the en_presa bit (RESET_CR3 bit 7) set to 1, the lvia becomes an additional reset source through the presa reset path. When this bit is set to 1 along with the en_presa bit (RESET_CR3 bit 7) cleared to 0, the lvia becomes an interrupt source. When this bit is cleared to 0, the bit state (either a zero or a one) of the en_presa bit (RESET_CR3 bit 7) has no impact on the reset or interrupt functionality. When this bit is set, there is a possible glitch on the output. To account for this glitch the user must mask the interrupt prior to setting this bit, then clear the status register immediately after this bit is set. Only then this circuit is ready for use. |
| 0 | en_lvid | Enables the low-voltage-interrupt or reset feature on the external digital supply. When this bit is set to 1 along with the en_presd bit (RESET_CR3 bit 6) set to 1, the lvid becomes an additional reset source through the presd reset path. When this bit is set to 1 along with the en_presd bit (RESET_CR3 bit 6) cleared to 0, the lvid becomes an interrupt source. When this bit is cleared to 0, the bit state (either a zero or a one) of the en_presd bit (RESET_CR3 bit 6) has no impact on the reset or interrupt functionality. When this bit is set, there is a possible glitch on the output. To account for this glitch the user must mask the interrupt prior to setting this bit, then clear the status register immediately after this bit is set. Only then this circuit is ready for use. |

1.3.163 RESET_CR2

Software Reset Control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

RESET_CR2: 0x400046F6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|-------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | swr |

This register control the software reset (SWR).

Register Segment: 1

| Bits | Name | Description |
|------|------|---|
| 0 | swr | Setting this bit will cause a system reset. |

1.3.164 RESET_CR3

LVD/POR Mode Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR3: 0x400046F7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|----------|--------|---|---|----------|---|---|
| SW Access:Reset | R/W:1 | R/W:1 | NA:000 | | | R/W:000 | | |
| HW Access | R | R | NA | | | R | | |
| Name | en_presa | en_presd | | | | tmux_sel | | |

This register controls mode settings for the LVDPOR subsystem.

Register Segment: 0

| Bits | Name | Description |
|------|---------------|--|
| 7 | en_presa | When this bit is set to 1 along with the en_lvia bit (RESET_CR1 bit 1) set to 1 , the lvia becomes an additional reset source through the presa reset path. When this bit is cleared to 0 along with the en_lvia bit (RESET_CR1 bit 1) set to 1, the lvia is only used as an interrupt source. If the en_lvia bit (RESET_CR1 bit 1) is cleared to 0, the bit state (either a zero or a one) has no impact on the reset or interrupt functionality. This bit is in segment 0. |
| 6 | en_presd | When this bit is set to 1 along with the en_lvid bit (RESET_CR1 bit 0) set to 1 , the lvid becomes an additional reset source through the presd reset path. When this bit is cleared to 0 along with the en_lvid bit (RESET_CR1 bit 0) set to 1, the lvid is only used as an interrupt source. If the en_lvid bit (RESET_CR1 bit 0) is cleared to 0, the bit state (either a zero or a one) has no impact on the reset or interrupt functionality. This bit is in segment 0. |
| 2:0 | tmux_sel[2:0] | Selects the circuit output to steer to the 'tmuxout' pin. This field is not in a protected segment. |

[See Table 1-103.](#)

Table 1-103. Bit field encoding: tmux_sel

| Value | Name | Description |
|--------|-----------|-------------------------------------|
| 3'b000 | TMODE_000 | Normal mode (output driven to vgnd) |
| 3'b001 | TMODE_001 | PRES-D |
| 3'b010 | TMODE_010 | PRES-A |
| 3'b011 | TMODE_011 | LVI-D |
| 3'b100 | TMODE_100 | LVI-A |
| 3'b101 | TMODE_101 | HVI-A |
| 3'b110 | TMODE_110 | LPCOMP-D (set => powergood) |
| 3'b111 | TMODE_111 | LPCOMP-A (set => powergood) |

1.3.165 RESET_CR4

Reset Ignore Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR4: 0x400046F8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------------|-----------------|-----------------|---------------|---------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:1 | R/W:1 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | ignore_hbr1 | ignore_lpcompa1 | ignore_lpcompd1 | ignore_presa1 | ignore_presd1 |

This register configures the system to ignore certain reset sources.

Register Segment: 0

| Bits | Name | Description |
|------|-----------------|---|
| 4 | ignore_hbr1 | When both this bit and ignore_hbr2 are set to 1, the HBR circuit is disabled. |
| 3 | ignore_lpcompa1 | When both this bit and ignore_lpcompa2 are set to 1, the LPCOMP-A circuits is disabled. Before entering Low Power Modes (LPM), this bit must be high. |
| 2 | ignore_lpcompd1 | When both this bit and ignore_lpcompd2 are set to 1, the LPCOMP-D circuit is disabled. Before entering Low Power Modes (LPM), this bit must be high. |
| 1 | ignore_presa1 | When both this bit and ignore_presa2 are set to 1, the PRES-A circuits is disabled. |
| 0 | ignore_presd1 | When both this bit and ignore_presd2 are set to 1, the PRES-D circuit is disabled. |

1.3.166 RESET_CR5

Reset Ignore Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR5: 0x400046F9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------------|-----------------|-----------------|---------------|---------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:1 | R/W:1 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | ignore_hbr2 | ignore_lpcompa2 | ignore_lpcompd2 | ignore_presa2 | ignore_presd2 |

This register configures the system to ignore certain reset sources.

Register Segment: 0

| Bits | Name | Description |
|------|-----------------|---|
| 4 | ignore_hbr2 | When both this bit and ignore_hbr1 are set to 1, the HBR circuit is disabled. |
| 3 | ignore_lpcompa2 | When both this bit and ignore_lpcompa1 are set to 1, the LPCOMP-A circuits is disabled. Before entering Low Power Modes (LPM), this bit must be high. |
| 2 | ignore_lpcompd2 | When both this bit and ignore_lpcompd1 are set to 1, the LPCOMP-D circuit is disabled. Before entering Low Power Modes (LPM), this bit must be high. |
| 1 | ignore_presa2 | When both this bit and ignore_presa1 are set to 1, the PRES-A circuits is disabled. |
| 0 | ignore_presd2 | When both this bit and ignore_presd1 are set to 1, the PRES-D circuit is disabled. |

1.3.167 RESET_SR0

Reset and Voltage Detection Status Register 0

Reset: Reset Signals Listed Below

Register : Address

RESET_SR0: 0x400046FA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|-------|------|-------|--------|--------|--------|
| SW Access:Reset | R/W:00 | | RC:0 | NA:0 | RC:0 | RC:0 | RC:0 | RC:0 |
| HW Access | NA | | R/W | NA | R/W | R/W | R/W | R/W |
| Name | gpsw_s | | swr_s | | wdr_s | hvia_s | lvia_s | lvid_s |

This register gives persistent status for the reset and voltage detection systems.

| Bits | Name | Description |
|------|-------------|--|
| 7:6 | gpsw_s[1:0] | General purpose status for user software. These bits can be set to 1 or cleared to 0 by software and only reset by hard reset sources. They can be used to hold user defined status that persists through many resets. |
| 5 | swr_s | Persistent status of the software reset. This bit will be set to 1 when a software reset occurs and will stay set to 1 until cleared to 0 by the user or reset. Sticky (whole field) |
| 3 | wdr_s | Persistent status of the watchdog reset. This bit will be set to 1 when a watchdog reset occurs and will stay set to 1 until cleared to 0 by the user or reset. Sticky (whole field) |
| 2 | hvia_s | Persistent status of analog HVI. This bit will be set to 1 when the analog supply goes below the trip point for the HVI detector and will stay set to 1 until cleared to 0 by the user or reset. Sticky (whole field) |
| 1 | lvia_s | Persistent status of analog LVI. This bit will be set to 1 when the analog supply goes below the trip point for the LVI detector and will stay set to 1 until cleared to 0 by the user or reset. Sticky (whole field) |
| 0 | lvid_s | Persistent status of digital LVI. This bit will be set to 1 when the digital supply goes below the trip point for the LVI detector and will stay set to 1 until cleared to 0 by the user or reset. Sticky (whole field) |

Reset Table

| resetsignal | field(s) |
|---|---------------------------|
| IPOR/PRES/HBR for retention [reset_hard_retention] | wdr_s, swr_s, gpsw_s[1:0] |
| IPOR/PRES/HBR for non-retention [reset_hard_nonretention] | lvid_s, lvia_s, hvia_s |

1.3.168 RESET_SR1

Reset and Voltage Detection Status Register 1

Reset: IPOR/PRES/HBR for non-retention flops [reset_hard_nonretention]

Register : Address

RESET_SR1: 0x400046FB

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------|----------|---------|---------|-------|---|--------|
| SW Access:Reset | NA:0 | RC:0 | RC:0 | RC:0 | RC:0 | NA:00 | | RC:0 |
| HW Access | NA | R/W | R/W | R/W | R/W | NA | | R/W |
| Name | | lpcompa_s | lpcmpd_s | presa_s | presd_s | | | segr_s |

This register gives persistent status for the reset and voltage detection systems.

| Bits | Name | Description |
|------|-----------|---|
| 6 | lpcompa_s | Persistent status of analog LPCOMP. This bit will be set to 1 when the analog supply goes below the trip point for the LPCOMP circuit and will stay set to 1 until cleared to 0 by the user or reset. Note that this field is only useful during test mode when the LPCOMP-A circuit does not cause a system reset. Sticky (whole field) |
| 5 | lpcmpd_s | Persistent status of digital LPCOMP. This bit will be set to 1 when the digital supply goes below the trip point for the LPCOMP circuit and will stay set to 1 until cleared to 0 by the user or reset. Note that this field is only useful during test mode when the LPCOMP-D circuit does not cause a system reset. Sticky (whole field) |
| 4 | presa_s | Persistent status of analog PRES. This bit will be set to 1 when the analog supply goes below the trip point for the PRES circuit and will stay set to 1 until cleared to 0 by the user or reset. Note that this field is only useful during test mode when the PRES-A circuit does not cause a system reset. Sticky (whole field) |
| 3 | presd_s | Persistent status of digital PRES. This bit will be set to 1 when the digital supply goes below the trip point for the PRES circuit and will stay set to 1 until cleared to 0 by the user or reset. Note that this field is only useful during test mode when the PRES-D circuit does not cause a system reset. Sticky (whole field) |
| 0 | segr_s | Persistent status of the segment reset. This bit will be set to 1 when the segment reset occurs circuit and will stay set to 1 until cleared to 0 by the user or reset. Note a segment reset occurs when a value other than 0xB4 or 0xB5 is written to the Segment Control Register. Sticky (whole field) |

1.3.169 RESET_SR2

Reset and Voltage Detection Status Register 2

Reset: IPOR/PRES/HBR for non-retention flops [reset_hard_nonretention]

Register : Address

RESET_SR2: 0x400046FC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|-----------|-----------|----------|---------|--------|--------|--------|
| SW Access:Reset | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 |
| HW Access | W | W | W | W | W | W | W | W |
| Name | hbrs_r | lpcompa_r | lpcompd_r | pres_a_r | presd_r | hvia_r | lvia_r | lvid_r |

This register gives real-time status for the reset and voltage detection systems.

| Bits | Name | Description |
|------|-----------|--|
| 7 | hbrs_r | Real-time status of HBR. This is only useful when the HBR does not cause a system level reset. |
| 6 | lpcompa_r | Real-time status of analog LPCOMP. This is only useful when the LPCOMP-A output is ignored. |
| 5 | lpcompd_r | Real-time status of digital LPCOMP. This is only useful when the LPCOMP-D output is ignored. |
| 4 | pres_a_r | Real-time status of analog PRES. This is only useful when the PRES-A output is ignored. |
| 3 | presd_r | Real-time status of digital PRES. This is only useful when the PRES-D output is ignored. |
| 2 | hvia_r | Real-time status of analog HVI. |
| 1 | lvia_r | Real-time status of analog LVI. |
| 0 | lvid_r | Real-time status of digital LVI. |

0x400046fd

1.3.170 RESET_SR3

Reset and Voltage Detection Status Register 3

Reset: IPOR/PRES/HBR for retention flops [reset_hard_retention]

Register : Address

RESET_SR3: 0x400046FD

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|---|---|------------|--------|---|---|
| SW Access:Reset | R:0000 | | | | R:1 | NA:000 | | |
| HW Access | R/W | | | | W | NA | | |
| Name | cksm_fail_cnts | | | | ipor_key_n | | | |

This register gives persistent status for the reset and voltage detection systems.

| Bits | Name | Description |
|------|---------------------|---|
| 7:4 | cksm_fail_cnts[3:0] | Count of the number of times the Checksum process has failed, causing a reset. These 4 bits will hold the count value and it will stay until cleared to 0 by a reset. |
| 3 | ipor_key_n | IPOR key status. When low, the IPOR key has been properly written using the IPOR_CR registers. |

1.3.171 RESET_TR

PRES Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_TR: 0x400046FE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0111 | | | | R/W:0111 | | | |
| HW Access | R | | | | R | | | |
| Name | presa | | | | presd | | | |

This register sets the trim for the precision voltage detectors (PRES).

Register Segment: 0

| Bits | Name | Description |
|------|------------|--|
| 7:4 | presa[3:0] | Trim for PRES-A. Default value sets the trip to 1.6V |
| 3:0 | presd[3:0] | Trim for PRES-D. Default value sets the trip to 1.6V |

1.3.172 SPC_FM_EE_CR FM_EE_CR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_FM_EE_CR: 0x40004700

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|----------|--------|---|---|-------------|-------------|
| SW Access:Reset | NA:00 | | R:0 | NA:000 | | | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | NA | | | R | R |
| Name | | | EE_AWAKE | | | | EE_Priority | FM_Priority |

This register contains control bits for the flash and eeprom arrays

| Bits | Name | Description |
|------|-------------|--|
| 5 | EE_AWAKE | Status signal to denote that the EEPROM array is awake & powered, when set equal to 1. On reset, this value is 0. When the EEPROM is enabled, after the 5 us startup time has elapsed, the bit will be set to a 1. |
| 1 | EE_Priority | Sets priority between the PHUB and the SPC for who gets control of the EEPROM array upon simultaneous access requests. 1-> SPC has priority. 0-> PHUB has priority. |
| 0 | FM_Priority | Sets priority between the cache controller and the SPC for who gets control of the flash array upon simultaneous access requests. 1-> SPC has priority. 0-> Cache controller has priority. |

1.3.173 SPC_FM_EE_WAKE_CNT

FM_EE_WAKE_CNT

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_FM_EE_WAKE_CNT: 0x40004701

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00011110 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | Wake_Count | | | | | | | |

Flash/EEPROM Wake Count Register

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | Wake_Count[7:0] | The wake count defines the number of Bus Clock cycles it takes for the flash or eeprom to wake up from being in a put into a low power mode independent of the chip power mode (while the rest of the chip remained in active or standby). Wake up time for these blocks is 5 us. The granularity of this register is 2 Bus Clock cycles, so a value of 0x1E (30d) defines the wake up time as 60 cycles of the Bus Clock. This register needs to be written with a value dependent on the Bus Clock frequency so that the duration of the cycles is equal to or greater than the 5 us delay required. The reset value of this register (0x1E) is for a Bus Clock frequency of 12 MHz. |

1.3.174 SPC_EE_SCR

EEPROM Status & Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_EE_SCR: 0x40004702

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|----------------|----------------|
| SW Access:Reset | NA:000000 | | | | | | R:0 | R/W:0 |
| HW Access | NA | | | | | | R/W | R |
| Name | | | | | | | EE_AHB_A CK | AHB_EE_R EQ |

This register contains status and control bits for the EEPROM array.

| Bits | Name | Description |
|------|------------|--|
| 1 | EE_AHB_ACK | Once the AHB_EE_REQ bit is set, this bit is set high once the EEPROM is available to be read across the PHUB interface. |
| 0 | AHB_EE_REQ | This bit is set high when a read access of the EEPROM, through the PHUB interface, is desired. This is a request bit and is part of a two bit interface with the EE_AHB_ACK bit. |

1.3.175 SPC_EE_ERR

EEPROM Error Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_EE_ERR: 0x40004703

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------------|
| SW Access:Reset | NA:0000000 | | | | | | | RC:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | EEPROM_error |

This register has an error bit for the EEPROM array on the chip. The error bit indicates whether or not the array has had a collision error where two masters (the SPC and the PHUB interface) attempted to access the array simultaneously. The bits are cleared upon a read of this register.

| Bits | Name | Description |
|------|--------------|------------------------------|
| 0 | EEPROM_error | Error bit for EEPROM array 0 |

1.3.176 SPC_CPU_DATA

SPC CPU Data Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

SPC_CPU_DATA: 0x40004720

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CPU_Data | | | | | | | |

This register is the command interface to the SPC that allows SPC instructions to be executed by the host CPU writing a sequential series of parameters to this location. This register is meant only for the CPU and not the DMA controller to prevent collisions between the CPU and the DMAC when both attempt to call a function in the SPC

| Bits | Name | Description |
|------|---------------|-------------|
| 7:0 | CPU_Data[7:0] | CPU Data. |

1.3.177 SPC_DMA_DATA

SPC DMA Data Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

SPC_DMA_DATA: 0x40004721

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DMA_Data | | | | | | | |

This register is the command interface to the SPC that allows SPC instructions to be executed by the DMA controller writing a sequential series of parameters to this location. This register is meant only for the DMA Controller and not the CPU to prevent collisions between the CPU and the DMAC when both attempt to call a function in the SPC

| Bits | Name | Description |
|------|---------------|-------------|
| 7:0 | DMA_Data[7:0] | DMA Data. |

1.3.178 SPC_SR

SPC Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_SR: 0x40004722

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|----------|------------|
| SW Access:Reset | R:000000 | | | | | | R:1 | R:0 |
| HW Access | R/W | | | | | | R/W | R/W |
| Name | Status_Code | | | | | | SPC_Idle | Data_Ready |

This register returns the current status of the SPC and the exit status of the last complete SPC instruction.

| Bits | Name | Description |
|------|------------------|--|
| 7:2 | Status_Code[5:0] | The Status Code represents the exit status of the last executed SPC instruction. See Table 1-106. |
| 1 | SPC_Idle | This bit indicates whether or not the SPC is currently executing an instruction. The bit transitions low as soon as the 1st byte of the 2-byte command key (0xB6) is written into the SPC CPU or DMA Data Register. The bit transitions high as soon as an instruction completes or if the 2nd byte of the command key is invalid. See Table 1-105. |
| 0 | Data_Ready | This bit indicates whether or not the SPC has data that is ready to be read from the SPC CPU or DMA Data Register. See Table 1-104. |

Table 1-104. Bit field encoding: DATA_RDY_ENUM

| Value | Name | Description |
|-------|-----------------|---|
| 1'h0 | DATA_IS_NOT_RDY | The SPC isn't ready for the next byte to be written |
| 1'h1 | DATA_IS_RDY | The SPC is read for the next byte to be written |

Table 1-105. Bit field encoding: INSTR_IDLE_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 1'h0 | INSTR_IS_NOT_IDLE | SPC is currently executing an SPC instruction. |
| 1'h1 | INSTR_IS_IDLE | SPC is idle and not busy executing an instruction. |

Table 1-106. Bit field encoding: SPC_SR_STATUS_CODE_ENUM

| Value | Name | Description |
|-------|--------------------------------|--|
| 6'h0 | SPC_SR_OPERATION_SUCCESS | Operation Successful |
| 6'h1 | SPC_SR_INVALID_ARR_AY_ID | Invalid Array ID for given command |
| 6'h2 | SPC_SR_INVALID_2_B_YTE_KEY | Invalid 2-byte key |
| 6'h3 | SPC_SR_ADDR_ARRAY_IS_ASLEEP | Addressed Array is Asleep |
| 6'h4 | SPC_SR_EXTERNAL_ACCESS_FAILURE | External Access Failure (SPC is not in external access mode) |
| 6'h5 | SPC_SR_INVALID_N_VALUE | Invalid N Value for given command |

1.3.178 SPC_SR (continued)

Table 1-106. Bit field encoding: SPC_SR_STATUS_CODE_ENUM

| | | |
|-------|---------------------------------------|--|
| 6'h6 | SPC_SR_TEST_MODE_FAILURE | Test Mode Failure (SPC is not in test mode) |
| 6'h7 | SPC_SR_SMART_WRIT_E_ALGO_CHKSUM | Smart Write Algorithm Checksum Failure |
| 6'h8 | SPC_SR_SMART_WRIT_E_PARAM_CHKSUM | Smart Write Parameter Checksum Failure |
| 6'h9 | SPC_SR_PROTECTION_CHK_FAILURE | Protection Check Failure: protection settings are in a state which prevents the given command from executing |
| 6'hA | SPC_SR_INVALID_ADD_R_PARAM | Invalid Address parameter for the given command |
| 6'hB | SPC_SR_INVALID_CM_D_CODE | Invalid Command Code |
| 6'hC | SPC_SR_INVALID_RO_W_ID | Invalid Row ID parameter for given command |
| 6'hD | SPC_SR_INVALID_INP_UT_GET_TEMP_ADC | Invalid input value for Get Temp & Get ADC commands |
| 6'hE | SPC_SR_TMP_SENTO_R_VBR_DRIVEN_EXT_DEV | Tempsensor Vbe is currently driven to an external device |
| 6'hF | SPC_SR_INVALID_SPC_STATE | Invalid SPC state (M8G's PC value out of range. Manual SPC Reset required) |
| 6'h10 | SPC_SR_START_RAN_GE_SMART_WRITE | START RANGE: Smart Write return codes (only when using Smart Write algorithm) SWU-016.1 for exact definitions |
| 6'h3F | SPC_SR_END_RANGE_SMART_WRITE | END RANGE: Smart Write return codes (only when using Smart Write algorithm) SWU-016.1 for exact definitions |
| 6'h20 | SPC_SR_PEP_PROGR_AM_FAILURE | PEP Program Failure (only when using PEP algorithm): Data Verification Failure (row latch checksum != programmed row checksum) |

1.3.179 SPC_CR

SPC Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_CR: 0x40004723

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|------|------------------------|------------------|
| SW Access:Reset | NA:0000 | | | | R:0 | NA:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R/W | NA | R | R/W |
| Name | | | | | SPC_CTRL | | SPC_Busclock_Frequency | SPC_Manual_Reset |

This register contains control bits for the SPC. This register is reset upon assertion of the SPC_Manual_Reset bit.

| Bits | Name | Description |
|------|------------------------|--|
| 3 | SPC_CTRL | This is a status bit that defines which SPC data register (SPC.CPU_DATA or SPC.DMA_DATA) was or is currently being used to send a command to the SPC. When one of the two data registers has the first byte of the SPC 2-byte command key written to it, that register now has temporary control of the SPC. Upon this register write, this bit is set accordingly. All subsequent register writes to the other data register are ignored until the command completes. |
| 1 | SPC_Busclock_Frequency | This is an internal bit. The bit is used to define the frequency of the bus (AHB) clock. The SPC uses this bit to determine the number of stall cycles when accessing the Flash. The bit should not be set when accessing EEPROM. When this bit is set EEPROM accesses are not timed properly which can result in incorrect read and write transactions. See Table 1-107. |
| 0 | SPC_Manual_Reset | Setting this bit manually resets the SPC. The SPC hardware automatically clears the bit after being held high for 2 cycles of the AHB Bus Clock. See Table 1-108. |

Table 1-107. Bit field encoding: SPC_BUSFREQ_ENUM

| Value | Name | Description |
|-------|------------------|---|
| 1'h0 | SPC_BUSFREQ_LOW | Tells the SPC that the Bus Clock Frequency is: 50 < Frequency <= 100. |
| 1'h1 | SPC_BUSFREQ_HIGH | Tells the SPC that the Bus Clock Frequency is: Frequency <= 50. |

Table 1-108. Bit field encoding: SPC_RESET_ENUM

| Value | Name | Description |
|-------|--------------|----------------------------------|
| 1'h0 | SPC_RST_LOW | SPC is in normal execution mode. |
| 1'h1 | SPC_RST_HIGH | SPC is in a reset state. |

1.3.180 SPC_DMM_MAP_SRAM[0..127]

SPC Direct Memory Mapping

Reset: N/A

Register : Address

SPC_DMM_MAP_SRAM: 0x40004780-0x400047FF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | spcsramdata | | | | | | | |

Maps one of 5 possible 128-byte pages from the 128-Data Store SRAM or 512-byte Code Store SRAM

| Bits | Name | Description |
|------|------------------|------------------|
| 7:0 | spcsramdata[7:0] | (no description) |

1.3.181 CACHE_CC_CTL

Cache Control Register

Reset: Reset Signals Listed Below

Register : Address

CACHE_CC_CTL: 0x40004800

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|-------------------|-------|---|-------|--------------|--------|
| SW Access:Reset | R/W:00 | | R/W:0 | NA:00 | | R/W:0 | R:U | R/W:0 |
| HW Access | R | | R | NA | | R/W | R/W | R/W |
| Name | FLASH_CYCLES | | FLASH_CYCLES_ADD4 | | | FLUSH | FLASH_LOWPWR | ENABLE |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:11111111 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | LP_MODE | | | | | | | |

CC_CTL is used to configure the behavior of the cache.

| Bits | Name | Description |
|------|-------------------|--|
| 15:8 | LP_MODE[7:0] | 0x0 - 0xfe: Specifies the number of cache hits after which the cache controller 0xff: Low Power Mode disabled. Assert SLEEP_REQ which will put the FLASH into a low-power mode. To put the FLASH immediately into a low-power state, set LP_MODE to 0. Normally this should only be done when executing code from SRAM. |
| 7:6 | FLASH_CYCLES[1:0] | Specifies the number of clock cycles the cache will wait before it samples data coming back from Flash. 0x1: 1 cycle. -> 0 MHz - 16 MHz 0x2: 2 cycles. -> 16 MHz - 33 MHz 0x3: 3 cycles. -> 33 MHz - 50 MHz 0x0: 4 cycles. -> 50 MHz - 67 MHz |
| 5 | FLASH_CYCLES_ADD4 | Adds 4 extra cycles to the FLASH_CYCLES setting to allow for extra margin and/or for higher frequency binning. 0 = no additional cycles added to FLASH_CYCLES. 1 = 4 extra cycles added to FLASH_CYCLES. |
| 2 | FLUSH | Writing a 1 will cause the cache to be flushed. All entries in the cache are invalidated on the next clock cycle. Note that invalidating the cache must be done with care as the prefetch logic in the CM3 will have already fetched several instructions before the write to this register is executed. Either a string of NOPs or other special instructions are required to insure data integrity. Reading this bit will always return 0 as the bit is automatically cleared once the cache has been flushed. Also, note the PHUB prefetch buffer is flushed with this bit. |
| 1 | FLASH_LOWPWR | 0=FLASH is at full power and ready for access. 1=FLASH is in a low-power mode and will take several microseconds on the first access. See the description for LP_MODE for more details on when FLASH is in a low-power mode. Note that this is a read-only bit. |
| 0 | ENABLE | 0=disable CACHE. 1=enable CACHE. |

1.3.181 CACHE_CC_CTL (continued)

Reset Table

| resetsignal | field(s) |
|---|--|
| N/A | FLASH_LOWPWR |
| System reset for retention flops [reset_all_retention] | ENABLE, FLUSH, FLASH_CYCLES_AD D4, FLASH_CYCLES[1:0], LP_MODE[7:0] |

0x40004880

1.3.182 CACHE_ECC_CORR

Error Correction detected

Reset: Reset Signals Listed Below

Register : Address

CACHE_ECC_CORR: 0x40004880

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|------|---------|-----------|
| SW Access:Reset | R/W:00000 | | | | | NA:0 | R/W:0 | R/W:0 |
| HW Access | R/W | | | | | NA | R/W | R/W |
| Name | ECC_ADDR | | | | | | INT_ENB | INT_VALID |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ECC_ADDR | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ECC_ADDR | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ECC_ADDR | | | | | | | |

A Single Bit error was detected and corrected. The address where the error occurred is stored in this register. An ECC correction at address 0x1234_5678 would result in this register containing 0x1234_567b. Note that the 3 LSBs have the INT_VALID, INT_ENB and a reserved bit in them. Note that the interrupts from all sources within the cache are logically ORed together. Software must read all of the registers to determine which interrupts have caused the interrupt.

| Bits | Name | Description |
|------|----------------|--|
| 31:3 | ECC_ADDR[28:0] | Flash address where error was detected and corrected. Note that the 3 LSBs are not captured but contain the fields above. |
| 1 | INT_ENB | 0=Disable interrupt. 1=Enable interrupt on ECC correction. This bit is logically ANDed with INT_VALID before the interrupt is sent to the CPU. |
| 0 | INT_VALID | 0=ECC_ADDR field is invalid. No ECC correction has occurred. 1=ECC_ADDR field contains the address where a single bit error was detected. ECC_ADDR is frozen until INT_VALID is written with a 0. |

Reset Table

| resetsignal | field(s) |
|-------------|----------|
|-------------|----------|

1.3.182 CACHE_ECC_CORR (continued)

Reset Table

| | |
|--------------------------------|----------------|
| System reset for retention | INT_ENB |
| flops | |
| [reset_all_retention] | |
| Domain reset for non-retention | INT_VALID, |
| flops | ECC_ADDR[28:0] |
| [reset_all_nonretention] | |
|] | |

0x40004888

1.3.183 CACHE_ECC_ERR

Error Correction failed

Reset: Reset Signals Listed Below

Register : Address

CACHE_ECC_ERR: 0x40004888

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|------|---------|-----------|
| SW Access:Reset | R/W:00000 | | | | | NA:0 | R/W:0 | R/W:0 |
| HW Access | R/W | | | | | NA | R/W | R/W |
| Name | ERR_ADDR | | | | | | INT_ENB | INT_VALID |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ERR_ADDR | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ERR_ADDR | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ERR_ADDR | | | | | | | |

A multi-Bit error was detected and cannot be corrected. The address where the error occurred is stored in this register.

| Bits | Name | Description |
|------|----------------|--|
| 31:3 | ERR_ADDR[28:0] | Flash address where error was detected. Note that the LSBs of the address are dropped since FLASH is 64 bits wide. The INT_VALID and INT_ENB and a reserved bit are in the 3 LSBs. |
| 1 | INT_ENB | 0=Disable interrupt. 1=Enable interrupt on ECC error. This bit is logically ANDed with INT_VALID before the interrupt is sent to the CPU. |
| 0 | INT_VALID | 0=ERR_ADDR field is invalid. No ECC detection has occurred. 1=ERR_ADDR field contains the address where a multi-bit error was detected. ERR_ADDR is frozen until INT_VALID is written with a 0. |

Reset Table

| resetsignal | field(s) |
|--|----------|
| System reset for retention flops [reset_all_retention] | INT_ENB |

1.3.183 **CACHE_ECC_ERR** (continued)

Reset Table

```
Domain reset for non- INT_VALID,  
retention          flops ERR_ADDR[28:0]  
[reset_all_nonretention  
]
```

0x40004890

1.3.184 CACHE_FLASH_ERR

FLASH error

Reset: Reset Signals Listed Below

Register : Address

CACHE_FLASH_ERR: 0x40004890

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|------|---------|-----------|
| SW Access:Reset | R/W:00000 | | | | | NA:0 | R/W:0 | R/W:0 |
| HW Access | R/W | | | | | NA | R/W | R/W |
| Name | ERR_ADDR | | | | | | INT_ENB | INT_VALID |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ERR_ADDR | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ERR_ADDR | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ERR_ADDR | | | | | | | |

Attempted write to Flash error. FLASH cannot be written to via the PHUB port. Only the SPC can write to FLASH. Typically this indicates that the code has failed and should be reset.

| Bits | Name | Description |
|------|----------------|---|
| 31:3 | ERR_ADDR[28:0] | Flash address where error was detected. Note that the 3 LSBs are not captured but contain the fields above. |
| 1 | INT_ENB | 0=Disable interrupt. 1=Enable interrupt on FLASH write error. This bit is logically ANDed with INT_VALID before the interrupt is sent to the CPU. |
| 0 | INT_VALID | 0=ERR_ADDR field is invalid. 1=ERR_ADDR field contains the address where a write to flash was attempted. ERR_ADDR is frozen until INT_VALID is written with a 0. |

Reset Table

| resetsignal | field(s) |
|--|----------|
| System reset for retention flops [reset_all_retention] | INT_ENB |

1.3.184 **CACHE_FLASH_ERR** (continued)

Reset Table

```
Domain reset for non- INT_VALID,  
retention          flops ERR_ADDR[28:0]  
[reset_all_nonretention  
]
```

1.3.185 CACHE_HITMISS

HIT/MISS counters

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_HITMISS: 0x40004898

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | MISS_COUNT | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | MISS_COUNT | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | HIT_COUNT | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | HIT_COUNT | | | | | | | |

This register contains two 16-bit counters which count the number of cache hits and misses. The hit/miss ratio can be used to optimize code performance by analyzing where the code misses cache. When the cache misses, a fetch from FLASH is required which typically takes several wait states. Minimizing the cache misses will improve performance. If excessive cache misses are determined for a particular section of code, the code can either be rewritten to fit better in cache or relocate speed critical code to SRAM. To measure cache performance, the HITMISS register should be written with 0 at the start of a block of code to be measured. Then the code is executed and at the end of the code under measurement, the HITMISS register will be read. The cache hit ratio is computed with: $\text{hit\%} = \text{HITMISS}[31:16] * 100 / (\text{HITMISS}[31:16] + \text{HITMISS}[15:0])$; Note that when either the HIT_COUNT or MISS_COUNT register reaches their maximum value, both counters will stop counting. This allows the HIT/MISS ratio to be computed even if there are more than 64K hits/misses from the start of the code to the end. However the computation will only include the first 64K hits or misses from when the counter was zeroed. Often an interrupt service routine can be triggered at regular intervals and measure the hit/miss ratio over time as the code is being executed.

| Bits | Name | Description |
|------|------|-------------|
|------|------|-------------|

1.3.185 CACHE_HITMISS (continued)

| | | |
|-------|------------------|--|
| 31:16 | HIT_COUNT[15:0] | <p>The HIT_COUNT register operates in 2 modes based on the value in LP_MODE of the cache control register (CC_CTL.LP_MODE).</p> <p>When LP_MODE is 0xff, HIT_COUNT will increment every time cache is able to provide the data to the CPU from its local copy of the FLASH data (a cache hit). Once the maximum value of either HIT_COUNT or MISS_COUNT is reached, HIT_COUNT will stop counting. Writing a 0 will clear the counter but always write all 32-bits to insure both counters are cleared at the same time. When LP_MODE is any value other than 0xff, the HIT_COUNT is reserved for internal use. HIT_COUNT in this mode is used to keep track of the number of hits from the last MISS. When HIT_COUNT=LP_MODE, then the FLASH is put into a low-power mode until a MISS occurs. Note that HIT_COUNT becomes read-only when LP_MODE!=0xff.</p> |
| 15:0 | MISS_COUNT[15:0] | <p>The MISS_COUNT register operates only when LP_MODE is equal to 0xff. The counter is incremented each time the cache controller has to fetch data from FLASH. When either MISS_COUNT or HIT_COUNT reaches the maximum count value of 0xffff, then both counters stop counting. Writing a 0 will clear MISS_COUNT and enable counting.</p> |

1.3.186 I2C_XCFG

I2C Extended Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_XCFG: 0x400049C8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|--------|----------------|------------|--------|---|---|------------|
| SW Access:Reset | R/W:0 | R/W:0 | R:0 | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | R | R | R/W | R/W | NA | | | R |
| Name | csr_clk_en | i2c_on | ready_to_sleep | force_nack | | | | hw_addr_en |

This register configures enhanced features. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Always write reserved bits with a value of '0'. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|----------------|---|
| 7 | csr_clk_en | This bit is used for gating system clock for the blocks core logic that is not associated with AHB interface. Clock is made available to the core logic only when this bit is set to 1 and the input pin ext_clk_en is also active. If either of them is not active, the blocks core logic does not receive the system clock. See Table 1-109. |
| 6 | i2c_on | This bit should be set by the user during initial block configuration if the user wants to use the I2C block as wake-up source. Only when this bit set along with other bits mentioned in the sleep mode section, the I2C wakes up system from sleep on address match. |
| 5 | ready_to_sleep | Once the user sets the force_nack bit, the I2C block sets this bit if I2C is not busy or it waits for ongoing transaction to be completed and then sets this bit. As long as this bit is set, the I2C block is going to nack all the transactions. Clearing force_nack bit automatically clears this bit. HW clears this bit automatically on assertion of PD (Power Down) |
| 4 | force_nack | This bit must be set by the user before putting the device to sleep and wait for ready_to_sleep status bit to be set. This can be cleared by user by writing '0' and the HW clears it automatically on assertion of PD(Power Down) |
| 0 | hw_addr_en | When this bit is set to a '1', hardware address compare is enabled. On an address match, an interrupt is generated, CSR register bit 3 is set, and the clock is stalled until the CPU writes a 0 into the CSR register bit 3. The address is automatically ACKed on a match. On an address mismatch, no interrupt is generated, clock is not stalled, and bit 3 in the CSR register is set. The CPU must write a 0 into the CSR register bit 3 to clear it. The address is automatically NACKed on a mismatch. You must configure the compare address in the ADR register. When this bit is set to a '0', software address compare is enabled. An interrupt is generated, the clock is stalled, and CSR register bit 3 is set when the received address byte is available in the Data register; to enable the CPU to do a firmware address compare. The clock is stalled until the CPU writes a 0 into the CSR register bit 3. The functionality of this bit is independent of the data buffering mode. See Table 1-110. |

Table 1-109. Bit field encoding: csr_clk_en_enum

| Value | Name | Description |
|-------|------------|--|
| 1'b1 | CSR_CLK_EN | CLK gating for block core logic is enabled |

1.3.186 I2C_XCFG (continued)

Table 1-109. Bit field encoding: csr_clk_en_enum

| | | |
|------|-------------|---|
| 1'b0 | CSR_CLK_DIS | CLK gating for blobk core logic is disabled |
|------|-------------|---|

Table 1-110. Bit field encoding: hw_addr_en_enum

| Value | Name | Description |
|-------|-------------|-----------------------------------|
| 1'b1 | HW_ADDR_EN | HW Address comparison is enabled |
| 1'b0 | HW_ADDR_DIS | HW Address comparison is disabled |

1.3.187 I2C_ADR

I2C Slave Address Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_ADR: 0x400049CA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register holds the slave's 7-bit address. When hardware address compare mode is not enabled in the XCFG register, this register is not in use. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Always write reserved bits with a value of '0'. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|--------------------|---|
| 6:0 | slave_address[6:0] | These seven bits hold the slave's own device address. |

1.3.188 I2C_CFG

I2C Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_CFG: 0x400049D6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---------|--------------|---------|------|------------|---------|----------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | NA | R | R | R |
| Name | sio_select | pselect | bus_error_ie | stop_ie | | clock_rate | en_mstr | en_slave |

This register is used to set the basic operating modes, baud rate, and interrupt selection. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Always write reserved bits with a value of '0'. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|--------------|---|
| 7 | sio_select | I2C Pin Select for SCL/SDA lines from SIO1/SIO2, 0 = SCL and SDA lines get their inputs from SIO1 module.sclk_str1 and sda_ack1 are driven to SIO1 module and they get asserted once device wakes up from sleep. 1 = SCL and SDA lines get their inputs from SIO2 module. sclk_str2 and sda_ack2 are driven to SIO2 module and they get asserted once device wakes up from sleep. This bit is valid only when I2C.CFG[6] is asserted. See Table 1-116. |
| 6 | pselect | I2C Pin Select for SCL/SDA lines from GPIO/SIO, 0 = SCL and SDA lines get their inputs from GPIO module.sclk_str0 and sda_ack0 are driven to GPIO module and they get asserted once device wakes up from sleep. 1 = SCL and SDA lines get their inputs from one of the SIO Blocks that is chosen based on the configuration of bit I2C.CFG[7] See Table 1-115. |
| 5 | bus_error_ie | Bus Error Interrupt Enable 0 disabled 1 enabled. An interrupt is generated on the detection of a Bus error condition. See Table 1-111. |
| 4 | stop_ie | Stop Interrupt Enable 0 disabled 1 enabled. An interrupt is generated on the detection of a Stop condition. See Table 1-117. |
| 2 | clock_rate | 0 Samples/bit is 16, 1 Samples/bit is 32 See Table 1-112. |
| 1 | en_mstr | 0 Disabled 1 enabled See Table 1-113. |
| 0 | en_slave | 0 Disabled 1 enabled See Table 1-114. |

Table 1-111. Bit field encoding: bus_error_ie_enum

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.188 I2C_CFG (continued)

Table 1-111. Bit field encoding: bus_error_ie_enum

| | | |
|------|------------------|---------------------------------|
| 1'b1 | BUS_ERROR_IE_EN | Bus Error Interrupt is enabled |
| 1'b0 | BUS_ERROR_IE_DIS | Bus Error Interrupt is disabled |

Table 1-112. Bit field encoding: clock_rate_enum

| Value | Name | Description |
|-------|--------|--|
| 1'b0 | RATE_1 | Samples/bit is 16. For 100K Standard mode OR 400K Fast mode. |
| 1'b1 | RATE_2 | Samples/bit is 32. For 50K Standard mode. |

Table 1-113. Bit field encoding: en_mstr_enum

| Value | Name | Description |
|-------|------------|--|
| 1'b1 | MASTER_EN | Master mode is enabled for the device |
| 1'b0 | MASTER_DIS | Master mode is disabled for the device |

Table 1-114. Bit field encoding: en_slave_enum

| Value | Name | Description |
|-------|-----------|---------------------------------------|
| 1'b1 | SLAVE_EN | Slave mode is enabled for the device |
| 1'b0 | SLAVE_DIS | Slave mode is disabled for the device |

Table 1-115. Bit field encoding: pselect_enum

| Value | Name | Description |
|-------|-------------|---|
| 1'b1 | PSELECT_EN | SCL/SDA lines get their inputs from SIO blocks |
| 1'b0 | PSELECT_DIS | SCL/SDA lines get their inputs from GPIO blocks |

Table 1-116. Bit field encoding: sio_select_enum

| Value | Name | Description |
|-------|----------------|--|
| 1'b1 | SIO_SELECT_EN | SCL/SDA lines get their inputs from SIO2 block |
| 1'b0 | SIO_SELECT_DIS | SCL/SDA lines get their inputs from SIO1 block |

Table 1-117. Bit field encoding: stop_ie_enum

| Value | Name | Description |
|-------|-------------|----------------------------|
| 1'b1 | STOP_IE_EN | Stop Interrupt is enabled |
| 1'b0 | STOP_IE_DIS | Stop Interrupt is disabled |

1.3.189 I2C_CSR

I2C Control and Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_CSR: 0x400049D7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|----------|-------------|-------|---------|----------|---------|---------------|
| SW Access:Reset | R/WZC:0 | R/W:0 | R/WZC:0 | R/W:0 | R/WZC:0 | R/W:0 | R/WZC:0 | R/WZC:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | bus_error | lost_arb | stop_status | ack | address | transmit | lrb | byte_complete |

This register is used by the slave to control the flow of data bytes and to keep track of the bus state during a transfer. Bits in this register are held in reset until one of the enable bits in CFG is set. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|---------------|--|
| 7 | bus_error | 0 Status bit. It must be cleared by firmware by writing a '0' to the bit position. It is never cleared by the hardware. 1 a misplaced Start or Stop condition was detected. |
| 6 | lost_arb | 0 This bit is set immediately on lost arbitration; however, it does not cause an interrupt. This status may be checked after the following Byte Complete interrupt. Any Start detect or a write to the Start or Restart generate bits (MCSR register), when operating in Master mode, will also clear the bit. 1 lost Arbitration |
| 5 | stop_status | 0 Status bit. It must be cleared by firmware with write of '0' to the bit position. It is never cleared by the hardware. 1 a Stop condition was detected. |
| 4 | ack | Acknowledge Out. Bit is automatically cleared by hardware on a Byte Complete event. 0 nack the last received byte. 1 ack the last received byte |
| 3 | address | 0 Status bit. It must be cleared by firmware with write of '0' to the bit position. 1 the received byte is a slave address. |
| 2 | transmit | Bit is set by firmware to define the direction of the byte transfer. Any Start detect will clear the bit. 0 receive mode 1 transmit mode See Table 1-118. |
| 1 | lrb | Last Received Bit. The value of the 9th bit in a Transmit sequence, which is the acknowledge bit from the receiver. Any Start detect or a write to the Start or Restart generate bits, when operating in Master mode, will also clear the bit. 0 last transmitted byte was ACK'ed by the receiver. 1 last transmitted byte was NACK'ed by the receiver. |
| 0 | byte_complete | Transmit/Receive Mode: 0 no completed transmit/receive since last cleared by firmware. Any Start detect or a write to the start or Restart generate bits, when operating in Master mode, will also clear the bit. Transmit mode: 1 eight bits of data have been transmitted and an ACK or NACK has been received. Receive mode: 1 eight bits of data have been received. |

Table 1-118. Bit field encoding: transmit_enum

| Value | Name | Description |
|-------|--------------|---------------------------------------|
| 1'b1 | TRANSMIT_EN | Bytes are transferred from the device |
| 1'b0 | TRANSMIT_DIS | Bytes are received from the device |

1.3.190 I2C_D

I2C Data Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_D: 0x400049D8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data | | | | | | | |

This register provides read/write access to the Shift register. This register is read only for received data and write only for transmitted data. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|-----------|---|
| 7:0 | data[7:0] | Read received data or write data to transmit. |

1.3.191 I2C_MCSR

I2C Master Control and Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_MCSR: 0x400049D9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|----------|----------|-------------|-------------|-----------|
| SW Access:Reset | NA:000 | | | R/W:0 | R:0 | R:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R/W | R/W | R/W | R/W | R/W |
| Name | | | | stop_gen | bus_busy | master_mode | restart_gen | start_gen |

This register implements I2C framing controls and provides Bus Busy status. Bits in this register are held in reset until one of the enable bits in CFG is set. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|-------------|---|
| 4 | stop_gen | This bit is set only for master transmitter and used at the end of byte transfer. After byte complete status is set, if this bit is set followed by the Transmit bit in I2C.CSR register, Stop condition is generated after byte complete. This bit is automatically reset to 0 after the Stop, start or Restart has been generated. During data phase, if Stop Gen bit is set to 0, clearing the Transmit bit in I2C.CSR register will also generate a Stop condition. |
| 3 | bus_busy | This bit is set to the following. 0 when a Stop condition is detected (from any bus master). 1 when a Start condition is detected (from any bus master). |
| 2 | master_mode | This bit is set/cleared by hardware when the device is operating as a master. 0 stop condition detected, generated by this device. 1 start condition detected, generated by this device. |
| 1 | restart_gen | This bit is cleared by hardware when the Restart generation is complete. 0 restart generation complete. 1 generate a Restart condition. |
| 0 | start_gen | This bit is cleared by hardware when the Start generation is complete. 0 start generation complete. 1 generate a Start condition and send a byte (address) to the I2C bus, if bus is not busy. |

1.3.192 I2C_CLK_DIV1

I2C Clock Divide Factor Register-1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_CLK_DIV1: 0x400049DB

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | divide_factor_1 | | | | | | | |

This register has the 8 LSB bits of the 10-bit Clock Divider. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|----------------------|--|
| 7:0 | divide_factor_1[7:0] | The configuration of this register along with that in register CLK_DIV2 defines the factor by which the SYSCLK will be divided in the I2C block. |

1.3.193 I2C_CLK_DIV2

I2C Clock Divide Factor Register-2

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_CLK_DIV2: 0x400049DC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|-----------------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | divide_factor_2 | |

This register has the 2 MSB bits of the 10-bit Clock Divider. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|----------------------|--|
| 1:0 | divide_factor_2[1:0] | The configuration of this register along with that in register CLK_DIV1 defines the factor by which the SYSCLK will be divided in the I2C block. |

1.3.194 I2C_TMOUT_CSR

I2C TIMEOUT CSR.

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_TMOUT_CSR: 0x400049DD

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------------|----------------|------------------------|------------------------|------------------------|
| SW Access:Reset | R:000 | | | R:1 | R:1 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | | | R/W | R/W | R | R | R |
| Name | Reserved | | | sda_pin_status | scl_pin_status | i2c_timeout_int_enable | i2c_sda_timeout_enable | i2c_scl_timeout_enable |

I2C TIMEOUT Configuration and Status Register. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|------------------------|------------------------------|
| 7:5 | Reserved[2:0] | Reserved |
| 4 | sda_pin_status | SDA Line status |
| 3 | scl_pin_status | SCL Line status |
| 2 | i2c_timeout_int_enable | I2C Timeout interrupt enable |
| 1 | i2c_sda_timeout_enable | I2C SDA Timeout enable |
| 0 | i2c_scl_timeout_enable | I2C SCL Timeout enable |

1.3.195 I2C_TMOUT_SR

I2C TIMEOUT SR.

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_TMOUT_SR: 0x400049DE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---|------------------|------------------|
| SW Access:Reset | R:000000 | | | | | | R/WOC:0 | R/WOC:0 |
| HW Access | R | | | | | | R/W | R/W |
| Name | Reserved | | | | | | sda_tmout_status | scl_tmout_status |

I2C TIMEOUT status for SCL, SDA lines Register. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|------------------|--------------------|
| 7:2 | Reserved[5:0] | Reserved |
| 1 | sda_tmout_status | SDA Timeout status |
| 0 | scl_tmout_status | SCL Timeout status |

1.3.196 I2C_TMOUT_CFG0

I2C TIMEOUT Period Configuration

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_TMOUT_CFG0: 0x400049DF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:11111111 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | timeout_period_lowbyte | | | | | | | |

I2C TIMEOUT period configuration period Lower Byte register. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|-----------------------------|--------------------|
| 7:0 | timeout_period_lowbyte[7:0] | SCL Timeout status |

1.3.197 I2C_TMOUT_CFG1

I2C TIMEOUT Period Configuration

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_TMOUT_CFG1: 0x400049E0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---------------------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R/W:1111 | | | |
| HW Access | R | | | | R | | | |
| Name | Reserved | | | | timeout_period_highnibble | | | |

I2C TIMEOUT period configuration period Higher Nibble register. Note this register is on reset_all_nonretention by default. However, if PWRSYS.CR1.i2creg_backup = 1 then this register is effectively on reset_all_retention.

| Bits | Name | Description |
|------|---------------------------------|--------------------|
| 7:4 | Reserved[3:0] | Reserved |
| 3:0 | timeout_period_highnibble [3:0] | SCL Timeout status |

1.3.198 DEC_CR

Decimator Control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_CR: 0x40004E00

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|--------|---------|---------|-----------|---|-----------|------------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | | R | R/W |
| Name | sat_en | fir_en | ocor_en | gcor_en | conv_mode | | xstart_en | start_conv |

This register provides information about start, stop, mode, and feature enables. A read of this register produces the last value written to this register with the exception of bit 0. If a 1 is read from bit 0 and conv_mode doesn't = 00 this indicates the filter is running. If a 0 is read and conv_mode doesn't = 00 the block is in the standby state. If conv_mode = 00 bit 0 has no meaning and could be 1 or 0.

| Bits | Name | Description |
|------|---------|---|
| 7 | sat_en | Controls saturation logic in the Post Processing filter. When enabled, the resulting outputs of the Post Processing filter are held to the most positive or negative values, rather than wrapping around. Conversion results are unpredictable if this bit is changed while the Post Processing filter is running. This bit is ignored if FIR_EN, OCOR_EN and GCOR_EN are all 0. This feature is used to prevent wrap-around if the Decimator is mis-configured when using the Post Processor. NOTE: This is different from the Overflow Correction described in DR2H. See Table 1-123. |
| 6 | fir_en | Controls whether or not Post Processing filter implements a FIR filter. If this bit is set it enables the Post Processing filter. Conversion results are unpredictable if this bit is changed while the filter is running. The decimation period of this filter is controlled by the DR2 bits in register DR2 and DR2H. See Table 1-120. |
| 5 | ocor_en | This bit controls the offset correction feature of the Post Processing filter. If this bit is set it enables the Post Processing filter. The offset value is programmed in the OCOR bits of registers OCOR, OCORM and OCORH. Conversion results are unpredictable if this bit is changed while the filter is running. See Table 1-122. |
| 4 | gcor_en | This bit controls the gain correction feature of the Post Processing filter. If this bit is set it enables the Post Processing filter. The gain coefficient is programmed in the GCOR bits of registers GCOR and GCORH. Which bits in this 16-bit field that are valid is set in GVAL. Conversion results are unpredictable if this bit is changed while the filter is running. When this feature is enabled, the DR1 register field must be set to a value higher than 32 (worst case) for proper operation. See the DR1 register definition of cases where values less than 32 are allowed. See Table 1-121. |

1.3.198 DEC_CR (continued)

| | | |
|-----|----------------|--|
| 3:2 | conv_mode[1:0] | The value in these two bits controls the sampling mode the Decimator runs in. Single Sample mode resets all values in the ADC path, captures one sample (4 decimation cycles) and returns to the Standby state. Fast Filter mode is a continuous running Single Sample mode - the ADC path being reset between each sample. Continuous mode resets the ADC path, generates a sample and then without resetting the ADC path, generates a new sample every decimation cycle thereafter. Fast FIR mode is the same as the Continuous mode except it resets the ADC channel and starts again at the termination of the DR2 (FIR Filter) period. If Fast FIR mode is selected and FIR Enable is not set in bit 6, Fast FIR and Continuous mode function the same. Conversion results are unpredictable if these bits are changed while the filter is running. See Table 1-119. |
| 1 | xstart_en | Controls whether DSI signal ext_start is active. If XSTART_EN is high, it allows the ext_start input to start a conversion just as START_CONV does. Regardless of the state of this bit, writing to START_CONV will start a conversion. See Table 1-125. |
| 0 | start_conv | A write of 1 to this bit starts a conversion (regardless of the state of XSTART_EN) according to the CONV_MODE set in bits 2, 3. If read, a 1 indicates the filter is running when not in Single Sample mode. If a 0 is read the block is in the standby state when not in Single Sample mode. When in Single Sample mode this bit is cleared shortly after it is written and does not reflect the running state of the Decimator. If the Decimator is running in Single Sample Mode and this bit is written with a 1 the conversion start is queued, and will start then the previous one completes. If a 1 is read from this bit when in Single Sample Mode it indicates a conversion start is queued. Note that the other bits of this CSR are not queued so queued SS Mode starts must set the same bits in this register as the conversion running. If 0 is written to this bit, it forces the block into the Standby start via a soft-reset. This soft-reset works in any mode and at any time and takes a minimum of 1 and maximum of 2 adc_clk cycles to complete. If a 1 is written before the soft-reset has completed, the start is queued and the conversion will start when the soft-reset is complete. See Table 1-124. |

Table 1-119. Bit field encoding: conv_modes_enum

| Value | Name | Description |
|-------|---------------|---------------------|
| 2'b00 | SINGLE_SAMPLE | Single Sample Mode. |
| 2'b01 | FAST_FILTER | Fast Filter Mode. |
| 2'b10 | CONTINUOUS | Continuous Mode. |
| 2'b11 | FAST_FIR | Fast FIR. |

Table 1-120. Bit field encoding: fir_en_enum

| Value | Name | Description |
|-------|---------|-------------------------------|
| 1'b1 | FIR_EN | FIR filter function is on. |
| 1'b0 | FIR_DIS | FIR filter function disabled. |

Table 1-121. Bit field encoding: gcor_en_enum

| Value | Name | Description |
|-------|----------|------------------------------|
| 1'b1 | GCOR_EN | Gain correction enabled. |
| 1'b0 | GCOR_DIS | Default: no gain correction. |

Table 1-122. Bit field encoding: ocor_en_enum

| Value | Name | Description |
|-------|----------|----------------------------|
| 1'b1 | OCOR_EN | Offset correction enabled. |
| 1'b0 | OCOR_DIS | No offset correction. |

Table 1-123. Bit field encoding: sat_en_enum

| Value | Name | Description |
|-------|---------|-----------------------------|
| 1'b1 | SAT_EN | Saturation Control Enabled. |
| 1'b0 | SAT_DIS | No saturation control. |

1.3.198 DEC_CR (continued)

Table 1-124. Bit field encoding: start_conv_enum

| Value | Name | Description |
|-------|-----------|--|
| 1'b1 | DEC_START | Initiate a conversion. |
| 1'b0 | DEC_STOP | Kill current conversion (if running) and enter Standby state (SW reset). |

Table 1-125. Bit field encoding: xstart_en_enum

| Value | Name | Description |
|-------|------------|--|
| 1'b1 | XSTART_EN | Enable the DSI input signal ext_start to start a conversion. |
| 1'b0 | XSTART_DIS | Default: DSI signal ext_start is disabled. |

1.3.199 DEC_SR

Decimator Status Register

Reset: Reset Signals Listed Below

Register : Address

DEC_SR: 0x40004E01

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-----------------|------------|-----------|----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | W:0 | R/W:0 | R:0 |
| HW Access | NA | | R | R | R | R | R | R/W |
| Name | | | coreclk_disable | intr_pulse | out_align | intr_clr | intr_mask | conv_done |

This register provides information about interrupt, polling, status, and control features.

| Bits | Name | Description |
|------|-----------------|---|
| 5 | coreclk_disable | <p>This bit when set high disables (gates off) the clock to the entire core of the block (adc_clk). This includes all FFs except those used for the AHB interface and CSRs. When disabled (set high) the AHB interface to the CSR is still fully functional. This bit is ANDed with the primary input signal cic_clk_en to control the clock gate. cic_clk_en must be high and CoreCLK_Disable must be low for the clock to run.</p> <p>See Table 1-127.</p> |
| 4 | intr_pulse | <p>This read/write bit selects if cic_intr is pulse or level sensed. If level, a sample completion sets cic_intr high where it remains until bit 2 is written, a soft-reset if performed or if OUTSAMP/M/H is read. If pulse, a single cycle (pclk) strobe is generated on cic_intr to be used as an edge sensed interrupt or a DMAREQ. Regardless of which is selected, the interrupt output is still subject to masking by bit 1.</p> <p>See Table 1-130.</p> |
| 3 | out_align | <p>This bit when set high causes a read of OUTSAMP to produce the contents of OUTSAMPM and OUTSAMPM to produce the contents of OUTSAMPH. Effectively, this is an 8-bit right shift of the result. Note that the setting of this bit does not alter the content of the OUTSAMP registers. Setting this bit simply realigns the byte lanes when the register is read. If this bit is set low, the OUTSAMP registers are read normally. This feature is added to allow the SW to read 9 to 16 bit samples from the Decimator in one cycle on bits 15:0. Note also that when using Coherency checking in conjunction with this alignment feature that the Key Coherency Byte selected in the COHER register is referenced based on the address of the register being read, not the content delivered on the bus. This means that if this bit is set high with the intent to read sample data 23:8 on 15:0 that they Key Coherency Byte should be set to either OUTSAMP or OUTSAMPM, not OUTSAMPH.</p> <p>See Table 1-131.</p> |
| 2 | intr_clr | <p>INTR_CLR is a write-only bit that clears bit0 and cic_intr. A read always produces a 0.</p> <p>See Table 1-128.</p> |
| 1 | intr_mask | <p>INTR_MASK is a RD/WR bit that controls the generation of the conversion completion interrupt. A read produces that last value written to this bit. This bit functions as a mask regardless of the value of bit 4 (INTR PULSE).</p> <p>See Table 1-129.</p> |

1.3.199 DEC_SR (continued)

| | | |
|---|-----------|--|
| 0 | conv_done | CONV_DONE is a read-only bit indicating that the most recently started conversion has completed if it has been cleared since the last sample read. This same bit is the interrupt signal cic_intr when bit 4 is low, if not masked by bit 1. This bit is intended to provide a polling mechanism should this be preferred to receiving interrupts. It is cleared by writing a 1 to bit 2, a soft-reset or a read of register OUTSAMP, OUTSAMPM or OUTSAMPH (regardless of Coherency settings). |
|---|-----------|--|

See Table 1-126.

Reset Table

| resetsignal | field(s) |
|--|---|
| System reset for retention [reset_all_retention] | intr_mask, out_align, flops intr_pulse, coreclk_disable |
| Domain reset for non-retention [reset_all_nonretention] | conv_done, intr_clr flops |

Table 1-126. Bit field encoding: conv_done_enum

| Value | Name | Description |
|-------|--------------|---|
| 1'b1 | CONV_COMP | Most recently started conversion completed. |
| 1'b0 | CONV_NOTCOMP | Conversion not completed since last clear. |

Table 1-127. Bit field encoding: coreclk_disable_enum

| Value | Name | Description |
|-------|--------------------------|------------------------|
| 1'b1 | CORECLK_DISABLE_HI GH | Core Clock is Disabled |
| 1'b0 | CORECLK_DISABLE_L OW | Core Clock is Enabled |

Table 1-128. Bit field encoding: intr_clr_enum

| Value | Name | Description |
|-------|------------|--|
| 1'b1 | INTR_CLEAR | Clears CONV_DONE and the interrupt on cic_intr (if enabled). |
| 1'b0 | INTR_NOP | No affect. |

Table 1-129. Bit field encoding: intr_mask_enum

| Value | Name | Description |
|-------|--------------|---|
| 1'b1 | INTR_MASKED | Masks the interrupt generation on cic_intr. |
| 1'b0 | INTR_ENABLED | Allows CONV_DONE to generate an interrupt. |

Table 1-130. Bit field encoding: intr_pulse_enum

| Value | Name | Description |
|-------|------------|--|
| 1'b1 | INTR_PULSE | Selects a pulse interrupt on cic_intr. |
| 1'b0 | INTR_LEVEL | Selects a level interrupt on cic_intr. |

Table 1-131. Bit field encoding: out_align_enum

| Value | Name | Description |
|-------|----------------|---------------------------------------|
| 1'b1 | OUT_ALIGN_HIGH | Shifts SAMP registers right by 8-bits |
| 1'b0 | OUT_ALIGN_LOW | No affect on SAMP Registers |

1.3.200 DEC_SHIFT1

Decimator Shifter 1 (Input)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_SHIFT1: 0x40004E02

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|---|---|---|---|
| SW Access:Reset | NA:000 | | | R/W:00000 | | | | |
| HW Access | NA | | | R | | | | |
| Name | | | | shift1 | | | | |

This register provides control information to the input (left) shifter. SHIFT1 is a 5-bit field that sets the amount of left shift that the Modulator input will be shifted. Disturbing this field during a conversion will disturb the output value. This register should only be updated while the CIC filter is in the Standby state. Conversion results are unpredictable if these bits are changed while the filter is running. Not all values from 0 to 31 make computational sense. A read of this register produces the last value written to this register.

| Bits | Name | Description |
|------|-------------|--|
| 4:0 | shift1[4:0] | Value for left shift amount of modulator input data. 0 = no shift, 1 = left shift by 1 bit, up to the max supported 31. |

1.3.201 DEC_SHIFT2

Decimator Shifter 2 (Output)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_SHIFT2: 0x40004E03

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | shift2 | | | |

This register provides control of the post CIC (output) shifter. This shifter sits at the input of the Post Processor and is only functional on the CIC output sample when the Post Processor is in use. SHIFT2 is a 4-bit field that sets the amount of right shift on the output of the CIC filter as it enters the Post Processor. Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running. Shift2 shifts right by the amount held in this register. Not all values from 0 to 15 make computational sense. A read of this register produces the last value written to this register.

| Bits | Name | Description |
|------|-------------|--|
| 3:0 | shift2[3:0] | Value for the amount of right shift for the output of the CIC filter prior to entering the Post Processor. Functional values range from 0 to 15, 0 = no shift. |

1.3.202 DEC_DR2

Decimator Decimation Rate (2)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_DR2: 0x40004E04

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dr2_low | | | | | | | |

This register provides information to the Post Processor about the decimation rate of the FIR filter. This is a 10-bit field that sets the decimation ratio in the Post Processing filter. The upper 2 bits are found in register DR2H. The decimation ratio minus 1 in binary is the number to program in this 10-bit field. Valid decimation ratios are 2 to 1024. Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running. A read of this register produces the last value written to this register.

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | dr2_low[7:0] | FIR Filter decimation ratio bits [7:0] (of [9:0]). |

1.3.203 DEC_DR2H

Decimator Decimation Rate (2) and Overflow Correction

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_DR2H: 0x40004E05

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|------|----------|---|
| SW Access:Reset | R/W:00000 | | | | | NA:0 | R/W:00 | |
| HW Access | R | | | | | NA | R | |
| Name | of_width | | | | | | dr2_high | |

This register provides information to the Post Processor about the decimation rate of the FIR filter. This is a 10-bit field that sets the decimation ratio in the Post Processing filter. The lower 8 bits are found in register DR2. The decimation ratio minus 1 in binary is the number to program in this 10-bit field. Valid decimation ratios are 2 to 1024. The Overflow Correction Width field is used to correct for 2's complement overflow in output results. For n bit results the CIC filter will create a maximum number of $+2^n$ (for positive ranges) or $+2^{(n-1)}$ (for signed ranges) which both need (n+1) bits to represent. When read truncated to n bits this produces errors in the output range. This field allows SW to program a reference to the size of n and where the n bits are in the output register and it controls correction HW that clamps the output value to $+2^n-1$ and $+2^{(n-1)}-1$, respectively. Changing either of the fields in this register during a conversion will disrupt the output value. Conversion results are unpredictable if this register is changed while the Decimator is running. A read of this register produces the last value written to this register.

| Bits | Name | Description |
|------|---------------|--|
| 7:3 | of_width[4:0] | Occupying the top 5 bits of this register is the Overflow Correction Bit-Width field (it is unrelated to the DR2). This field both enables and sets the bit width of the Overflow Correction logic in the CIC core. With n = number of bits in the sample SW will read from OUTSAMP, the following formula gives the value to program into OF_WIDTH: OF_WIDTH = n-1+s (for signed ranges), OF_WIDTH = n+s (for positive ranges) -- where s = the number of bit positions the result field is left-shifted from the lsb of the OUTSAMP register. Examples: For an 8-bit result that is lsb aligned in OUTSAMP and is signed, n=8, s=0 so: OF_WIDTH = 8-1+0 = 7. For an 8-bit result that is lsb aligned in OUTSAMP and is a positive range: OF_WIDTH = 8+0 = 8. For a signed 12-bit result that is shifted into the high two bytes: OF_WIDTH = 12-1+8 = 19. Functional values of OF_WIDTH are 5 to 22 (6 to 23-bit numbers). Any other value in this field disables the Overflow Correction feature and data is not altered when passing through the Overflow Correction logic. Overflow Correction only works on positive numbers. Example: If OF_WIDTH is set to 7 (for an 8-bit signed value) and given a range of -144 to 144, the 144 will get truncated to 127 but the -144 will not get truncated. |
| 1:0 | dr2_high[1:0] | FIR Filter decimation ratio bits [9:8] (of [9:0]). See description in DR2 register |

1.3.204 DEC_DR1

Decimator Decimation Rate (1) of CIC Filter

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_DR1: 0x40004E06

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dr1 | | | | | | | |

DR1 is an 8-bit field that sets the decimation ratio in the CIC filter. The decimation ratio minus 1 in binary is the number to program in this register. Valid decimation ratios are any value in the range 2 to 256 (program 1-255) for all modes where the Post Processor is not in use. Note this does not mean the results will be valid. For higher levels of input data (moddat), higher DR1 values will saturate the CIC filter and give meaningless results. This is true for any of the 4 modes Single Sample, Continuous, Fast Filter or Fast FIR. Because the Post Processor needs time to perform its enabled calculations, the minimum DR1 for cases where the Post Process is enabled are greater and are a function of what Post Processing features are enabled. These restrictions also apply to SS Mode if started back-to-back or queued. Minimum DR1 values for each are given as: Offset Correction: DR1 \geq 4, FIR (Sync1): DR1 \geq 4, Both Offset and FIR: DR1 \geq 5, Gain Correction: DR1 \geq GVAL + 5, Gain and Offset: DR1 \geq GVAL + 6, Gain and FIR: DR1 \geq GVAL + 6, Gain and Offset and FIR: DR1 \geq GVAL + 7, (where GVAL is the 0-based value programmed into the register). Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running.

| Bits | Name | Description |
|------|----------|-----------------------------|
| 7:0 | dr1[7:0] | CIC Filter decimation rate. |

1.3.205 DEC_OCOR

Decimator Offset Correction Coefficient (Low Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_OCOR: 0x40004E08

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ocor_low | | | | | | | |

OCOR / OCORM / OCORH is a 24-bit 2's compliment signed field that is the offset correction value used if the Post Processor Offset feature is enabled. The field is specified in registers OCOR, OCORM, and OCORH. This register may be written while the filter is running. OCOR, OCORM and OCORH can be coherency interlocked (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the Offset field is written the field is flagged incoherent until the Key Coherency Byte is written. Once the Key Coherency Byte is written the field is flagged coherent again. When not coherent, the HW will not pass any portion of the 24-bit number to the Post Processor. When incoherent, the previous Offset value is used. A new Offset value is accepted when a write to the Key Coherency Byte is seen - as defined in the COHER register. The 3 bytes of the Offset field may be written in any order but the Key Coherency Byte must be written last.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | ocor_low[7:0] | Offset correction coefficient bits [7:0] (of [23:0]). |

1.3.206 DEC_OCORM

Decimator Offset Correction Coefficient (Middle Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_OCORM: 0x40004E09

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ocor_mid | | | | | | | |

See description in OCOR register above.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | ocor_mid[7:0] | Offset correction coefficient bits [15:8] (of [23:0]). |

1.3.207 DEC_OCORH

Decimator Offset Correction Coefficient (High Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_OCORH: 0x40004E0A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ocor_high | | | | | | | |

See description in OCOR register above.

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | ocor_high[7:0] | Offset correction coefficient bits [23:16] (of [23:0]). |

1.3.208 DEC_GCOR

Decimator Gain Correction Coefficient (Low Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_GCOR: 0x40004E0C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | gcor_low | | | | | | | |

GCOR / GCORH is a 16-bit field that is the gain correction value for the Post Processor. The field is specified in registers GCOR and GCORH. This register may be written while the filter is running. If a multiply is in progress, updates to the gain correction value will be ignored until the start of the next multiply. Which bits that are valid in the 16 bit field is signified in the GVAL register. The implementation in HW is a shift_add multiply which consumes a clock cycle (adc_clk) for each valid bit in the GCOR field as defined by GVAL. GCOR, GCORH and GVAL can be coherency interlocked (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the Gain/Gain_Value field is written the field is flagged incoherent until the Key Coherency Byte is written. Once the Key Coherency Byte is written the field is flagged coherent again. When not coherent, the HW will not pass any portion of the 16-bit Gain number or 8-bit Gain Value to the Post Processor. When incoherent, the previous written values are used. A new Gain/Gain_Value is accepted when a write to the Key Coherency Byte is seen - as defined in the COHER register. The 3 bytes of the Gain/Gain_Value field may be written in any order but the Key Coherency Byte must be written last. READ: A read of this register produces the last value written to this register. Reads have no affect on coherency flags.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | gcor_low[7:0] | Gain correction coefficient bits [7:0] (of [15:0]). |

1.3.209 DEC_GCORH

Decimator Gain Correction Coefficient (High Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_GCORH: 0x40004E0D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | gcor_high | | | | | | | |

Seed description of GCOR register above.

| Bits | Name | Description |
|------|----------------|--|
| 7:0 | gcor_high[7:0] | Gain correction coefficient bits [15:8] (of [15:0]). |

1.3.210 DEC_GVAL

Decimator Gain Correction Size Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_GVAL: 0x40004E0E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | gval | | | |

GVAL is a 4-bit field that signifies to the HW how many bits of GCOR field are valid. The number of valid bits minus one should be written (0000b = 1 bit, 1111b = all 16 bits). Updates to this register will be ignored until the start of the next multiply. This register may be written while the filter is running. The valid field is measured from LSB (bit 0) up. Note that the HW always assumes the field specified by GVAL is left justified (starts at bit 0 of GCOR) and has a binary-point after the left-most digit. For example, if GVAL is programmed with a 7d, this means there are 8 valid bits in GCOR and they have the format x.xxxxxxb. If GCOR (GCORH, GCOR) holds the value 00000000 10100000b and GVAL is 7, only the low-order 8 bits are considered (10100000b) and the binary point is assumed after the left-most digit (1.0100000b). The multiply coefficient in the example would be 1.25d. Although a good explanation example, this isn't the most efficient way to multiply by 1.25d. Better would be GCOR (GCORH, GCOR) holds the value 00000000 00000101b and GVAL is 2, which gives (1.01b). Another example: If it is desired to multiply by a gain coefficient of 0.125d (0.001b) then GCOR would be programmed with a value of 00000001b, GCORH with 00000000b and GVAL (GVAL) with 0011b - meaning there are 4 valid bits x.xxxx. The multiplier thus has a coefficient range of $1/(2^{15})$ to $2.0-(1/(2^{15}))$ in steps of $1/(2^{15})$. GCOR, GCORH and GVAL can be coherency interlocked (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the Gain/Gain_Value field is written the field is flagged incoherent until the Key Coherency Byte is written. Once the Key Coherency Byte is written the field is flagged coherent again. When not coherent, the HW will not pass any portion of the 16-bit Gain number or 8-bit Gain Value to the Post Processor. When incoherent, the previous written values are used. A new Gain/Gain_Value is accepted when a write to the Key Coherency Byte is seen - as defined in the COHER register. The 3 bytes of the Gain/Gain_Value field may be written in any order but the Key Coherency Byte must be written last. READ: A read of this register produces the last value written to this register. Reads have no affect on coherency flags.

| Bits | Name | Description |
|------|-----------|--|
| 3:0 | gval[3:0] | Number of valid bits minus one in Gain Coefficient registers GCORH and GCOR. |

1.3.211 DEC_OUTSAMP

Decimator Output Data Sample (Low Byte)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMP: 0x40004E10

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | samp_low | | | | | | | |

This register is read-only and contains the low order byte of the conversion result. In some configurations of the block the output results of interest are placed in bits 23:8 of the output sample field. To allow reading such values in one bus cycle an alignment feature is added to shift the result right by 8-bits. This feature is enabled by the OUTPUT_ALIGN bit of the SR register. This register can be coherency interlock protected (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the OUTSAMP / OUTSAMPM / OUTSAMPH field is read the field is flagged incoherent until the Key Coherency Byte is read. Once the Key Coherency Byte is read the field is flagged coherent again. When the Decimator generates a new sample and the output sample field is coherent, the output sample field is over-written with the new value - regardless of whether it had been read prior or not. If the output sample field is flagged incoherent when the new sample is generated, the new sample is lost and the output sample field is left untouched. There is no warning given when either a new sample is lost or an unread output sample is overwritten. WRITE: This register is read-only - writes to this address complete but have no affect.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | samp_low[7:0] | Low order byte of the filter conversion result, bits [7:0] (of [23:0]) --- Or if the out_align bit is set it contains bits [15:8] (of [23:0]). |

1.3.212 DEC_OUTSAMPM

Decimator Output Data Sample (Middle Byte)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMPM: 0x40004E11

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | samp_middle | | | | | | | |

This register is read-only and contains the middle order byte of the conversion result. In some configurations of the block the output results of interest are placed in bits 23:8 of the output sample field. To allow reading such values in one bus cycle an alignment feature is added to shift the result right by 8-bits. This feature is enabled by the OUTPUT_ALIGN bit of the SR register. This register can be coherency interlock protected (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the OUTSAMP / OUTSAMPM / OUTSAMPH field is read the field is flagged incoherent until the Key Coherency Byte is read. Once the Key Coherency Byte is read the field is flagged coherent again. When the Decimator generates a new sample and the output sample field is coherent, the output sample field is over-written with the new value - regardless of whether it had been read prior or not. If the output sample field is flagged incoherent when the new sample is generated, the new sample is lost and the output sample field is left untouched. There is no warning given when either a new sample is lost or an unread output sample is overwritten. WRITE: This register is read-only - writes to this address complete but have no affect.

| Bits | Name | Description |
|------|------------------|---|
| 7:0 | samp_middle[7:0] | Middle order byte of the filter conversion result, bits [15:8] (of [23:0]) --- Or if the out_align bit is set it contains bits [23:16] (of [23:0]). |

1.3.213 DEC_OUTSAMP

Decimator Output Data Sample (High Byte)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMP: 0x40004E12

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | samp_high | | | | | | | |

This register is read-only and contains the high order byte of the conversion result. This register can be coherency interlock protected (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the OUTSAMP / OUTSAMPM / OUTSAMPH field is read the field is flagged incoherent until the Key Coherency Byte is read. Once the Key Coherency Byte is read the field is flagged coherent again. When the Decimator generates a new sample and the output sample field is coherent, the output sample field is over-written with the new value - regardless of whether it had been read prior or not. If the output sample field is flagged incoherent when the new sample is generated, the new sample is lost and the output sample field is left untouched. There is no warning given when either a new sample is lost or an unread output sample is overwritten. Note that even though there is no register defined for the high byte (address xx13) of this register, if this register is read as a 16-bit access the top byte will contain the sign extension. WRITE: This register is read-only - writes to this address complete but have no affect.

| Bits | Name | Description |
|------|----------------|--|
| 7:0 | samp_high[7:0] | High order byte of the filter conversion result, bits [23:16] (of [23:0]). |

1.3.214 DEC_OUTSAMPS

Decimator Output Data Sample (Sign Extension)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMPS: 0x40004E13

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | samp_signext | | | | | | | |

* This is a pseudo register. There are no FFs or even an address decode for this pseudo register. If read or written as a byte it acts the same as all other unused byte addresses in the block's address space - writes are ignored and reads produce 0 on the bus. However, if OUTSAMPH is read as a 16-bit value, it is sign extended onto the bus on these 8 bits. This pseudo register definition is here simply to document this sign extension functionality. WRITE: This register is read-only - writes to this address complete but have no affect. If read as a byte, it always returns 0. If read as the high byte of a 16-bit read of OUTSAMPH, it always returns the sign extension of the value in OUTSAMP/M/H.

| Bits | Name | Description |
|------|-------------------|--|
| 7:0 | samp_signext[7:0] | Sign extension of the value held in OUTSAMP. |

1.3.215 DEC_COHER

Decimator Coherency Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_COHER: 0x40004E14

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|----------|---|----------|---|----------|---|
| SW Access:Reset | NA:00 | | R/W:00 | | R/W:00 | | R/W:00 | |
| HW Access | NA | | R | | R | | R | |
| Name | | | gcor_key | | ocor_key | | samp_key | |

The three 2-bit fields of this register are used to select which of the 3 bytes (of the OCOR, GCOR/GVAL and OUTSAMP fields) will be used as the Key Coherency Byte (KCB). Or, if no coherency checking is desired, to turn it off. The KCB selected is SW's way of tell the HW which byte of the 3-byte field it will access to signify the completion of a coherent operation. For the OCOR and GCOR/GVAL 3-byte fields, selecting the key byte tells the HW which of the bytes it will write last to note that all of the bytes it wants to update have been written. When any non-Key byte is written, the coherency HW locks the underlying ALU hardware from seeing the potentially incoherent value. While incoherent the ALU uses a shadow copy of the last coherent value received. The SW lastly writes the KCB and the HW flags the field as coherent and the next ALU operation needing that coefficient will get a copy of the newly written value. The OUTSAMP field is basically the same other than it's a read only register and the coherency protects the output sample from being overwritten by a subsequent sample if the present sample is in the process of being read (this is technically an overrun condition). If no byte of the previous sample has been read, a new sample will overwrite the last. If the previous sample is in the process of being read, a new sample will be dropped. Coherency doesn't protect against over/under flow, it only makes sure the sample read is coherent.

| Bits | Name | Description |
|------|---------------|--|
| 5:4 | gcor_key[1:0] | Sets the Key Coherency Byte of the GCOR/GCORH/GVAL field See Table 1-132. |
| 3:2 | ocor_key[1:0] | Sets the Key Coherency Byte of the OCOR/OCORM/OCORH field See Table 1-133. |
| 1:0 | samp_key[1:0] | Sets the Key Coherency Byte of the OUTSAMP/OUTSAMP/OUTSAMP field See Table 1-134. |

Table 1-132. Bit field encoding: gcor_key_enum

| Value | Name | Description |
|-------|---------------|--|
| 2'b00 | GCOR_KEY_OFF | Gain Coefficient Coherency checking off. |
| 2'b01 | GCOR_KEY_LOW | Key Byte is low byte (GCOR). |
| 2'b10 | GCOR_KEY_MID | Key Byte is med byte (GCORH). |
| 2'b11 | GCOR_KEY_HIGH | Key Byte is high byte (GVAL). |

Table 1-133. Bit field encoding: ocor_key_enum

| Value | Name | Description |
|-------|---------------|--|
| 2'b00 | OCOR_KEY_OFF | Offset Coefficient Coherency checking off. |
| 2'b01 | OCOR_KEY_LOW | Key Byte is low byte (OCOR). |
| 2'b10 | OCOR_KEY_MID | Key Byte is med byte (OCORM). |
| 2'b11 | OCOR_KEY_HIGH | Key Byte is high byte (OCORH). |

Table 1-134. Bit field encoding: samp_key_enum

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.215 DEC_COHER (continued)

Table 1-134. Bit field encoding: samp_key_enum

| | | |
|-------|---------------|---------------------------------------|
| 2'b00 | SAMP_KEY_OFF | Output Sample Coherency checking off. |
| 2'b01 | SAMP_KEY_LOW | Key Byte is low byte (OUTSAMP). |
| 2'b10 | SAMP_KEY_MID | Key Byte is med byte (OUTSAMPM). |
| 2'b11 | SAMP_KEY_HIGH | Key Byte is high byte (OUTSAMPH). |

1.3.216 TMR[0..3]_CFG0

Configuration Register CFG0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CFG0: 0x40004F00

TMR1_CFG0: 0x40004F0C

TMR2_CFG0: 0x40004F18

TMR3_CFG0: 0x40004F24

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------------|---|-------|-------|----------|---------|-------|-------|
| SW Access:Reset | R/W:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | | R | R | R | R | R | R |
| Name | DEADBAND_PERIOD | | DB | INV | CMP_BUFF | ONESHOT | MODE | EN |

This register is used to configure the timer block.

| Bits | Name | Description |
|------|----------------------|---|
| 7:6 | DEADBAND_PERIOD[1:0] | Deadband Period |
| 5 | DB | Deadband mode--Deadband phases phi1 and phi2 are outputted on CMP and TC output pins respectively. See Table 1-135. |
| 4 | INV | Invert sense of TIMEREN signal |
| 3 | CMP_BUFF | Buffer compare register. Compare register updates only on timer terminal count. |
| 2 | ONESHOT | Timer stops upon reaching stop condition defined by TMR_CFG bits. Can be restarted by asserting TIMER RESET or disabling and re-enabling block. |
| 1 | MODE | Mode. (0 = Timer; 1 = Comparator) See Table 1-136. |
| 0 | EN | Enables timer/comparator. |

Table 1-135. Bit field encoding: db_enum

| Value | Name | Description |
|-------|----------|--|
| 1'b0 | Timer | CMP and TC are output. |
| 1'b1 | Deadband | PHI1 (instead of CMP) and PHI2 (instead of TC) are output. |

Table 1-136. Bit field encoding: mode_enum

| Value | Name | Description |
|-------|------------|---|
| 1'b0 | Timer | Timer mode. CNT/CMP register holds timer count value. |
| 1'b1 | Comparator | Comparator mode. CNT/CMP register holds comparator threshold value. |

1.3.217 TMR[0..3]_CFG1

Configuration Register CFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CFG1: 0x40004F01

TMR1_CFG1: 0x40004F0D

TMR2_CFG1: 0x40004F19

TMR3_CFG1: 0x40004F25

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|----------------|---|---|--------|-------|-------|---------|
| SW Access:Reset | R/W:0 | R/W:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | | | R | R | R | R |
| Name | BUS_CLK_SEL | CLK_BUS_EN_SEL | | | DBMODE | DCOR | FTC | IRQ_SEL |

This register is used to configure the timer block.

| Bits | Name | Description |
|------|---------------------|--|
| 7 | BUS_CLK_SEL | Bus Clock selection. See Table 1-137. |
| 6:4 | CLK_BUS_EN_SEL[2:0] | Digital Global Clock selection. See Table 1-138. |
| 3 | DBMODE | Deadband mode (asynchronous/synchronous). CMP output pin is also affected when not in deadband mode (CFG0.DEADBAND). See Table 1-139. |
| 2 | DCOR | Disable Clear on Read (DCOR) of Status Register SR0. See Table 1-140. |
| 1 | FTC | First Terminal Count (FTC). Setting this bit forces a single pulse on the TC pin when first enabled. See Table 1-141. |
| 0 | IRQ_SEL | Irq selection. (0 = raw interrupts; 1 = status register interrupts) See Table 1-142. |

Table 1-137. Bit field encoding: bus_sel_enum

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | clk_d | Use the digital clocks, clk_d[*], as system clock. |
| 1'b1 | clk_bus | Use the system bus clock, clk_bus, as system clock. |

Table 1-138. Bit field encoding: clk_cfg_enum

| Value | Name | Description |
|--------|--------|--|
| 3'b000 | clk_d0 | Select digital clock 0, clk_d[0], as clock enable. |
| 3'b001 | clk_d1 | Select digital clock 1, clk_d[1], as clock enable. |
| 3'b010 | clk_d2 | Select digital clock 2, clk_d[2], as clock enable. |
| 3'b011 | clk_d3 | Select digital clock 3, clk_d[3], as clock enable. |
| 3'b100 | clk_d4 | Select digital clock 4, clk_d[4], as clock enable. |
| 3'b101 | clk_d5 | Select digital clock 5, clk_d[5], as clock enable. |
| 3'b110 | clk_d6 | Select digital clock 6, clk_d[6], as clock enable. |
| 3'b111 | clk_d7 | Select digital clock 7, clk_d[7], as clock enable. |

1.3.217 TMR[0..3]_CFG1 (continued)

Table 1-139. Bit field encoding: dbmode_enum

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | Asynchronous | Asynchronous kill: Output is gated off immediately, and restored after a minimum of 1 application clock cycle. |
| 1'b1 | Synchronous | Synchronous kill: Output is gated of immediately, and restored after a minimum of one full counter period (at the terminal count). |

Table 1-140. Bit field encoding: dcor_enum

| Value | Name | Description |
|-------|-----------------------|---|
| 1'b0 | Enable clear on read | Clear status register, SR0, when read. |
| 1'b1 | Disable clear on read | Do not clear status register, SR0, when read. |

Table 1-141. Bit field encoding: ftc_enum

| Value | Name | Description |
|-------|-------------|--|
| 1'b0 | Disable FTC | Disable the single cycle pulse, which signifies the timer is starting. |
| 1'b1 | Enable FTC | Enable the single cycle pulse, which signifies the timer is starting. |

Table 1-142. Bit field encoding: irq_sel_enum

| Value | Name | Description |
|-------|------------|--|
| 1'b0 | Raw IRQ | IRQ from raw signals, maskable by corresponding mask bit in SR0 register. |
| 1'b1 | Status IRQ | IRQ from status signals, maskable by corresponding mask bit in SR0 register. Clear interrupt by writing '0' to corresponding status bit of SR0 register. |

1.3.218 TMR[0..3]_CFG2

Configuration Register CFG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CFG2: 0x40004F02

TMR1_CFG2: 0x40004F0E

TMR2_CFG2: 0x40004F1A

TMR3_CFG2: 0x40004F26

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---------|---|---|-------|-------|---------|---|
| SW Access:Reset | R/W:0 | R/W:000 | | | R/W:0 | R/W:0 | R/W:00 | |
| HW Access | R | R | | | R | R | R | |
| Name | HW_EN | CMP_CFG | | | ROD | COD | TMR_CFG | |

This register is used to configure the timer block.

| Bits | Name | Description |
|------|--------------|---|
| 7 | HW_EN | When set Timer Enable controls counting. |
| 6:4 | CMP_CFG[2:0] | Comparator configuration: 000 = '=='; 001 = '<'; 010 = '<=' 011 = '>'; 100 = '>=' See Table 1-143. |
| 3 | ROD | Reset On Disable (ROD). Resets internal state of output logic. |
| 2 | COD | Clear On Disable (COD). Clears or gates outputs to zero. |
| 1:0 | TMR_CFG[1:0] | Timer configuration (MODE = 0): 000 = Continuous; 001 = Pulsewidth; 010 = Period; 011 = Stop on IRQ See Table 1-144. |

Table 1-143. Bit field encoding: cmp_cfg_enum

| Value | Name | Description |
|--------|-----------------------|---|
| 3'b000 | Equal | Compare Equal '==' |
| 3'b001 | Less than | Compare Less Than '<'. See Table 1-143. |
| 3'b010 | Less than or equal | Compare Less Than or Equal '<='. |
| 3'b011 | Greater | Compare Greater Than '>'. See Table 1-143. |
| 3'b100 | Greater than or equal | Compare Greater Than or Equal '>='. |

Table 1-144. Bit field encoding: tmr_cfg_enum

| Value | Name | Description |
|-------|------------|---|
| 2'b00 | Continuous | Timer runs while EN bit of CFG0 register is set to '1'. |
| 2'b01 | Pulsewidth | Timer runs from positive to negative edge of TIMEREN. |
| 2'b10 | Period | Timer runs from positive to positive edge of TIMEREN. |
| 2'b11 | Irq | Timer runs until IRQ. |

1.3.219 TMR[0..3]_SR0

Status Register SR0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_SR0: 0x40004F03

TMR1_SR0: 0x40004F0F

TMR2_SR0: 0x40004F1B

TMR3_SR0: 0x40004F27

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|------|-------|-------|--------------|-------|--------|
| SW Access:Reset | RC:0 | RC:0 | RC:0 | RC:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R/W | R/W | R/W | R/W | R | R | R | R |
| Name | TC | CAP_CMP | TEN | TSTOP | MTC | MCAP_CM P | MTEN | MTSTOP |

This register is used to configure interrupt masking and obtain status. Status bits 7-4 are cleared on read.

| Bits | Name | Description |
|------|----------|---|
| 7 | TC | Terminal count status. Interrupt, Sticky (individual bits) |
| 6 | CAP_CMP | Capture/Compare status (MODE = 0--Capture; MODE = 1--Compare). Interrupt, Sticky (individual bits) |
| 5 | TEN | Timer enable status. Interrupt, Sticky (individual bits) |
| 4 | TSTOP | Timer stop status. Interrupt, Sticky (individual bits) |
| 3 | MTC | Terminal count interrupt mask. (0 = Masked; 1 = Unmasked) |
| 2 | MCAP_CMP | Capture/Compare interrupt mask (MODE = 0--Capture; MODE = 1--Compare). (0 = Masked; 1 = Unmasked) |
| 1 | MTEN | Timer enable interrupt mask. (0 = Masked; 1 = Unmasked) |
| 0 | MTSTOP | Timer stop interrupt mask. (0 = Masked; 1 = Unmasked) |

1.3.220 TMR[0..3]_PER0

Timer Period Register PER0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_PER0: 0x40004F04

TMR1_PER0: 0x40004F10

TMR2_PER0: 0x40004F1C

TMR3_PER0: 0x40004F28

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | TIMER_PERIOD0 | | | | | | | |

This register contains the count value the timer is loaded with. When enabled the counter down counts from the value of this register to zero. NOTE: A period of 0 is not supported.

| Bits | Name | Description |
|------|--------------------|---|
| 7:0 | TIMER_PERIOD0[7:0] | Determines the high byte of the period for the timer. |

1.3.221 TMR[0..3]_PER1

Timer Period Register PER1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_PER1: 0x40004F05

TMR1_PER1: 0x40004F11

TMR2_PER1: 0x40004F1D

TMR3_PER1: 0x40004F29

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | TIMER_PERIOD1 | | | | | | | |

This register contains the count value the timer is loaded with. When enabled the counter down counts from the value of this register to zero. NOTE: A period of 0 is not supported.

| Bits | Name | Description |
|------|--------------------|--|
| 7:0 | TIMER_PERIOD1[7:0] | Determines the low byte of the period for the timer. |

1.3.222 TMR[0..3]_CNT_CMP0

Count/Comparator value CNT/CMP0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CNT_CMP0: 0x40004F06

TMR1_CNT_CMP0: 0x40004F12

TMR2_CNT_CMP0: 0x40004F1E

TMR3_CNT_CMP0: 0x40004F2A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COUNT_COMPARE0 | | | | | | | |

This register is a shared register. Its meaning depends upon the value of the MODE bit in the CFG0 register. (MODE = 0--Count value; MODE = 1--Comparator value).

| Bits | Name | Description |
|------|---------------------|--|
| 7:0 | COUNT_COMPARE0[7:0] | MODE = 0--LSB of current count value; MODE = 1--LSB of comparator threshold. |

1.3.223 TMR[0..3]_CNT_CMP1

Count/Comparator value CNT/CMP1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CNT_CMP1: 0x40004F07

TMR1_CNT_CMP1: 0x40004F13

TMR2_CNT_CMP1: 0x40004F1F

TMR3_CNT_CMP1: 0x40004F2B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COUNT_COMPARE1 | | | | | | | |

This register is a shared register. Its meaning depends upon the value of the MODE bit in the CFG0 register. (MODE = 0--Count value; MODE = 1--Comparator value).

| Bits | Name | Description |
|------|---------------------|--|
| 7:0 | COUNT_COMPARE1[7:0] | MODE = 0--MSB of current count value; MODE = 1--MSB of comparator threshold. |

1.3.224 TMR[0..3]_CAP0

Capture Value CAP0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CAP0: 0x40004F08

TMR1_CAP0: 0x40004F14

TMR2_CAP0: 0x40004F20

TMR3_CAP0: 0x40004F2C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CAPTURE_VALUE0 | | | | | | | |

This register holds the captured LSB of the timer count value. A 16-bit read of the CNT register returns the current timer value and captures. An 8-bit LSB read of the CNT register returns the LSB and captures both the LSB and MSB. This register only has meaning when MODE = 0 and is not to be used for any purpose when MODE = 1.

| Bits | Name | Description |
|------|---------------------|--|
| 7:0 | CAPTURE_VALUE0[7:0] | Captured LSB of the timer count value. |

1.3.225 TMR[0..3]_CAP1

Capture Value CAP1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CAP1: 0x40004F09

TMR1_CAP1: 0x40004F15

TMR2_CAP1: 0x40004F21

TMR3_CAP1: 0x40004F2D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CAPTURE_VALUE1 | | | | | | | |

This register holds the captured MSB of the timer count value. A 16-bit read of the CNT register returns the current timer value and captures. An 8-bit LSB read of the CNT register returns the LSB and captures both the LSB and MSB. This register only has meaning when MODE = 0 and is not to be used for any purpose when MODE = 1.

| Bits | Name | Description |
|------|---------------------|--|
| 7:0 | CAPTURE_VALUE1[7:0] | Captured MSB of the timer count value. |

1.3.226 TMR[0..3]_RT0

Configuration Register RT0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_RT0: 0x40004F0A

TMR1_RT0: 0x40004F16

TMR2_RT0: 0x40004F22

TMR3_RT0: 0x40004F2E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------------|---|------------------|---|-----------------|---|--------------|---|
| SW Access:Reset | R/W:00 | | R/W:00 | | R/W:00 | | R/W:00 | |
| HW Access | R | | R | | R | | R | |
| Name | TIMER_RST_SRC_SEL | | TIMER_EN_SRC_SEL | | CAPTURE_SRC_SEL | | KILL_SRC_SEL | |

This register is used to configure the dsi input routing to the timer block.

| Bits | Name | Description |
|------|------------------------|--|
| 7:6 | TIMER_RST_SRC_SEL[1:0] | Selects the driver for the timer reset signal See Table 1-145. |
| 5:4 | TIMER_EN_SRC_SEL[1:0] | Selects the driver for the timer enable signal See Table 1-145. |
| 3:2 | CAPTURE_SRC_SEL[1:0] | Selects the driver for the capture signal See Table 1-145. |
| 1:0 | KILL_SRC_SEL[1:0] | Selects the driver for the kill signal See Table 1-145. |

Table 1-145. Bit field encoding: src_enum

| Value | Name | Description |
|-------|---------|-----------------------------|
| 2'b00 | dsi_in0 | dsi_in0 selected as source. |
| 2'b01 | dsi_in1 | dsi_in1 selected as source. |
| 2'b10 | dsi_in2 | dsi_in2 selected as source. |
| 2'b11 | dsi_in3 | dsi_in3 selected as source. |

1.3.227 TMR[0..3]_RT1

Configuration Register RT1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_RT1: 0x40004F0B

TMR1_RT1: 0x40004F17

TMR2_RT1: 0x40004F23

TMR3_RT1: 0x40004F2F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|---------|----------|----------|----------|----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R | R | R | R | R | R |
| Name | | | SYNCTC | SYNCCMP | SYNCDSI3 | SYNCDSI2 | SYNCDSI1 | SYNCDSI0 |

This register is used to configure the dsi input routing to the timer block. Input signals, dsi_in0, dsi_in1, dsi_in2 and dsi_in3, are double synchronized to the system/bus clock. Output signals, tc and cmp, are registered on the application clock.

| Bits | Name | Description |
|------|----------|--|
| 5 | SYNCTC | Register TC/TC-IRQ with selected clk_bus_en (0 = not registered; 1 = registered) |
| 4 | SYNCCMP | Register CMP/CMPB output with selected clk_bus_en (0 = not registered; 1 = registered) |
| 3 | SYNCDSI3 | Synchronize DSI input, dsi_in3, to clk_bus (0 = no synchronization; 1 = synchronization) |
| 2 | SYNCDSI2 | Synchronize DSI input, dsi_in2, to clk_bus (0 = no synchronization; 1 = synchronization) |
| 1 | SYNCDSI1 | Synchronize DSI input, dsi_in1, to clk_bus (0 = no synchronization; 1 = synchronization) |
| 0 | SYNCDSI0 | Synchronize DSI input, dsi_in0, to clk_bus (0 = no synchronization; 1 = synchronization) |

1.3.228 PRT[0..14]_PC[0..7]

Port Pin Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|-----------------------|-----------------------|
| PRT0_PC0: 0x40005000 | PRT0_PC1: 0x40005001 |
| PRT0_PC2: 0x40005002 | PRT0_PC3: 0x40005003 |
| PRT0_PC4: 0x40005004 | PRT0_PC5: 0x40005005 |
| PRT0_PC6: 0x40005006 | PRT0_PC7: 0x40005007 |
| PRT1_PC0: 0x40005008 | PRT1_PC1: 0x40005009 |
| PRT1_PC2: 0x4000500A | PRT1_PC3: 0x4000500B |
| PRT1_PC4: 0x4000500C | PRT1_PC5: 0x4000500D |
| PRT1_PC6: 0x4000500E | PRT1_PC7: 0x4000500F |
| PRT2_PC0: 0x40005010 | PRT2_PC1: 0x40005011 |
| PRT2_PC2: 0x40005012 | PRT2_PC3: 0x40005013 |
| PRT2_PC4: 0x40005014 | PRT2_PC5: 0x40005015 |
| PRT2_PC6: 0x40005016 | PRT2_PC7: 0x40005017 |
| PRT3_PC0: 0x40005018 | PRT3_PC1: 0x40005019 |
| PRT3_PC2: 0x4000501A | PRT3_PC3: 0x4000501B |
| PRT3_PC4: 0x4000501C | PRT3_PC5: 0x4000501D |
| PRT3_PC6: 0x4000501E | PRT3_PC7: 0x4000501F |
| PRT4_PC0: 0x40005020 | PRT4_PC1: 0x40005021 |
| PRT4_PC2: 0x40005022 | PRT4_PC3: 0x40005023 |
| PRT4_PC4: 0x40005024 | PRT4_PC5: 0x40005025 |
| PRT4_PC6: 0x40005026 | PRT4_PC7: 0x40005027 |
| PRT5_PC0: 0x40005028 | PRT5_PC1: 0x40005029 |
| PRT5_PC2: 0x4000502A | PRT5_PC3: 0x4000502B |
| PRT5_PC4: 0x4000502C | PRT5_PC5: 0x4000502D |
| PRT5_PC6: 0x4000502E | PRT5_PC7: 0x4000502F |
| PRT6_PC0: 0x40005030 | PRT6_PC1: 0x40005031 |
| PRT6_PC2: 0x40005032 | PRT6_PC3: 0x40005033 |
| PRT6_PC4: 0x40005034 | PRT6_PC5: 0x40005035 |
| PRT6_PC6: 0x40005036 | PRT6_PC7: 0x40005037 |
| PRT12_PC0: 0x40005060 | PRT12_PC1: 0x40005061 |
| PRT12_PC2: 0x40005062 | PRT12_PC3: 0x40005063 |
| PRT12_PC4: 0x40005064 | PRT12_PC5: 0x40005065 |
| PRT12_PC6: 0x40005066 | PRT12_PC7: 0x40005067 |

1.3.228 PRT[0..14]_PC[0..7] (continued)

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|-------|---------|-----------|-------------|-------------|-------------|----------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | bypass | slew | bidirEn | pin_state | driveMode_2 | driveMode_1 | driveMode_0 | data_out |

The Port Pin Configuration Registers (PRTxPC0 through PRTxPC7) access several configuration or status bits of a single I/O port pin at once. Please reference the register description of the aliased register for detailed information the port configuration controlled by a given bit.

| Bits | Name | Description |
|------|-------------|--|
| 7 | bypass | The Bypass bit is the same as the corresponding bit in the port bypass register. See Table 1-147. |
| 6 | slew | The slew bit is the same as the corresponding bit in the port slew register. |
| 5 | bidirEn | The BiDir En bit is the same as the corresponding bit in the port bidirection enable register. See Table 1-146. |
| 4 | pin_state | The Pin State bit (read only) is the same as the corresponding bit in the port pin state register. |
| 3 | driveMode_2 | The DM2 bit is the same as the corresponding bit in the drive mode 2 register. Please refer to the IO chapter section on IO drive modes for detailed information on the 8 different drive mode configurations. |
| 2 | driveMode_1 | The DM1 bit is the same as the corresponding bit in the drive mode 1 register. Please refer to the IO chapter section on IO drive modes for detailed information on the 8 different drive mode configurations. |
| 1 | driveMode_0 | The DM0 bit is the same as the corresponding bit in the drive mode 0 register. Please refer to the IO chapter section on IO drive modes for detailed information on the 8 different drive mode configurations. |
| 0 | data_out | The data out bit is the same as the corresponding bit in the data register. |

Table 1-146. Bit field encoding: bidir_en_enum

| Value | Name | Description |
|-------|-----------|--------------------------------------|
| 1'b0 | BIDIR_DIS | dynamic bidirectional mode disabled. |
| 1'b1 | BIDIR_EN | dynamic bidirectional mode enabled. |

Table 1-147. Bit field encoding: bypass_en_enum

| Value | Name | Description |
|-------|------------|---------------------------|
| 1'b0 | BYPASS_DIS | bypass function disabled. |
| 1'b1 | BYPASS_EN | bypass function enabled. |

1.3.229 IO_PC_PRT15_PC[0..5]

Port Pin Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IO_PC_PRT15_PC0: 0x40005078

IO_PC_PRT15_PC1: 0x40005079

IO_PC_PRT15_PC2: 0x4000507A

IO_PC_PRT15_PC3: 0x4000507B

IO_PC_PRT15_PC4: 0x4000507C

IO_PC_PRT15_PC5: 0x4000507D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|-------|---------|-----------|-----------------|-----------------|-----------------|----------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R:0 | R/W:0 | R/W:0 | R/W:0 | R/W:1 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | bypass | slew | bidirEn | pin_state | driveMode_ 2 | driveMode_ 1 | driveMode_ 0 | data_out |

The Port Pin Configuration Registers (PRTxPC0 through PRTxPC7) access several configuration or status bits of a single I/O port pin at once. Please reference the register description of the aliased register for detailed information the port configuration controlled by a given bit.

| Bits | Name | Description |
|------|-------------|--|
| 7 | bypass | The Bypass bit is the same as the corresponding bit in the port bypass register. See Table 1-149. |
| 6 | slew | The slew bit is the same as the corresponding bit in the port slew register. |
| 5 | bidirEn | The BiDir En bit is the same as the corresponding bit in the port bidirection enable register. See Table 1-148. |
| 4 | pin_state | The Pin State bit (read only) is the same as the corresponding bit in the port pin state register. |
| 3 | driveMode_2 | The DM2 bit is the same as the corresponding bit in the drive mode 2 register. Please refer to the IO chapter section on IO drive modes for detailed information on the 8 different drive mode configurations. |
| 2 | driveMode_1 | The DM1 bit is the same as the corresponding bit in the drive mode 1 register. Please refer to the IO chapter section on IO drive modes for detailed information on the 8 different drive mode configurations. |
| 1 | driveMode_0 | The DM0 bit is the same as the corresponding bit in the drive mode 0 register. Please refer to the IO chapter section on IO drive modes for detailed information on the 8 different drive mode configurations. |
| 0 | data_out | The data out bit is the same as the corresponding bit in the data register. |

Table 1-148. Bit field encoding: bidir_en_enum

| Value | Name | Description |
|-------|-----------|--------------------------------------|
| 1'b0 | BIDIR_DIS | dynamic bidirectional mode disabled. |
| 1'b1 | BIDIR_EN | dynamic bidirectional mode enabled. |

Table 1-149. Bit field encoding: bypass_en_enum

| Value | Name | Description |
|-------|------------|---------------------------|
| 1'b0 | BYPASS_DIS | bypass function disabled. |
| 1'b1 | BYPASS_EN | bypass function enabled. |

1.3.230 IO_PC_PRT15_7_6_PC[0..1]

Port Pin Configuration Register

Reset: Reset Signals Listed Below

Register : Address

IO_PC_PRT15_7_6_PC0: 0x4000507E

IO_PC_PRT15_7_6_PC1: 0x4000507F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|-------|---|-----------|------|-----------|-------------|----------|
| SW Access:Reset | R/W:0 | NA:00 | | R:U | NA:0 | R/W:0 | R/W:0 | R/W:1 |
| HW Access | R/W | NA | | R/W | NA | R/W | R/W | R/W |
| Name | bypass | | | pin_state | | pullUp_en | driveMode_0 | data_out |

The Port Pin Configuration Registers (PRTxPC0 through PRTxPC7) access several configuration or status bits of a single I/O port pin at once. Please reference the register description of the aliased register for detailed information the port configuration controlled by a given bit.

| Bits | Name | Description |
|------|-------------|--|
| 7 | bypass | The Bypass bit is the same as the corresponding bit in the port bypass register. See Table 1-150. |
| 4 | pin_state | The Pin State bit (read only) is the same as the corresponding bit in the port pin state register. |
| 2 | pullUp_en | The pull-up en bit is the same as the corresponding bit in the drive mode 1 register. |
| 1 | driveMode_0 | The DM0 bit is the same as the corresponding bit in the drive mode 0 register. |
| 0 | data_out | The data out bit is the same as the corresponding bit in the data register. |

Reset Table

| resetsignal | field(s) |
|--|--|
| N/A | pin_state |
| System reset for retention flops [reset_all_retention] | data_out, driveMode_0, pullUp_en, bypass |

Table 1-150. Bit field encoding: bypass_en_enum

| Value | Name | Description |
|-------|------------|---------------------------|
| 1'b0 | BYPASS_DIS | bypass function disabled. |
| 1'b1 | BYPASS_EN | bypass function enabled. |

1.3.231 PRT[0..14]_DR_ALIAS

Aliased Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DR_ALIAS: 0x40005080

PRT1_DR_ALIAS: 0x40005081

PRT2_DR_ALIAS: 0x40005082

PRT3_DR_ALIAS: 0x40005083

PRT4_DR_ALIAS: 0x40005084

PRT5_DR_ALIAS: 0x40005085

PRT6_DR_ALIAS: 0x40005086

PRT12_DR_ALIAS: 0x4000508C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DataReg_alias | | | | | | | |

This register is used to set the output data output state for the corresponding GPIO port.

| Bits | Name | Description |
|------|--------------------|---|
| 7:0 | DataReg_alias[7:0] | The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. This register is only accessible if the PRTxBIT_MASK register bits are set. |

1.3.232 PRT15_DR_15_ALIAS

Aliased Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DR_15_ALIAS: 0x4000508F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------------|----------------------|---------------|---|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:000000 | | | | | |
| HW Access | R/W | R/W | R/W | | | | | |
| Name | DataReg_D M_alias | DataReg_D P_alias | DataReg_alias | | | | | |

This register is used to set the output data output state for the corresponding GPIO port.

| Bits | Name | Description |
|------|--------------------|---|
| 7 | DataReg_DM_alias | The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. This register is only accessible if the PRTxBIT_MASK register bits are set. |
| 6 | DataReg_DP_alias | The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. This register is only accessible if the PRTxBIT_MASK register bits are set. |
| 5:0 | DataReg_alias[5:0] | The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. This register is only accessible if the PRTxBIT_MASK register bits are set. |

1.3.233 PRT[0..14]_PS_ALIAS

Aliased Port Pin State Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|----------------------------|
| PRT0_PS_ALIAS: 0x40005090 | PRT1_PS_ALIAS: 0x40005091 |
| PRT2_PS_ALIAS: 0x40005092 | PRT3_PS_ALIAS: 0x40005093 |
| PRT4_PS_ALIAS: 0x40005094 | PRT5_PS_ALIAS: 0x40005095 |
| PRT6_PS_ALIAS: 0x40005096 | PRT12_PS_ALIAS: 0x4000509C |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | PinState_alias | | | | | | | |

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

| Bits | Name | Description |
|------|---------------------|---|
| 7:0 | PinState_alias[7:0] | <p>Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin:</p> <ul style="list-style-type: none"> 1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0 Reads LOW if the pin voltage is below that threshold, logic low. <p>If the drive mode for the pin is set to High-Z Analog, the pin state will read 0 independent of the voltage on the pin.</p> |

This register is only accessible if the PRTxBIT_MASK register bits are set.

1.3.234 PRT15_PS15_ALIAS

Aliased Port Pin State Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_PS15_ALIAS: 0x4000509F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------------------|-----------------------|----------------|---|---|---|---|---|
| SW Access:Reset | R:0 | R:0 | R:000000 | | | | | |
| HW Access | R/W | R/W | R/W | | | | | |
| Name | PinState_D M_alias | PinState_D P_alias | PinState_alias | | | | | |

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

| Bits | Name | Description |
|------|-------------------|---|
| 7 | PinState_DM_alias | <p>Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin:</p> <p>1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0 Reads LOW if the pin voltage is below that threshold, logic low.</p> <p>If the drive mode for the pin is set to High-Z, the pin state read will return an unknown state.</p> |
| 6 | PinState_DP_alias | <p>This register is only accessible if the PRTxBIT_MASK register bits are set.</p> <p>Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin:</p> <p>1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0 Reads LOW if the pin voltage is below that threshold, logic low.</p> <p>If the drive mode for the pin is set to High-Z, the pin state read will return an unknown state.</p> |

This register is only accessible if the PRTxBIT_MASK register bits are set.

1.3.234 PRT15_PS15_ALIAS (continued)

| | | |
|-----|---------------------|--|
| 5:0 | PinState_alias[5:0] | <p>Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin:</p> <ul style="list-style-type: none">1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high.0 Reads LOW if the pin voltage is below that threshold, logic low. <p>If the drive mode for the pin is set to High-Z Analog, the pin state will read 0 independent of the voltage on the pin.</p> |
|-----|---------------------|--|

This register is only accessible if the PRTxBIT_MASK register bits are set.

1.3.235 PRT[0..11]_DR

Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DR: 0x40005100

PRT1_DR: 0x40005110

PRT2_DR: 0x40005120

PRT3_DR: 0x40005130

PRT4_DR: 0x40005140

PRT5_DR: 0x40005150

PRT6_DR: 0x40005160

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DataReg | | | | | | | |

This register is used to set the output data state for the corresponding GPIO port.

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | DataReg[7:0] | The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. |

1.3.236 PRT[0..11]_PS

Port Pin State Register1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_PS: 0x40005101

PRT1_PS: 0x40005111

PRT2_PS: 0x40005121

PRT3_PS: 0x40005131

PRT4_PS: 0x40005141

PRT5_PS: 0x40005151

PRT6_PS: 0x40005161

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PinState | | | | | | | |

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | PinState[7:0] | <p>Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin:</p> <ul style="list-style-type: none"> 1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 1'b0 Reads LOW if the pin voltage is below that threshold, logic low. <p>If the drive mode for the pin is set to High-Z Analog, the pin state will read 0 independent of the voltage on the pin.</p> |

1.3.237 PRT[0..11]_DM[0..2]

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------|----------------------|
| PRT0_DM0: 0x40005102 | PRT0_DM1: 0x40005103 |
| PRT0_DM2: 0x40005104 | PRT1_DM0: 0x40005112 |
| PRT1_DM1: 0x40005113 | PRT1_DM2: 0x40005114 |
| PRT2_DM0: 0x40005122 | PRT2_DM1: 0x40005123 |
| PRT2_DM2: 0x40005124 | PRT3_DM0: 0x40005132 |
| PRT3_DM1: 0x40005133 | PRT3_DM2: 0x40005134 |
| PRT4_DM0: 0x40005142 | PRT4_DM1: 0x40005143 |
| PRT4_DM2: 0x40005144 | PRT5_DM0: 0x40005152 |
| PRT5_DM1: 0x40005153 | PRT5_DM2: 0x40005154 |
| PRT6_DM0: 0x40005162 | PRT6_DM1: 0x40005163 |
| PRT6_DM2: 0x40005164 | |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DriveMode | | | | | | | |

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO chapter section on IO drive modes for detailed information on the eight different drive mode configurations.

| Bits | Name | Description |
|------|------|-------------|
|------|------|-------------|

1.3.237 PRT[0..11]_DM[0..2] (continued)

| | | |
|-----|----------------|---|
| 7:0 | DriveMode[7:0] | 1'b0 Corresponding drive mode register bit asserted low. 1'b1 Corresponding drive mode register asserted high. |
|-----|----------------|---|

The combination of the 3 drive mode registers per port determines the drive mode setting for each GPIO pin.

Drive mode is configured on a pad by pad basis using the bit specific drive mode of each pin. Please refer to the IO chapter section on drive modes for detailed information on the eight different drive mode configurations.

$$DM [2:0] = \{PRT X .DM2 [y], PRT X .DM1 [y], PRT X .DM0 [y]\}$$

DM [2:0] : Complete drive mode setting for pin [y] 3'b000 : Mode 0, input/output buffers disabled. 3'b001 : Mode 1, input only 3'b010 : Mode 2, weak pull-up, strong pull-down 3'b011 : Mode 3, strong pull-up, weak pull-down 3'b100 : Mode 4, open drain, strong pull-down 3'b101 : Mode 5, open drain, strong pull-up 3'b110 : Mode 6, strong pull-up, strong pull-down 3'b111 : Mode 7, weak pull-up, weak pull-down

Please reference the IO section in the IROS book 1.

1.3.238 PRT[0..11]_SLW

Port slew rate control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_SLW: 0x40005105

PRT1_SLW: 0x40005115

PRT2_SLW: 0x40005125

PRT3_SLW: 0x40005135

PRT4_SLW: 0x40005145

PRT5_SLW: 0x40005155

PRT6_SLW: 0x40005165

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | SlwCtl | | | | | | | |

The output drive on any I/O pin can be set to a fast edge rate mode (Slew=0) or slow edge rate mode (Slew=1) The slew rate only applies to strong output drive modes, not to resistive drive modes. Slower edge rates normally reduce EMI issues and are recommended when speed is not critical.

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | SlwCtl[7:0] | Each bit controls the output edge rate of the corresponding port pin. 1'b0 Fast edge rate mode 1'b1 Slow edge rate mode |

1.3.239 PRT[0..11]_BYP

Port Bypass enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_BYP: 0x40005106

PRT1_BYP: 0x40005116

PRT2_BYP: 0x40005126

PRT3_BYP: 0x40005136

PRT4_BYP: 0x40005146

PRT5_BYP: 0x40005156

PRT6_BYP: 0x40005166

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | Bypass | | | | | | | |

The Port Bypass Registers select output data from either the data output register or internal sources such as digital global bus.

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | Bypass[7:0] | 1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 Port logic data register drives the corresponding port pin. <i>The drive mode settings must configure the port to enable the output buffer or the DSI dynamic drive control must configure the output enable for the pad.</i> |

1.3.240 PRT[0..11]_BIE

Port Bidirection enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_BIE: 0x40005107

PRT1_BIE: 0x40005117

PRT2_BIE: 0x40005127

PRT3_BIE: 0x40005137

PRT4_BIE: 0x40005147

PRT5_BIE: 0x40005157

PRT6_BIE: 0x40005167

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | BidirectEn | | | | | | | |

The Port Bidirectional Enable Registers are used to enable dynamic bidirectional mode at any pin.

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | BidirectEn[7:0] | Each bit controls the bidirectional mode of the corresponding port pin. 1'b0 Normal operation of pad. Drive mode setting configures output buffer 1'b1 Selected dynamic control DSI configures output buffer |

1.3.241 PRT[0..11]_INP_DIS

Input buffer disable override

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|--------------------------|--------------------------|
| PRT0_INP_DIS: 0x40005108 | PRT1_INP_DIS: 0x40005118 |
| PRT2_INP_DIS: 0x40005128 | PRT3_INP_DIS: 0x40005138 |
| PRT4_INP_DIS: 0x40005148 | PRT5_INP_DIS: 0x40005158 |
| PRT6_INP_DIS: 0x40005168 | |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | Inp_dis | | | | | | | |

The bits asserted force the input buffers off.

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | Inp_dis[7:0] | 1'b1 Input buffers are disabled, overrides drive mode register settings. 1'b0 Input buffers are configured based on drive mode register settings. |

1.3.242 PRT[0..11]_CTL

Port wide control signals

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------|----------------------|
| PRT0_CTL: 0x40005109 | PRT1_CTL: 0x40005119 |
| PRT2_CTL: 0x40005129 | PRT3_CTL: 0x40005139 |
| PRT4_CTL: 0x40005149 | PRT5_CTL: 0x40005159 |
| PRT6_CTL: 0x40005169 | |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-------------|---|---|-----------|
| SW Access:Reset | NA:0000 | | | | R/W:000 | | | R/W:0 |
| HW Access | NA | | | | R | | | R |
| Name | | | | | portEmifCfg | | | vtrip_sel |

The port wide vtrip select register is used to select the input buffer trip point select. The emif configuration bits are used to configure the port for external memory access.

| Bits | Name | Description |
|------|------------------|---|
| 3:1 | portEmifCfg[2:0] | GPIO emif selection option configures the port for External memory interface. See Table 1-151. |
| 0 | vtrip_sel | The GPIO cells include a vtrip_sel signal to alter the input buffer voltage. See Table 1-152. |

Table 1-151. Bit field encoding: emif_cfg_enum

| Value | Name | Description |
|--------|----------|---|
| 3'b000 | NOT_EMIF | Port not selected for EMIF control |
| 3'b001 | LSB_ADDR | Port selected as Address LS byte range |
| 3'b010 | UPR_ADDR | Port selected as Address upper byte range |
| 3'b011 | MSB_ADDR | Port selected as Address MS byte range |
| 3'b101 | LSB_DATA | Port selected as Data lower byte range |
| 3'b110 | MSB_DATA | Port selected as Data upper byte range |

Table 1-152. Bit field encoding: vtrip_sel_enum

| Value | Name | Description |
|-------|-------------|--|
| 1'b0 | VTRIP_CMOS | Input buffer functions as a CMOS input buffer. |
| 1'b1 | VTRIP_LVTTL | Input buffer functions as a LVTTTL input buffer. |

1.3.243 PRT[0..11]_PRT

Port wide configuration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_PRT: 0x4000510A

PRT1_PRT: 0x4000511A

PRT2_PRT: 0x4000512A

PRT3_PRT: 0x4000513A

PRT4_PRT: 0x4000514A

PRT5_PRT: 0x4000515A

PRT6_PRT: 0x4000516A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|------|------------|------|------------|------------|------------|------|
| SW Access:Reset | W:0 | W:0 | W:0 | NA:0 | W:0 | W:0 | W:0 | NA:0 |
| HW Access | R | R | R | NA | R | R | R | NA |
| Name | byPass | slew | bidirectEn | | driveMode2 | driveMode1 | driveMode0 | |

The Port Configuration Register accesses several available configuration registers on a port-wide basis with a single bit write.

| Bits | Name | Description |
|------|------------|--|
| 7 | byPass | The Bypass bit sets all the bits for the port bypass register. See Table 1-154. |
| 6 | slew | The slew bit is the same as the corresponding bit in the port slew register. |
| 5 | bidirectEn | The BiDir En bit sets all bits for the port bidirection enable register. See Table 1-153. |
| 3 | driveMode2 | A write to this bit sets all bits for the corresponding drive mode register of the entire port. |
| 2 | driveMode1 | A write to this bit sets all bits for the corresponding drive mode register of the entire port. |
| 1 | driveMode0 | A write to this bit sets all bits for the corresponding drive mode register of the entire port. |

Table 1-153. Bit field encoding: bidir_en_enum

| Value | Name | Description |
|-------|-----------|--------------------------------------|
| 1'b0 | BIDIR_DIS | dynamic bidirectional mode disabled. |
| 1'b1 | BIDIR_EN | dynamic bidirectional mode enabled. |

Table 1-154. Bit field encoding: bypass_en_enum

| Value | Name | Description |
|-------|------------|---------------------------|
| 1'b0 | BYPASS_DIS | bypass function disabled. |
| 1'b1 | BYPASS_EN | bypass function enabled. |

1.3.244 PRT[0..11]_BIT_MASK

Bit-mask for Aliased Register access

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_BIT_MASK: 0x4000510B

PRT1_BIT_MASK: 0x4000511B

PRT2_BIT_MASK: 0x4000512B

PRT3_BIT_MASK: 0x4000513B

PRT4_BIT_MASK: 0x4000514B

PRT5_BIT_MASK: 0x4000515B

PRT6_BIT_MASK: 0x4000516B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | bit_mask | | | | | | | |

The bits asserted in the bit-mask register allow direct access to the data register or pin state register via the aliased registers.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | bit_mask[7:0] | 1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space. |

1.3.245 PRT[0..11]_AMUX

Port Analog global mux bus enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_AMUX: 0x4000510C

PRT1_AMUX: 0x4000511C

PRT2_AMUX: 0x4000512C

PRT3_AMUX: 0x4000513C

PRT4_AMUX: 0x4000514C

PRT5_AMUX: 0x4000515C

PRT6_AMUX: 0x4000516C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | Amux | | | | | | | |

Analog global mux switch.

| Bits | Name | Description |
|------|-----------|---|
| 7:0 | Amux[7:0] | Connects analog mux bus to the pad when asserted. |

1.3.246 PRT[0..11]_AG

Port Analog global enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_AG: 0x4000510D

PRT1_AG: 0x4000511D

PRT2_AG: 0x4000512D

PRT3_AG: 0x4000513D

PRT4_AG: 0x4000514D

PRT5_AG: 0x4000515D

PRT6_AG: 0x4000516D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | AnalogGlobal | | | | | | | |

Analog global switch.

| Bits | Name | Description |
|------|-------------------|--|
| 7:0 | AnalogGlobal[7:0] | Connects analog global to the pad when asserted. |

1.3.247 PRT[0..11]_LCD_COM_SEG

Port LCD Com seg bits.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_LCD_COM_SEG: 0x4000510E

PRT1_LCD_COM_SEG: 0x4000511E

PRT2_LCD_COM_SEG: 0x4000512E

PRT3_LCD_COM_SEG: 0x4000513E

PRT4_LCD_COM_SEG: 0x4000514E

PRT5_LCD_COM_SEG: 0x4000515E

PRT6_LCD_COM_SEG: 0x4000516E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | com_seg | | | | | | | |

Selects whether a pin is set as a common or segment drive pin.

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | com_seg[7:0] | Specify whether the pin will drive common or segment mode when LCD is enabled. 1'b0 Segment 1'b1 Common |

1.3.248 PRT[0..11]_LCD_EN

Port LCD enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_LCD_EN: 0x4000510F

PRT1_LCD_EN: 0x4000511F

PRT2_LCD_EN: 0x4000512F

PRT3_LCD_EN: 0x4000513F

PRT4_LCD_EN: 0x4000514F

PRT5_LCD_EN: 0x4000515F

PRT6_LCD_EN: 0x4000516F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | Lcd_en | | | | | | | |

Enables a given pin for LCD drive mode. Make sure PRT1_PIN2 LCD_EN is not set when P1_2 is used as configurable XRES, otherwise behavior of device is not guaranteed

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | Lcd_en[7:0] | Enable the pin for LCD mode. 1'b0 Disabled 1'b1 Enabled |

1.3.249 PRT12_DR

Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_DR: 0x400051C0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DataReg | | | | | | | |

This register is used to set the output data state for the corresponding GPIO port.

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | DataReg[7:0] | The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. |

1.3.250 PRT12_PS

Port Pin State Register1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_PS: 0x400051C1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PinState | | | | | | | |

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | PinState[7:0] | <p>Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin:</p> <p>1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high.</p> <p>1'b0 Reads LOW if the pin voltage is below that threshold, logic low.</p> <p>If the drive mode for the pin is set to High-Z Analog, the pin state will read 0 independent of the voltage on the pin.</p> |

1.3.251 PRT12_DM[0..2]

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_DM0: 0x400051C2

PRT12_DM1: 0x400051C3

PRT12_DM2: 0x400051C4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DriveMode | | | | | | | |

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO chapter section on IO drive modes for detailed information on the eight different drive mode configurations.

| Bits | Name | Description |
|------|------|-------------|
|------|------|-------------|

1.3.251 PRT12_DM[0..2] (continued)

| | | |
|-----|----------------|---|
| 7:0 | DriveMode[7:0] | 1'b0 Corresponding drive mode register bit asserted low. 1'b1 Corresponding drive mode register asserted high. |
|-----|----------------|---|

The combination of the 3 drive mode registers per port determines the drive mode setting for each GPIO pin.

Drive mode is configured on a pad by pad basis using the bit specific drive mode of each pin. Please refer to the IO chapter section on drive modes for detailed information on the eight different drive mode configurations.

$$DM [2:0] = \{PRT X .DM2 [y] , PRT X .DM1 [y] , PRT X .DM0 [y] \}$$

DM [2:0] : Complete drive mode setting for pin [y] 3'b000 : Mode 0, input/output buffers disabled. 3'b001 : Mode 1, input only 3'b010 : Mode 2, weak pull-up, strong pull-down 3'b011 : Mode 3, strong pull-up, weak pull-down 3'b100 : Mode 4, open drain, strong pull-down 3'b101 : Mode 5, open drain, strong pull-up 3'b110 : Mode 6, strong pull-up, strong pull-down 3'b111 : Mode 7, weak pull-up, weak pull-down

Please reference the IO section in the IROS book 1.

1.3.252 PRT12_SLW

Port slew rate control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SLW: 0x400051C5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | SlwCtl | | | | | | | |

The output drive on any I/O pin can be set to a fast edge rate mode (Slew=0) or slow edge rate mode (Slew=1) The slew rate only applies to strong output drive modes, not to resistive drive modes. Slower edge rates normally reduce EMI issues and are recommended when speed is not critical.

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | SlwCtl[7:0] | Each bit controls the output edge rate of the corresponding port pin. 1'b0 Fast edge rate mode 1'b1 Slow edge rate mode |

1.3.253 PRT12_BYP

Port Bypass enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_BYP: 0x400051C6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | Bypass | | | | | | | |

The Port Bypass Registers select output data from either the data output register or internal sources such as digital global bus.

| Bits | Name | Description |
|------|-------------|--|
| 7:0 | Bypass[7:0] | <p>1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin.</p> <p>1'b0 Port logic data register drives the corresponding port pin.</p> <p><i>The drive mode settings must configure the port to enable the output buffer or the DSI dynamic drive control must configure the output enable for the pad.</i></p> |

1.3.254 PRT12_BIE

Port Bidirection enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_BIE: 0x400051C7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | BidirectEn | | | | | | | |

The Port Bidirectional Enable Registers are used to enable dynamic bidirectional mode at any pin.

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | BidirectEn[7:0] | Each bit controls the bidirectional mode of the corresponding port pin. 1'b0 Normal operation of pad. Drive mode setting configures output buffer 1'b1 Selected dynamic control DSI configures output buffer |

1.3.255 PRT12_INP_DIS

Input buffer disable override

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_INP_DIS: 0x400051C8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | Inp_dis | | | | | | | |

The bits asserted force the input buffers off.

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | Inp_dis[7:0] | 1'b1 Input buffers are disabled, overrides drive mode register settings. 1'b0 Input buffers are configured based on drive mode register settings. |

1.3.256 PRT12_SIO_HYST_EN

SIO Hysteresis enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_HYST_EN: 0x400051C9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | sio_diff_hyst_en | | | | | | | |

The SIO hysteresis enable for the SIO differential input buffer.

| Bits | Name | Description |
|------|-----------------------|------------------|
| 7:0 | sio_diff_hyst_en[7:0] | (no description) |

1.3.257 PRT12_PRT

Port wide configuration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_PRT: 0x400051CA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|------|------------|------|------------|------------|------------|------|
| SW Access:Reset | W:0 | W:0 | W:0 | NA:0 | W:0 | W:0 | W:0 | NA:0 |
| HW Access | R | R | R | NA | R | R | R | NA |
| Name | byPass | slew | bidirectEn | | driveMode2 | driveMode1 | driveMode0 | |

The Port Configuration Register accesses several available configuration registers on a port-wide basis with a single bit write.

| Bits | Name | Description |
|------|------------|--|
| 7 | byPass | The Bypass bit sets all the bits for the port bypass register. See Table 1-156. |
| 6 | slew | The slew bit is the same as the corresponding bit in the port slew register. |
| 5 | bidirectEn | The BiDir En bit sets all bits for the port bidirection enable register. See Table 1-155. |
| 3 | driveMode2 | A write to this bit sets all bits for the corresponding drive mode register of the entire port. |
| 2 | driveMode1 | A write to this bit sets all bits for the corresponding drive mode register of the entire port. |
| 1 | driveMode0 | A write to this bit sets all bits for the corresponding drive mode register of the entire port. |

Table 1-155. Bit field encoding: bidir_en_enum

| Value | Name | Description |
|-------|-----------|--------------------------------------|
| 1'b0 | BIDIR_DIS | dynamic bidirectional mode disabled. |
| 1'b1 | BIDIR_EN | dynamic bidirectional mode enabled. |

Table 1-156. Bit field encoding: bypass_en_enum

| Value | Name | Description |
|-------|------------|---------------------------|
| 1'b0 | BYPASS_DIS | bypass function disabled. |
| 1'b1 | BYPASS_EN | bypass function enabled. |

1.3.258 PRT12_BIT_MASK

Bit-mask for Aliased Register access

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_BIT_MASK: 0x400051CB

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | bit_mask | | | | | | | |

The bits asserted in the bit-mask register allow direct access to the data register or pin state register via the aliased registers.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | bit_mask[7:0] | 1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space. |

0x400051cc

1.3.259 PRT12_SIO_REG_HIFREQ

Regulated pull-up driver DC current setting

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_REG_HIFREQ: 0x400051CC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------------------|------|------------------------|------|------------------------|------|------------------------|------|
| SW Access:Reset | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | R | NA | R | NA | R | NA | R | NA |
| Name | sio_reg_hifr eq_7_6 | | sio_reg_hifr eq_5_4 | | sio_reg_hifr eq_3_2 | | sio_reg_hifr eq_1_0 | |

Sets each SIO pair's pull-up driver DC current. For output frequency $\leq 10\text{MHz}$, setting this low will lower the DC current on the SIO pin pair. For output frequency $> 10\text{MHz} \leq 33\text{MHz}$, set the bit high.

| Bits | Name | Description |
|------|--------------------|---------------------------|
| 7 | sio_reg_hifreq_7_6 | pull-up driver DC current |
| 5 | sio_reg_hifreq_5_4 | pull-up driver DC current |
| 3 | sio_reg_hifreq_3_2 | pull-up driver DC current |
| 1 | sio_reg_hifreq_1_0 | pull-up driver DC current |

1.3.260 PRT12_AG

Port Analog global enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_AG: 0x400051CD

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------------|---|------------------|---|------------------|---|------------------|---|
| SW Access:Reset | R/W:00 | | R/W:00 | | R/W:00 | | R/W:00 | |
| HW Access | R | | R | | R | | R | |
| Name | AnalogGlobal_7_6 | | AnalogGlobal_5_4 | | AnalogGlobal_3_2 | | AnalogGlobal_1_0 | |

Analog global switch.

| Bits | Name | Description |
|------|-----------------------|---|
| 7:6 | AnalogGlobal_7_6[1:0] | Connects analog global when asserted. See Table 1-157. |
| 5:4 | AnalogGlobal_5_4[1:0] | Connects analog global when asserted. See Table 1-157. |
| 3:2 | AnalogGlobal_3_2[1:0] | Connects analog global when asserted. See Table 1-157. |
| 1:0 | AnalogGlobal_1_0[1:0] | Connects analog global when asserted. See Table 1-157. |

Table 1-157. Bit field encoding: pr12_ag_enum

| Value | Name | Description |
|-------|----------|----------------------------------|
| 2'b00 | NO_AG | No AG selected. |
| 2'b01 | AG0_SEL | low bit AG connection selected. |
| 2'b10 | AG1_SEL | high bit AG connection selected. |
| 2'b11 | VCCD_SEL | VCCD connection selected. |

1.3.261 PRT12_SIO_CFG

SIO Input Output Configuration

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_CFG: 0x400051CE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|-------------|--------------|-------------|--------------|-------------|--------------|-------------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | ibuf_sel_7_6 | vreg_en_7_6 | ibuf_sel_5_4 | vreg_en_5_4 | ibuf_sel_3_2 | vreg_en_3_2 | ibuf_sel_1_0 | vreg_en_1_0 |

Sets each SIO pair's input output Configuration. vreg_en=0 & ibuf_sel=0 sets the mode to Single Ended Input Buffer, Non-regulated Output Buffer. vreg_en=0 & ibuf_sel=1 sets the mode to Differential Input Buffer, Non-regulated Output Buffer. vreg_en=1 & ibuf_sel=0 sets the mode to Single Ended Input Buffer, Regulated Output Buffer. vreg_en=1 & ibuf_sel=1 sets the mode to Differential Input Buffer, Regulated Output Buffer.

| Bits | Name | Description |
|------|--------------|--|
| 7 | ibuf_sel_7_6 | sets the ibuf_sel for the corresponding SIO pair |
| 6 | vreg_en_7_6 | sets the vreg_en for the corresponding SIO pair |
| 5 | ibuf_sel_5_4 | sets the ibuf_sel for the corresponding SIO pair |
| 4 | vreg_en_5_4 | sets the vreg_en for the corresponding SIO pair |
| 3 | ibuf_sel_3_2 | sets the ibuf_sel for the corresponding SIO pair |
| 2 | vreg_en_3_2 | sets the vreg_en for the corresponding SIO pair |
| 1 | ibuf_sel_1_0 | sets the ibuf_sel for the corresponding SIO pair |
| 0 | vreg_en_1_0 | sets the vreg_en for the corresponding SIO pair |

1.3.262 PRT12_SIO_DIFF

Differential Input Buffer reference voltage selection

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_DIFF: 0x400051CF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---------------|--------------|---------------|--------------|---------------|--------------|---------------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vref_sel_7_6 | vtrip_sel_7_6 | vref_sel_5_4 | vtrip_sel_5_4 | vref_sel_3_2 | vtrip_sel_3_2 | vref_sel_1_0 | vtrip_sel_1_0 |

Sets each SIO pair's input buffer switching threshold. If `ibuf_sel=0`, `vref_sel` has no impact as the single-ended receiver is used. In this case: `vtrip_sel=0` sets the single-ended input buffer threshold to CMOS levels. `vtrip_sel=1` sets the single-ended input buffer threshold to LVTTTL levels. If `ibuf_sel=1`, the differential receiver is used and `vref_sel` does have functional impact. In this case: `vref_sel=0 & vtrip_sel=0` sets the differential input buffer threshold to $0.5 \cdot v_{io}$. `vref_sel=0 & vtrip_sel=1` sets the differential input buffer threshold to $0.4 \cdot v_{io}$. `vref_sel=1 & vtrip_sel=0` sets the differential input buffer threshold to $0.5 \cdot v_{ohref}$. `vref_sel=1 & vtrip_sel=1` sets the differential input buffer threshold to `vohref`.

| Bits | Name | Description |
|------|---------------|---|
| 7 | vref_sel_7_6 | sets the vref_sel for the corresponding SIO pair |
| 6 | vtrip_sel_7_6 | sets the vtrip_sel for the corresponding SIO pair |
| 5 | vref_sel_5_4 | sets the vref_sel for the corresponding SIO pair |
| 4 | vtrip_sel_5_4 | sets the vtrip_sel for the corresponding SIO pair |
| 3 | vref_sel_3_2 | sets the vref_sel for the corresponding SIO pair |
| 2 | vtrip_sel_3_2 | sets the vtrip_sel for the corresponding SIO pair |
| 1 | vref_sel_1_0 | sets the vref_sel for the corresponding SIO pair |
| 0 | vtrip_sel_1_0 | sets the vtrip_sel for the corresponding SIO pair |

1.3.263 PRT15_DR

Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DR: 0x400051F0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|------------|------------|---|---|---|---|---|
| SW Access:Reset | R/W:1 | R/W:1 | R/W:000000 | | | | | |
| HW Access | R | R | R | | | | | |
| Name | DataReg_DM | DataReg_DP | DataReg | | | | | |

This register is used to set the output data state for the corresponding GPIO port.

| Bits | Name | Description |
|------|--------------|--|
| 7 | DataReg_DM | The data written to this register specifies the high (Data=1) or low (Data=0) state for the corresponding USB pin when GPIO mode is enabled by setting the USB.USBIO_CR1 iomode bit. |
| 6 | DataReg_DP | The data written to this register specifies the high (Data=1) or low (Data=0) state for the corresponding USB pin when GPIO mode is enabled by setting the USB.USBIO_CR1 iomode bit. |
| 5:0 | DataReg[5:0] | The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. |

1.3.264 PRT15_PS

Port Pin State Register1

Reset: Reset Signals Listed Below

Register : Address

PRT15_PS: 0x400051F1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------------|-----------------|----------|---|---|---|---|---|
| SW Access:Reset | R:U | R:U | R:000000 | | | | | |
| HW Access | R/W | R/W | R/W | | | | | |
| Name | PinState_D M | PinState_D P | PinState | | | | | |

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

| Bits | Name | Description |
|------|---------------|--|
| 7 | PinState_DM | <p>Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin:</p> <p>1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high.</p> <p>1'b0 Reads LOW if the pin voltage is below that threshold, logic low.</p> <p>If the drive mode for the pin is set to High-Z, a read of the pin state will return an undefined value.</p> |
| 6 | PinState_DP | <p>Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin:</p> <p>1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high.</p> <p>1'b0 Reads LOW if the pin voltage is below that threshold, logic low.</p> <p>If the drive mode for the pin is set to High-Z, a read of the pin state will return an undefined value.</p> |
| 5:0 | PinState[5:0] | <p>Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin:</p> <p>1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high.</p> <p>1'b0 Reads LOW if the pin voltage is below that threshold, logic low.</p> <p>If the drive mode for the pin is set to High-Z Analog, the pin state will read 0 independent of the voltage on the pin.</p> |

Reset Table

| resetsignal | field(s) |
|---|-----------------------------|
| N/A | PinState_DP, PinState_DM |
| System reset for retention flops [reset_all_retention] | PinState[5:0] |

1.3.265 PRT15_DM0

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DM0: 0x400051F2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------------|------------------|------------|---|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:000000 | | | | | |
| HW Access | R | R | R | | | | | |
| Name | DriveMode_ DM | DriveMode_ DP | DriveMode | | | | | |

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO chapter section on IO drive modes for detailed information on the eight different drive mode configurations. The PRTx.DM0[7:6] select the drive mode setting for the limited GPIO functionality of the USBIO.

| Bits | Name | Description |
|------|--------------|--|
| 7 | DriveMode_DM | <p>If iomode is set to GPIO mode in USB_USBIO_CR1, driveMode_DM configures the D- pin drive mode. If IOMode is set to USB mode, driveMode_DM is ignored by the D-.</p> <p>1'b0: open drain mode. If dmi is high, DM is open drain, if dmi is low, DM forced low. 1'b1: drive out. The pin follows the Datareg_DM value</p> |
| 6 | DriveMode_DP | <p>Pull-up enable control for USBIO D+ pin.</p> <p>If iomode is set to GPIO mode in USB_USBIO_CR1, driveMode_DP configures the D+ pin drive mode. If IOMode is set to USB mode, driveMode_DP is ignored by the D+.</p> <p>1'b0: open drain mode. If dpi is high, DP is open drain, if dpi is low, DP forced low. 1'b1: drive out. The pin follows the Datareg_DP value</p> |

1.3.265 PRT15_DM0 (continued)

| | | |
|-----|----------------|---|
| 5:0 | DriveMode[5:0] | 1'b0 Corresponding drive mode register bit asserted low. 1'b1 Corresponding drive mode register asserted high. |
|-----|----------------|---|

The combination of the 3 drive mode registers per port determines the drive mode setting for each GPIO pin.

Drive mode is configured on a pad by pad basis using the bit specific drive mode of each pin. Please refer to the IO chapter section on drive modes for detailed information on the eight different drive mode configurations.

$DM [2:0] = \{PRT X .DM2 [y], PRT X .DM1 [y], PRT X .DM0 [y]\}$

DM [2:0] : Complete drive mode setting for pin [y]
 3'b000 : Mode 0, input/output buffers disabled.
 3'b001 : Mode 1, input only
 3'b010 : Mode 2, weak pull-up, strong pull-down
 3'b011 : Mode 3, strong pull-up, weak pull-down
 3'b100 : Mode 4, open drain, strong pull-down
 3'b101 : Mode 5, open drain, strong pull-up
 3'b110 : Mode 6, strong pull-up, strong pull-down
 3'b111 : Mode 7, weak pull-up, weak pull-down

Please reference the IO section in the IROS book 1.

1.3.266 PRT15_DM1

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DM1: 0x400051F3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|--------------|------------|---|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:000000 | | | | | |
| HW Access | R | R | R | | | | | |
| Name | PullUp_en_DM | PullUp_en_DP | DriveMode | | | | | |

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO chapter section on IO drive modes for detailed information on the eight different drive mode configurations. The PRTx.DM1[7:6] enable the 5 kOhm pull-ups on the limited GPIO functionality USBIO pins.

| Bits | Name | Description |
|------|--------------|--|
| 7 | PullUp_en_DM | <p>Pull-up enable control for USBIO D- pin.</p> <p>If iomode is set to GPIO mode in USB_USBIO_CR1, pullUp_en_DM configures the D- 5kOhm pull-up resistor. If IOMode is set to USB mode, pullUp_en_DM is ignored by the D-.</p> <p>1'b1: 5kOhm pull-up enabled on D- 1'b0: no pull-up</p> |
| 6 | PullUp_en_DP | <p>If iomode is set to GPIO mode in USB_USBIO_CR1, pullUp_en_DP configures the D+ 5kOhm pull-up resistor. If IOMode is set to USB mode, pullUp_en_DP is ignored by the D+.</p> <p>1'b1: 5kOhm pull-up enabled on D+ 1'b0: no pull-up</p> |

1.3.266 PRT15_DM1 (continued)

| | | |
|-----|----------------|---|
| 5:0 | DriveMode[5:0] | 1'b0 Corresponding drive mode register bit asserted low. 1'b1 Corresponding drive mode register asserted high. |
|-----|----------------|---|

The combination of the 3 drive mode registers per port determines the drive mode setting for each GPIO pin.

Drive mode is configured on a pad by pad basis using the bit specific drive mode of each pin. Please refer to the IO chapter section on drive modes for detailed information on the eight different drive mode configurations.

$$DM [2:0] = \{PRT X .DM2 [y], PRT X .DM1 [y], PRT X .DM0 [y]\}$$

DM [2:0] : Complete drive mode setting for pin [y]
 3'b000 : Mode 0, input/output buffers disabled.
 3'b001 : Mode 1, input only
 3'b010 : Mode 2, weak pull-up, strong pull-down
 3'b011 : Mode 3, strong pull-up, weak pull-down
 3'b100 : Mode 4, open drain, strong pull-down
 3'b101 : Mode 5, open drain, strong pull-up
 3'b110 : Mode 6, strong pull-up, strong pull-down
 3'b111 : Mode 7, weak pull-up, weak pull-down

Please reference the IO section in the IROS book 1.

1.3.267 PRT15_DM2

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DM2: 0x400051F4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | DriveMode | | | | | |

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO chapter section on IO drive modes for detailed information on the eight different drive mode configurations.

| Bits | Name | Description |
|------|------|-------------|
|------|------|-------------|

1.3.267 PRT15_DM2 (continued)

| | | |
|-----|----------------|---|
| 5:0 | DriveMode[5:0] | 1'b0 Corresponding drive mode register bit asserted low. 1'b1 Corresponding drive mode register asserted high. |
|-----|----------------|---|

The combination of the 3 drive mode registers per port determines the drive mode setting for each GPIO pin.

Drive mode is configured on a pad by pad basis using the bit specific drive mode of each pin. Please refer to the IO chapter section on drive modes for detailed information on the eight different drive mode configurations.

$$DM [2:0] = \{PRT X .DM2 [y], PRT X .DM1 [y], PRT X .DM0 [y]\}$$

DM [2:0] : Complete drive mode setting for pin [y]
 3'b000 : Mode 0, input/output buffers disabled.
 3'b001 : Mode 1, input only
 3'b010 : Mode 2, weak pull-up, strong pull-down
 3'b011 : Mode 3, strong pull-up, weak pull-down
 3'b100 : Mode 4, open drain, strong pull-down
 3'b101 : Mode 5, open drain, strong pull-up
 3'b110 : Mode 6, strong pull-up, strong pull-down
 3'b111 : Mode 7, weak pull-up, weak pull-down

Please reference the IO section in the IROS book 1.

1.3.268 PRT15_SLW

Port slew rate control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_SLW: 0x400051F5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | SlwCtl | | | | | |

The output drive on any I/O pin can be set to a fast edge rate mode (Slew=0) or slow edge rate mode (Slew=1) The slew rate only applies to strong output drive modes, not to resistive drive modes. Slower edge rates normally reduce EMI issues and are recommended when speed is not critical.

| Bits | Name | Description |
|------|-------------|---|
| 5:0 | SlwCtl[5:0] | Each bit controls the output edge rate of the corresponding port pin. 1'b0 Fast edge rate mode 1'b1 Slow edge rate mode |

1.3.269 PRT15_BYP

Port Bypass enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_BYP: 0x400051F6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|------------|---|---|---|---|---|
| SW Access:Reset | R/W:00 | | R/W:000000 | | | | | |
| HW Access | R | | R | | | | | |
| Name | Bypass_usb | | Bypass | | | | | |

The Port Bypass Registers select output data from either the data output register or internal sources such as digital global bus. Shared USB pins must be set to GPIO mode.

| Bits | Name | Description |
|------|-----------------|---|
| 7:6 | Bypass_usb[1:0] | 1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 DMI/DPI outputs from USB drives the corresponding port pin configured in IO mode. <i>GPIO mode must be enabled in order to bypass the shared function USB/IO pins.</i> |
| 5:0 | Bypass[5:0] | 1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 Port logic data register drives the corresponding port pin. <i>The drive mode settings must configure the port to enable the output buffer or the DSI dynamic drive control must configure the output enable for the pad.</i> |

1.3.270 PRT15_BIE

Port Bidirection enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_BIE: 0x400051F7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | BidirectEn | | | | | |

The Port Bidirectional Enable Registers are used to enable dynamic bidirectional mode at any pin.

| Bits | Name | Description |
|------|-----------------|--|
| 5:0 | BidirectEn[5:0] | Each bit controls the bidirectional mode of the corresponding port pin. 1'b0 Normal operation of pad. Drive mode setting configures output buffer 1'b1 Selected dynamic control DSI configures output buffer |

1.3.271 PRT15_INP_DIS

Input buffer disable override

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_INP_DIS: 0x400051F8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|----------------|------------|---|---|---|---|---|
| SW Access:Reset | R/W:1 | R/W:1 | R/W:000000 | | | | | |
| HW Access | R | R | R | | | | | |
| Name | seinput_dis_dm | seinput_dis_dp | Inp_dis | | | | | |

The bits asserted force the input buffers off.

| Bits | Name | Description |
|------|----------------|--|
| 7 | seinput_dis_dm | 1'b1 Single ended input disabled, IO mode disabled for USBIO. 1'b0 Single ended input enabled. |
| 6 | seinput_dis_dp | 1'b1 Single ended input disabled, IO mode disabled for USBIO. 1'b0 Single ended input enabled. |
| 5:0 | Inp_dis[5:0] | 1'b1 Input buffers are disabled, overrides drive mode register settings. 1'b0 Input buffers are configured based on drive mode register settings. |

1.3.272 PRT15_CTL

Port wide control signals

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_CTL: 0x400051F9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|-----------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | vtrip_sel |

The port wide vtrip select register is used to select the input buffer trip point select

| Bits | Name | Description |
|------|-----------|--|
| 0 | vtrip_sel | The GPIO cells include a vtrip_sel signal to alter the input buffer voltage. See Table 1-158. |

Table 1-158. Bit field encoding: vtrip_sel_enum

| Value | Name | Description |
|-------|-------------|---|
| 1'b0 | VTRIP_CMOS | Input buffer functions as a CMOS input buffer. |
| 1'b1 | VTRIP_LVTTL | Input buffer functions as a LVTTL input buffer. |

1.3.273 PRT15_PRT

Port wide configuration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_PRT: 0x400051FA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|------|------------|------|------------|------------|------------|------|
| SW Access:Reset | W:0 | W:0 | W:0 | NA:0 | W:0 | W:0 | W:0 | NA:0 |
| HW Access | R | R | R | NA | R | R | R | NA |
| Name | byPass | slew | bidirectEn | | driveMode2 | driveMode1 | driveMode0 | |

The Port Configuration Register accesses several available configuration registers on a port-wide basis with a single bit write. The write will have no effect on reserved register bits. Please reference the applicable registers definitions.

The port-wide configuration register will not configure the shared USB pins drive mode or pull-up settings.

| Bits | Name | Description |
|------|------------|--|
| 7 | byPass | The Bypass bit sets all the bits for the port bypass register. See Table 1-160. |
| 6 | slew | The slew bit is the same as the corresponding bit in the port slew register. |
| 5 | bidirectEn | The BiDir En bit sets all bits for the port bidirection enable register. See Table 1-159. |
| 3 | driveMode2 | A write to this bit sets all bits for the corresponding drive mode register of the entire port. |
| 2 | driveMode1 | A write to this bit sets all bits for the corresponding drive mode register of the entire port. |
| 1 | driveMode0 | A write to this bit sets all bits for the corresponding drive mode register of the entire port. |

Table 1-159. Bit field encoding: bidir_en_enum

| Value | Name | Description |
|-------|-----------|--------------------------------------|
| 1'b0 | BIDIR_DIS | dynamic bidirectional mode disabled. |
| 1'b1 | BIDIR_EN | dynamic bidirectional mode enabled. |

Table 1-160. Bit field encoding: bypass_en_enum

| Value | Name | Description |
|-------|------------|---------------------------|
| 1'b0 | BYPASS_DIS | bypass function disabled. |
| 1'b1 | BYPASS_EN | bypass function enabled. |

1.3.274 PRT15_BIT_MASK

Bit-mask for Aliased Register access

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_BIT_MASK: 0x400051FB

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------------|-----------------|------------|---|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:000000 | | | | | |
| HW Access | R | R | R | | | | | |
| Name | bit_mask_d m | bit_mask_d p | bit_mask | | | | | |

The bits asserted in the bit-mask register allow direct access to the data register or pin state register via the aliased registers.

| Bits | Name | Description |
|------|---------------|---|
| 7 | bit_mask_dm | Aliased register access of port 15[7:6] is for USB pins when configured to GPIO mode. 1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space. |
| 6 | bit_mask_dp | Aliased register access of port 15[7:6] is for USB pins when configured to GPIO mode. 1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space. |
| 5:0 | bit_mask[5:0] | 1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space. |

1.3.275 PRT15_AMUX

Port Analog global mux bus enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_AMUX: 0x400051FC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | Amux | | | | | |

Analog global mux switch.

| Bits | Name | Description |
|------|-----------|---|
| 5:0 | Amux[5:0] | Connects analog mux bus to the pad when asserted. |

1.3.276 PRT15_AG

Port Analog global enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_AG: 0x400051FD

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | AnalogGlobal | | | | | |

Analog global switch.

| Bits | Name | Description |
|------|-------------------|--|
| 5:0 | AnalogGlobal[5:0] | Connects analog global to the pad when asserted. |

1.3.277 PRT15_LCD_COM_SEG

Port LCD Com seg bits.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_LCD_COM_SEG: 0x400051FE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | com_seg | | | | | |

Selects whether a pin is set as a common or segment drive pin.

| Bits | Name | Description |
|------|--------------|---|
| 5:0 | com_seg[5:0] | Specify whether the pin will drive common or segment mode when LCD is enabled. 1'b0 Segment 1'b1 Common |

1.3.278 PRT15_LCD_EN

Port LCD enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_LCD_EN: 0x400051FF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | Lcd_en | | | | | |

Enables a given pin for LCD drive mode

| Bits | Name | Description |
|------|-------------|---|
| 5:0 | Lcd_en[5:0] | Enable the pin for LCD mode. 1'b0 Disabled 1'b1 Enabled |

1.3.279 PRT0_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OUT_SEL0: 0x40005200

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y*, the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*], PRT [*x*] OUT_SEL0 [*y*]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y*, the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*], PRT [*x*] OUT_SEL0 [*y*]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.280 PRT0_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OUT_SEL1: 0x40005201

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y] , PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y] , PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.281 PRT0_OE_SEL0

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OE_SEL0: 0x40005202

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.282 PRT0_OE_SEL1

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OE_SEL1: 0x40005203

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.283 PRT0_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DBL_SYNC_IN: 0x40005204

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dbl_sync_in | | | | | | | |

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

| Bits | Name | Description |
|------|------------------|--|
| 7:0 | dbl_sync_in[7:0] | When asserted selects to synchronize the data in from the corresponding pad. |

1.3.284 PRT0_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_SYNC_OUT: 0x40005205

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | sync_out | | | | | | | |

The port sync register selects to synchronize the data driving the pad using the existing port data register.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | sync_out[7:0] | When asserted selects to synchronize the data from the DSI driving the corresponding pad. |

1.3.285 PRT0_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_CAPS_SEL: 0x40005206

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | caps_sel | | | | | | | |

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | caps_sel[7:0] | When asserted selects the global DSI to drive dig_glbl_ctl on the pad. |

1.3.286 PRT1_OUT_SELO

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OUT_SELO: 0x40005208

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y] , PRT [x] OUT_SELO [y] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y] , PRT [x] OUT_SELO [y] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.287 PRT1_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OUT_SEL1: 0x40005209

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y*, the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*], PRT [*x*] OUT_SEL0 [*y*]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y*, the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*], PRT [*x*] OUT_SEL0 [*y*]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.288 PRT1_OE_SEL0

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OE_SEL0: 0x4000520A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.289 PRT1_OE_SEL1

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OE_SEL1: 0x4000520B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.290 PRT1_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_DBL_SYNC_IN: 0x4000520C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dbl_sync_in | | | | | | | |

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

| Bits | Name | Description |
|------|------------------|--|
| 7:0 | dbl_sync_in[7:0] | When asserted selects to synchronize the data in from the corresponding pad. |

1.3.291 PRT1_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_SYNC_OUT: 0x4000520D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | sync_out | | | | | | | |

The port sync register selects to synchronize the data driving the pad using the existing port data register.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | sync_out[7:0] | When asserted selects to synchronize the data from the DSI driving the corresponding pad. |

1.3.292 PRT1_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_CAPS_SEL: 0x4000520E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | caps_sel | | | | | | | |

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | caps_sel[7:0] | When asserted selects the global DSI to drive dig_glbl_ctl on the pad. |

1.3.293 PRT2_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OUT_SEL0: 0x40005210

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y*, the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*], PRT [*x*] OUT_SEL0 [*y*]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y*, the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*], PRT [*x*] OUT_SEL0 [*y*]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.294 PRT2_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OUT_SEL1: 0x40005211

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.295 PRT2_OE_SEL0

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OE_SEL0: 0x40005212

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.296 PRT2_OE_SEL1

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OE_SEL1: 0x40005213

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.297 PRT2_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_DBL_SYNC_IN: 0x40005214

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dbl_sync_in | | | | | | | |

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

| Bits | Name | Description |
|------|------------------|--|
| 7:0 | dbl_sync_in[7:0] | When asserted selects to synchronize the data in from the corresponding pad. |

1.3.298 PRT2_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_SYNC_OUT: 0x40005215

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | sync_out | | | | | | | |

The port sync register selects to synchronize the data driving the pad using the existing port data register.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | sync_out[7:0] | When asserted selects to synchronize the data from the DSI driving the corresponding pad. |

1.3.299 PRT2_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_CAPS_SEL: 0x40005216

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | caps_sel | | | | | | | |

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | caps_sel[7:0] | When asserted selects the global DSI to drive dig_glbl_ctl on the pad. |

1.3.300 PRT3_OUT_SELO

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OUT_SELO: 0x40005218

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.301 PRT3_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OUT_SEL1: 0x40005219

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y*, the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*], PRT [*x*] OUT_SEL0 [*y*]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y*, the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*], PRT [*x*] OUT_SEL0 [*y*]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.302 PRT3_OE_SEL0

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OE_SEL0: 0x4000521A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.303 PRT3_OE_SEL1

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OE_SEL1: 0x4000521B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.304 PRT3_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_DBL_SYNC_IN: 0x4000521C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dbl_sync_in | | | | | | | |

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

| Bits | Name | Description |
|------|------------------|--|
| 7:0 | dbl_sync_in[7:0] | When asserted selects to synchronize the data in from the corresponding pad. |

1.3.305 PRT3_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_SYNC_OUT: 0x4000521D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | sync_out | | | | | | | |

The port sync register selects to synchronize the data driving the pad using the existing port data register.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | sync_out[7:0] | When asserted selects to synchronize the data from the DSI driving the corresponding pad. |

1.3.306 PRT3_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_CAPS_SEL: 0x4000521E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | caps_sel | | | | | | | |

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | caps_sel[7:0] | When asserted selects the global DSI to drive dig_glbl_ctl on the pad. |

1.3.307 PRT4_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OUT_SEL0: 0x40005220

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.308 PRT4_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OUT_SEL1: 0x40005221

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.309 PRT4_OE_SEL0

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OE_SEL0: 0x40005222

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.310 PRT4_OE_SEL1

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OE_SEL1: 0x40005223

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.311 PRT4_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_DBL_SYNC_IN: 0x40005224

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dbl_sync_in | | | | | | | |

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

| Bits | Name | Description |
|------|------------------|--|
| 7:0 | dbl_sync_in[7:0] | When asserted selects to synchronize the data in from the corresponding pad. |

1.3.312 PRT4_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_SYNC_OUT: 0x40005225

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | sync_out | | | | | | | |

The port sync register selects to synchronize the data driving the pad using the existing port data register.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | sync_out[7:0] | When asserted selects to synchronize the data from the DSI driving the corresponding pad. |

1.3.313 PRT4_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_CAPS_SEL: 0x40005226

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | caps_sel | | | | | | | |

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | caps_sel[7:0] | When asserted selects the global DSI to drive dig_glbl_ctl on the pad. |

1.3.314 PRT5_OUT_SELO

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OUT_SELO: 0x40005228

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.315 PRT5_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OUT_SEL1: 0x40005229

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.316 PRT5_OE_SEL0

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OE_SEL0: 0x4000522A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.317 PRT5_OE_SEL1

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OE_SEL1: 0x4000522B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.318 PRT5_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_DBL_SYNC_IN: 0x4000522C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dbl_sync_in | | | | | | | |

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

| Bits | Name | Description |
|------|------------------|--|
| 7:0 | dbl_sync_in[7:0] | When asserted selects to synchronize the data in from the corresponding pad. |

1.3.319 PRT5_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_SYNC_OUT: 0x4000522D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | sync_out | | | | | | | |

The port sync register selects to synchronize the data driving the pad using the existing port data register.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | sync_out[7:0] | When asserted selects to synchronize the data from the DSI driving the corresponding pad. |

1.3.320 PRT5_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_CAPS_SEL: 0x4000522E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | caps_sel | | | | | | | |

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | caps_sel[7:0] | When asserted selects the global DSI to drive dig_glbl_ctl on the pad. |

1.3.321 PRT6_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OUT_SEL0: 0x40005230

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.322 PRT6_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OUT_SEL1: 0x40005231

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SELO [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.323 PRT6_OE_SEL0

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OE_SEL0: 0x40005232

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.324 PRT6_OE_SEL1

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OE_SEL1: 0x40005233

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.325 PRT6_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_DBL_SYNC_IN: 0x40005234

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dbl_sync_in | | | | | | | |

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

| Bits | Name | Description |
|------|------------------|--|
| 7:0 | dbl_sync_in[7:0] | When asserted selects to synchronize the data in from the corresponding pad. |

1.3.326 PRT6_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_SYNC_OUT: 0x40005235

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | sync_out | | | | | | | |

The port sync register selects to synchronize the data driving the pad using the existing port data register.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | sync_out[7:0] | When asserted selects to synchronize the data from the DSI driving the corresponding pad. |

1.3.327 PRT6_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_CAPS_SEL: 0x40005236

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | caps_sel | | | | | | | |

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | caps_sel[7:0] | When asserted selects the global DSI to drive dig_glbl_ctl on the pad. |

1.3.328 PRT12_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OUT_SEL0: 0x40005260

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.329 PRT12_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OUT_SEL1: 0x40005261

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y*, the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*], PRT [*x*] OUT_SEL0 [*y*]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y*, the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*], PRT [*x*] OUT_SEL0 [*y*]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.330 PRT12_OE_SEL0

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OE_SEL0: 0x40005262

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.331 PRT12_OE_SEL1

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OE_SEL1: 0x40005263

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOEsel | | | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | portOEsel[7:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.332 PRT12_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_DBL_SYNC_IN: 0x40005264

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dbl_sync_in | | | | | | | |

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

| Bits | Name | Description |
|------|------------------|--|
| 7:0 | dbl_sync_in[7:0] | When asserted selects to synchronize the data in from the corresponding pad. |

1.3.333 PRT12_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SYNC_OUT: 0x40005265

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | sync_out | | | | | | | |

The port sync register selects to synchronize the data driving the pad using the existing port data register.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | sync_out[7:0] | When asserted selects to synchronize the data from the DSI driving the corresponding pad. |

1.3.334 PRT15_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OUT_SEL0: 0x40005278

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.335 PRT15_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OUT_SEL1: 0x40005279

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | portOutsel | | | | | | | |

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port x pin y , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port x pin y , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [x] OUT_SEL1 [y], PRT [x] OUT_SEL0 [y]}** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

| Bits | Name | Description |
|------|-----------------|--|
| 7:0 | portOutsel[7:0] | Selects which of the available taps are selected for the given I/O pin output. |

1.3.336 PRT15_OE_SEL0

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OE_SEL0: 0x4000527A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | portOEsel | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 5:0 | portOEsel[5:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.337 PRT15_OE_SEL1

Dynamic Drive Strength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OE_SEL1: 0x4000527B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | portOEsel | | | | | |

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [x] OE_SEL1 [y] , PRT [x] OE_SEL0 [y] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

| Bits | Name | Description |
|------|----------------|---|
| 5:0 | portOEsel[5:0] | Selects which of the available taps are selected for the given I/O pin. |

1.3.338 PRT15_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DBL_SYNC_IN: 0x4000527C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dbl_sync_in | | | | | | | |

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

| Bits | Name | Description |
|------|------------------|--|
| 7:0 | dbl_sync_in[7:0] | When asserted selects to synchronize the data in from the corresponding pad. |

1.3.339 PRT15_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_SYNC_OUT: 0x4000527D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | sync_out | | | | | | | |

The port sync register selects to synchronize the data driving the pad using the existing port data register.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | sync_out[7:0] | When asserted selects to synchronize the data from the DSI driving the corresponding pad. |

1.3.340 PRT15_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_CAPS_SEL: 0x4000527E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | sync_out | | | | | |

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

| Bits | Name | Description |
|------|---------------|--|
| 5:0 | sync_out[5:0] | When asserted selects the global DSI to drive dig_glbl_ctl on the pad. |

1.3.341 EMIF_NO_UDB

EMIF UDB/NO_UDB Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_NO_UDB: 0x40005400

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | no_udb |

This register indicates whether UDBs are generating external memory control signals or to enable EMIF to generate them for Flow Through Sync SRAM or Asynchronous SRAM. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

| Bits | Name | Description |
|------|--------|--|
| 0 | no_udb | 1'b0: UDB Mode. In this mode EMIF bypasses the external memory transfer request to UDBs and UDBs should be configured to generate the control signals for external memory. 1'b1: NO_UDB Mode. In this mode, the EMIF generates the control signals for Flow through Sync SRAM or Async SRAM |

0x40005401

1.3.342 EMIF_RP_WAIT_STATES

External Memory Interface Read Path Wait States Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_RP_WAIT_STATES: 0x40005401

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|----------------|---|---|
| SW Access:Reset | NA:00000 | | | | | R/W:000 | | |
| HW Access | NA | | | | | R | | |
| Name | | | | | | rp_wait_states | | |

This register configures the additional wait states for read operation. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

| Bits | Name | Description |
|------|---------------------|---|
| 2:0 | rp_wait_states[2:0] | <p>In NO_UDB mode the following table determines the minimum number of additional clock cycles (wait states) required to complete the external read operation (this table assumes EMIF_MEMCLK_DIV is programmed correctly relative to f(HCLK)):</p> <p>0 <= f(HCLK) <= 19: RP_WAIT_STATES can be 0 or more 19 < f(HCLK) <= 33: RP_WAIT_STATES must be >= 1 33 < f(HCLK) <= 41: RP_WAIT_STATES can be 0 or more 41 < f(HCLK) <= 54: RP_WAIT_STATES must be >= 1 54 < f(HCLK) <= 67: RP_WAIT_STATES must be >= 2 67 < f(HCLK) <= 82: RP_WAIT_STATES must be >= 2 82 < f(HCLK) <= 95: RP_WAIT_STATES must be >= 3 95 < f(HCLK) <= 99: RP_WAIT_STATES must be >= 4</p> |

1.3.343 EMIF_MEM_DWN

External Memory Power Down Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_MEM_DWN: 0x40005402

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | mem_pd |

This register puts the external memory into power down mode. This register is active only for Sync SRAM in NO_UDB mode. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

| Bits | Name | Description |
|------|--------|---|
| 0 | mem_pd | 1`b1: External Memory power down. 1`b0: External memory power up |

1.3.344 EMIF_MEMCLK_DIV

External Memory Clock Divider Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_MEMCLK_DIV: 0x40005403

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|------------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | memclk_div | |

This register sets the divider value for external memory clock frequency. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

| Bits | Name | Description |
|------|-----------------|---|
| 1:0 | memclk_div[1:0] | 2'b00: $f(\text{EM_clock}) = f(\text{HCLK})$, when $f(\text{HCLK}) \leq 33\text{MHz}$. 2'b01: $f(\text{EM_clock}) = 1/2f(\text{HCLK})$, when $33\text{MHz} \leq f(\text{HCLK}) \leq 67\text{MHz}$. 2'b10: $f(\text{EM_clock}) = 1/3f(\text{HCLK})$, when $67\text{MHz} \leq f(\text{HCLK}) \leq 99\text{MHz}$. 2'b11: $f(\text{EM_clock}) = 1/4f(\text{HCLK})$, Backup configuration. |

1.3.345 EMIF_CLOCK_EN

EMIF Clock Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_CLOCK_EN: 0x40005404

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|----------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | clock_en |

This register enables the clock for EMIF core logic.

| Bits | Name | Description |
|------|----------|--|
| 0 | clock_en | 1'b0: Disable Clock for EMIF core logic. 1'b1: Enable Clock for EMIF core. Along with this bit, the input 'emif_clk_en' to EMIF block should also be 1'b1 to enable the clock. This input can be made 1'b1 by setting corresponding bit in PM.ACT.CFG5 register in Power Manager. |

1.3.346 EMIF_EM_TYPE

External Memory Type Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_EM_TYPE: 0x40005405

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | em_type |

This register indicates whether to generate control signals for Sync or Async SRAM in NO_UDB mode

| Bits | Name | Description |
|------|---------|--|
| 0 | em_type | 1'b0: Generate control signals for Flow through Sync SRAM (CY7C1324H). 1'b1: Generate control signals for Async SRAM (CY7C1041D). |

1.3.347 EMIF_WP_WAIT_STATES

External Memory Interface Write Path Wait States Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_WP_WAIT_STATES: 0x40005406

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|----------------|---|---|
| SW Access:Reset | NA:00000 | | | | | R/W:000 | | |
| HW Access | NA | | | | | R | | |
| Name | | | | | | wp_wait_states | | |

This register configures the additional wait states for write operation. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

| Bits | Name | Description |
|------|---------------------|---|
| 2:0 | wp_wait_states[2:0] | In NO_UDB mode the following table determines the minimum number of additional clock cycles (wait states) required to complete the external write operation (this table assumes EMIF_MEMCLK_DIV is programmed correctly relative to f(HCLK)): <ul style="list-style-type: none"> 0 <= f(HCLK) <= 29: WP_WAIT_STATES can be 0 or more 29 < f(HCLK) <= 33: WP_WAIT_STATES must be >= 1 33 < f(HCLK) <= 62: WP_WAIT_STATES can be 0 or more 62 < f(HCLK) <= 67: WP_WAIT_STATES must be >= 1 67 < f(HCLK) <= 83: WP_WAIT_STATES can be 0 or more 83 < f(HCLK) <= 99: WP_WAIT_STATES must be >= 1 |

1.3.348 SC[0..3]_CR0

Switched Capacitor Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CR0: 0x40005800

SC1_CR0: 0x40005804

SC2_CR0: 0x40005808

SC3_CR0: 0x4000580C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|---|---------|---|---|------|
| SW Access:Reset | NA:00 | | R/W:00 | | R/W:000 | | | NA:0 |
| HW Access | NA | | R | | R | | | NA |
| Name | | | dft | | mode | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|---|
| 5:4 | dft[1:0] | Enables DFT mode for the switch cap block See Table 1-161. |
| 3:1 | mode[2:0] | Configuration select for the SC block See Table 1-162. |

Table 1-161. Bit field encoding: SC_DFT_ENUM

| Value | Name | Description |
|-------|---------------------------|---|
| 2'h0 | SC_DFT_NORMAL | Normal Operation |
| 2'h1 | SC_DFT_VBOOST | Vboost DFT |
| 2'h2 | SC_DFT_MODE_DEPE NDENT | Mode Dependent (PGA Mode = Voltage Integrator, TIA Mode = Charge Integrator, Naked Opamp Mode = Comparator) |
| 2'h3 | SC_DFT_RESET | DFT Rreset |

Table 1-162. Bit field encoding: SC_MODE_ENUM

| Value | Name | Description |
|--------|--------------------------|-----------------------------------|
| 3'b000 | SC_MODE_NAKED_OP AMP | Naked Op-Amp |
| 3'b001 | SC_MODE_TIA | Transimpedance Amplifier (TIA) |
| 3'b010 | SC_MODE_CTMIXER | Continuous Time Mixer |
| 3'b011 | SC_MODE_NRZ_SH | Discrete Time Mixer - NRZ S/H |
| 3'b100 | SC_MODE_UNITY | Unity Gain Buffer |
| 3'b101 | SC_MODE_1ST_MOD | First Order Modulator |
| 3'b110 | SC_MODE_PGA | Programmable Gain Amplifier (PGA) |
| 3'b111 | SC_MODE_TRACKAND HOLD | Track and Hold |

1.3.349 SC[0..3]_CR1

Switched Capacitor Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CR1: 0x40005801

SC1_CR1: 0x40005805

SC2_CR1: 0x40005809

SC3_CR1: 0x4000580D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------|-------|--------|---|--------|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:00 | | R/W:00 | |
| HW Access | NA | | R | R | R | | R | |
| Name | | | gain | div2 | comp | | drive | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|--|
| 5 | gain | Controls the ratio of the feedback cap for S/H Mixer mode and PGA mode See Table 1-166. |
| 4 | div2 | When 0, the sample clock only needs to be half the desired sample frequency for S/H Mixer mode See Table 1-164. |
| 3:2 | comp[1:0] | Selects between various compensation capacitor sizes See Table 1-163. |
| 1:0 | drive[1:0] | Selects between current settings (I_Load (uA)) in the output buffer See Table 1-165. |

Table 1-163. Bit field encoding: SC_COMP_ENUM

| Value | Name | Description |
|-------|----------------|-------------|
| 2'b00 | SC_COMP_3P0PF | 3.0pF |
| 2'b01 | SC_COMP_3P6PF | 3.6pF |
| 2'b10 | SC_COMP_4P35PF | 4.35pF |
| 2'b11 | SC_COMP_5P1PF | 5.1pF |

Table 1-164. Bit field encoding: SC_DIV2_ENUM

| Value | Name | Description |
|-------|-----------------|--------------------------|
| 1'b0 | SC_DIV2_DISABLE | no frequency division |
| 1'b1 | SC_DIV2_ENABLE | SC CLK is divided by two |

Table 1-165. Bit field encoding: SC_DRIVE_ENUM

| Value | Name | Description |
|-------|--------------|-------------|
| 2'b00 | I_LOAD_175UA | 175 uA |
| 2'b01 | I_LOAD_260UA | 260 uA |
| 2'b10 | I_LOAD_330UA | 330 uA |
| 2'b11 | I_LOAD_400UA | 400 uA |

1.3.349 SC[0..3]_CR1 (continued)

Table 1-166. Bit field encoding: SC_GAIN_ENUM

| Value | Name | Description |
|-------|----------|-------------|
| 1'b0 | GAIN_0DB | 0 dB |
| 1'b1 | GAIN_6DB | 6 dB |

1.3.350 SC[0..3]_CR2

Switched Capacitor Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CR2: 0x40005802

SC1_CR2: 0x40005806

SC2_CR2: 0x4000580A

SC3_CR2: 0x4000580E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---------|---|---|--------|---|---------|-----------|
| SW Access:Reset | R/W:0 | R/W:000 | | | R/W:00 | | R/W:0 | R/W:0 |
| HW Access | R | R | | | R | | R | R |
| Name | pga_gndvref | rval | | | redc | | r20_40b | bias_ctrl |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|---|
| 7 | pga_gndvref | Programmable Gain Amplifier Application - Ground VREF See Table 1-168. |
| 6:4 | rval[2:0] | Programmable Gain Amplifier (PGA) and Transimpedance Amplifier (TIA): Feedback resistor (Rfb) See Table 1-171. |
| 3:2 | redc[1:0] | Another stability control setting. Adjusts capacitance between amplifier output and first stage See Table 1-170. |
| 1 | r20_40b | PGA Mode: input impedance (Rin), Mixer Mode: input and feedback impedance (Rmix) See Table 1-169. |
| 0 | bias_ctrl | Toggles the bias current in the amplifier between normal and 1/2 See Table 1-167. |

Table 1-167. Bit field encoding: SC_BIAS_CONTROL_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | BIAS_1X | 1x current reference reduces bandwidth to increase stability |
| 1'b1 | BIAS_2X | normal operation - 2x current reference to increase bandwidth |

Table 1-168. Bit field encoding: SC_PGA_GNDVREF_ENUM

| Value | Name | Description |
|-------|-------------------|-------------------|
| 1'b0 | SC_PGA_GNDVREF_DI | VREF not grounded |
| | S | |
| 1'b1 | SC_PGA_GNDVREF_E | VREF grounded |
| | N | |

Table 1-169. Bit field encoding: SC_R20_40B_ENUM

| Value | Name | Description |
|-------|----------------|-------------|
| 1'b0 | SC_R20_40B_40K | 40kOhm |

1.3.350 SC[0..3]_CR2 (continued)

Table 1-169. Bit field encoding: SC_R20_40B_ENUM

| | | |
|------|----------------|--------|
| 1'b1 | SC_R20_40B_20K | 20kOhm |
|------|----------------|--------|

Table 1-170. Bit field encoding: SC_REDC_ENUM

| Value | Name | Description |
|-------|------------|--|
| 2'b00 | SC_REDC_00 | Varies depending on mode. See Switched Cap documentation |
| 2'b01 | SC_REDC_01 | Varies depending on mode. See Switched Cap documentation |
| 2'b10 | SC_REDC_10 | Varies depending on mode. See Switched Cap documentation |
| 2'b11 | SC_REDC_11 | Varies depending on mode. See Switched Cap documentation |

Table 1-171. Bit field encoding: SC_RVAL_ENUM

| Value | Name | Description |
|--------|--------------|-------------|
| 3'b000 | SC_RVAL_20 | 20 kOhm |
| 3'b001 | SC_RVAL_30 | 30 kOhm |
| 3'b010 | SC_RVAL_40 | 40 kOhm |
| 3'b011 | SC_RVAL_80 | 80 kOhm |
| 3'b100 | SC_RVAL_120 | 120 kOhm |
| 3'b101 | SC_RVAL_250 | 250 kOhm |
| 3'b110 | SC_RVAL_500 | 500 kOhm |
| 3'b111 | SC_RVAL_1000 | 1 MegaOhm |

1.3.351 DAC[0..3]_CR0

DAC Block Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_CR0: 0x40005820

DAC1_CR0: 0x40005824

DAC2_CR0: 0x40005828

DAC3_CR0: 0x4000582C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------|--------|---|-------|------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:00 | | R/W:0 | NA:0 |
| HW Access | NA | | | R | R | | R | NA |
| Name | | | | mode | range | | hs | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|--|
| 4 | mode | Mode Bit See Table 1-173. |
| 3:2 | range[1:0] | Ranges for mode=0 (VDAC) and mode=1 (IDAC) See Table 1-174. |
| 1 | hs | High Speed Bit See Table 1-172. |

Table 1-172. Bit field encoding: DAC_HS_ENUM

| Value | Name | Description |
|-------|------------------|---------------------------|
| 1'b0 | DAC_HS_LOWPOWER | regular (low power) |
| 1'b1 | DAC_HS_HIGHSPEED | high speed (higher power) |

Table 1-173. Bit field encoding: DAC_MODE_ENUM

| Value | Name | Description |
|-------|------------|-------------|
| 1'b0 | DAC_MODE_V | voltage DAC |
| 1'b1 | DAC_MODE_I | current DAC |

Table 1-174. Bit field encoding: DAC_RANGE_ENUM

| Value | Name | Description |
|-------|-------------|---|
| 2'b00 | DAC_RANGE_0 | x0=0V to 4*vref (1.024V); 0 to 31.875uA |
| 2'b01 | DAC_RANGE_1 | x1=0V to 16*vref (4.096V); 0 to 255uA |
| 2'b10 | DAC_RANGE_2 | x0=0V to 4*vref (1.024V); 0 to 2.040mA |
| 2'b11 | DAC_RANGE_3 | x1=0V to 16*vref (4.096V); not used |

1.3.352 DAC[0..3]_CR1

DAC Block Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_CR1: 0x40005821

DAC1_CR1: 0x40005825

DAC2_CR1: 0x40005829

DAC3_CR1: 0x4000582D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------|----------------|---------|---------|---------|---------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R | R | R | R | R | R |
| Name | | | mx_data | reset_u db_ en | mx_idir | idirbit | mx_ioff | ioffbit |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------------|---|
| 5 | mx_data | Select DATA source See Table 1-176. |
| 4 | reset_u db_ en | DAC reset enable See Table 1-179. |
| 3 | mx_idir | Mux selection for DAC current direction control See Table 1-177. |
| 2 | idirbit | register source for DAC current direction See Table 1-175. |
| 1 | mx_ioff | Mux selection for DAC current off control See Table 1-178. |
| 0 | ioffbit | register source for DAC current off |

Table 1-175. Bit field encoding: IDIRBIT_ENUM

| Value | Name | Description |
|-------|----------|----------------|
| 1'b1 | IDIR_SNK | Current sink |
| 1'b0 | IDIR_SRC | Current source |

Table 1-176. Bit field encoding: MX_DATA_ENUM

| Value | Name | Description |
|-------|-------------|----------------------------------|
| 1'b0 | MX_DATA_REG | Select register source (DACxn_D) |
| 1'b1 | MX_DATA_UDB | Select UDB source |

Table 1-177. Bit field encoding: MX_IDIR_ENUM

| Value | Name | Description |
|-------|-------------|----------------------------------|
| 1'b0 | MX_IDIR_REG | Register source idirbit selected |
| 1'b1 | MX_IDIR_UDB | UDB ictrl selected |

1.3.352 DAC[0..3]_CR1 (continued)

Table 1-178. Bit field encoding: MX_IOFF_ENUM

| Value | Name | Description |
|-------|-------------|----------------------------------|
| 1'b0 | MX_IOFF_REG | Register source ioffbit selected |
| 1'b1 | MX_IOFF_UDB | UDB ictrl selected |

Table 1-179. Bit field encoding: RESET_UDB_EN_ENUM

| Value | Name | Description |
|-------|--------------------------|--|
| 1'b0 | RESET_UDB_EN_DISA BLE | Disable DAC Reset Source from UDB (System reset always resets) |
| 1'b1 | RESET_UDB_EN_ENA BLE | Enable DAC Reset Source from UDB |

1.3.353 DAC[0..3]_TST

DAC Block Test Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_TST: 0x40005822

DAC1_TST: 0x40005826

DAC2_TST: 0x4000582A

DAC3_TST: 0x4000582E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|---|---|---|---|
| SW Access:Reset | NA:000 | | | R/W:00000 | | | | |
| HW Access | NA | | | R | | | | |
| Name | | | | test | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|---|
| 4:0 | test[4:0] | 5 test-select bits for bringing out internal nodes through an analog mux. Table shows internal net and test description See Table 1-180. |

Table 1-180. Bit field encoding: DAC_TEST_SEL

| Value | Name | Description |
|----------|-----------------------------------|---|
| 5'b00000 | DAC_TEST_SEL_DEFA ULT | Default; Normal Operation mode |
| 5'b00001 | DAC_TEST_SEL_IREF_ CALIBRATION | Calibration Step 1 (Iref); Measurement: Read out the dac_vout and test_io to calculate R=(Vdac_vout-Vtest_io)/Iref; IDAC (source) mode (mode=1 (IDAC), iout_sel=0 (source)) |
| 5'b00010 | DAC_TEST_SEL_IDAC_ CALIBRATION | Calibration Step 2 and Step 3; IDAC source/sink calibration; Step 2 Measurement: Using the R value calibrate IDAC source mode * (mode=1 (IDAC), iout_sel=0 (source)); Step 3 Measurement: Using the R value calibrate IDAC sink mode * (mode=1 (IDAC), iout_sel=1 (sink)) |
| 5'b00100 | DAC_TEST_SEL_VB | DFT, Observe Vb; vpwra-vth (0.6-0.7V); Normal operation mode (mode=0 (VDAC), iout_sel=dont care) |
| 5'b01000 | DAC_TEST_SEL_VFB | DFT, Observe Vfb; 256mV; Normal operation mode (mode=0 (VDAC), iout_sel=dont care) |
| 5'b10000 | DAC_TEST_SEL_IREF | DFT, measure Iref directly; Iref, 16uA sink nominal; DFT mode (mode=1 (IDAC), iout_sel=dont care) |

1.3.354 CMP[0..3]_CR

Comparator Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_CR: 0x40005840

CMP1_CR: 0x40005841

CMP2_CR: 0x40005842

CMP3_CR: 0x40005843

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------|-------|--------|-------|-------------|--------|---|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | |
| HW Access | NA | R | R | R | R | R | R | |
| Name | | filt | hyst | cal_en | mx_ao | pd_override | sel | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|---|
| 6 | filt | enables a glitch filter at the output of the comparator See Table 1-182. |
| 5 | hyst | enables a hysteresis of 10mV typ. See Table 1-183. |
| 4 | cal_en | enables shorting of the two comparator inputs for trim calibration purposes See Table 1-181. |
| 3 | mx_ao | comparator sleep always-on logic mux control See Table 1-184. |
| 2 | pd_override | Power down override to allow comparator to continue operating during sleep. Note: if chip wants to wakeup using p3comp resource, this bit must be set to 1. See Table 1-185. |
| 1:0 | sel[1:0] | Selects the mode of operation of the comparator See Table 1-186. |

Table 1-181. Bit field encoding: CMP_CAL_EN_ENUM

| Value | Name | Description |
|-------|-------------------|---------------------|
| 1'b0 | CMP_CAL_EN_DISABL | Disable calibration |
| | E | |
| 1'b1 | CMP_CAL_EN_ENABLE | Enable calibration |

Table 1-182. Bit field encoding: CMP_FILT_ENUM

| Value | Name | Description |
|-------|------------------|-----------------------|
| 1'b0 | CMP_FILT_DISABLE | Disable glitch filter |
| 1'b1 | CMP_FILT_ENABLE | Enable glitch filter |

1.3.354 CMP[0..3]_CR (continued)

Table 1-183. Bit field encoding: CMP_HYST_ENUM

| Value | Name | Description |
|-------|------------------|--------------------|
| 1'b1 | CMP_HYST_DISABLE | Disable hysteresis |
| 1'b0 | CMP_HYST_ENABLE | Enable hysteresis |

Table 1-184. Bit field encoding: CMP_MX_AO_ENUM

| Value | Name | Description |
|-------|------------------|---|
| 1'b0 | CMP_MX_AO_BYPASS | Bypass comparator sleep always-on logic |
| 1'b1 | CMP_MX_AO_ENABLE | Enable comparator sleep always-on logic |

Table 1-185. Bit field encoding: CMP_PD_OVERRIDE_ENUM

| Value | Name | Description |
|-------|-------------------------|---------------------------|
| 1'b0 | CMP_PD_OVERRIDE_DISABLE | Don't override power down |
| 1'b1 | CMP_PD_OVERRIDE_ENABLE | Override power down |

Table 1-186. Bit field encoding: SEL_ENUM

| Value | Name | Description |
|-------|-------------|---|
| 2'b00 | SEL_SLOW | slow mode |
| 2'b01 | SEL_FAST | fast mode |
| 2'b10 | SEL_LP | ultra low power mode. Note: if chip wants to wakeup using p3comp resource, p3comp shall be in ultra low power mode and pd_override bit must be set to 1 |
| 2'b11 | SEL_ILLEGAL | Illegal Mode |

1.3.355 LUT[0..3]_CR

LUT Config Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT0_CR: 0x40005848

LUT1_CR: 0x4000584A

LUT2_CR: 0x4000584C

LUT3_CR: 0x4000584E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | q | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--------------|
| 3:0 | q[3:0] | LUT function |

[See Table 1-187.](#)

Table 1-187. Bit field encoding: LUT_Q_ENUM

| Value | Name | Description |
|-------|------------------|-------------|
| 4'h0 | LUT_Q_0 | FALSE (0) |
| 4'h1 | LUT_Q_A_AND_B | A AND B |
| 4'h2 | LUT_Q_A_AND_NOTB | A AND !B |
| 4'h3 | LUT_Q_A | A |
| 4'h4 | LUT_Q_NOTA_AND_B | !A AND B |
| 4'h5 | LUT_Q_B | B |
| 4'h6 | LUT_Q_A_XOR_B | A XOR B |
| 4'h7 | LUT_Q_A_OR_B | A OR B |
| 4'h8 | LUT_Q_A_NOR_B | A NOR B |
| 4'h9 | LUT_Q_A_XNOR_B | A XNOR B |
| 4'ha | LUT_Q_NOTB | !B |
| 4'hb | LUT_Q_A_OR_NOTB | A OR !B |
| 4'hc | LUT_Q_NOTA | !A |
| 4'hd | LUT_Q_NOTA_OR_B | !A OR B |
| 4'he | LUT_Q_A_NAND_B | A NAND B |
| 4'hf | LUT_Q_1 | TRUE (1) |

1.3.356 LUT[0..3]_MX

LUT Input Mux Config Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT0_MX: 0x40005849

LUT1_MX: 0x4000584B

LUT2_MX: 0x4000584D

LUT3_MX: 0x4000584F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|---|-------|---|--------|---|
| SW Access:Reset | NA:00 | | R/W:00 | | NA:00 | | R/W:00 | |
| HW Access | NA | | R | | NA | | R | |
| Name | | | mx_b | | | | mx_a | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|--|
| 5:4 | mx_b[1:0] | Mux Select for LUT Input B See Table 1-188. |
| 1:0 | mx_a[1:0] | Mux Select for LUT Input A See Table 1-188. |

Table 1-188. Bit field encoding: LUT_MUX_ENUM

| Value | Name | Description |
|-------|-----------|----------------------|
| 2'h0 | LUT_MUX_0 | CMP0 output selected |
| 2'h1 | LUT_MUX_1 | CMP1 output selected |
| 2'h2 | LUT_MUX_2 | CMP2 output selected |
| 2'h3 | LUT_MUX_3 | CMP3 output selected |

1.3.357 OPAMP[0..3]_CR

Analog Output Buffer Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_CR: 0x40005858

OPAMP1_CR: 0x4000585A

OPAMP2_CR: 0x4000585C

OPAMP3_CR: 0x4000585E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|----------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | pwr_mode | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------------|-------------|
| 1:0 | pwr_mode[1:0] | Power Mode |

[See Table 1-189.](#)

Table 1-189. Bit field encoding: OPAMP_PWR_MODE_ENUM

| Value | Name | Description |
|-------|---------------------------|---------------|
| 2'h0 | OPAMP_PWR_MODE_ TIA | TIA (default) |
| 2'h1 | OPAMP_PWR_MODE_ SLOW | Slow |
| 2'h2 | OPAMP_PWR_MODE_ MEDIUM | Medium |
| 2'h3 | OPAMP_PWR_MODE_ FAST | Fast |

@0x40005858 + [0..3 * 0x2] + 0x1

1.3.358 OPAMP[0..3]_RSVD

OPAMP reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_RSVD: 0x40005859

OPAMP1_RSVD: 0x4000585B

OPAMP2_RSVD: 0x4000585D

OPAMP3_RSVD: 0x4000585F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|------------------------------|
| 7:0 | RSVD[7:0] | Reserved for OPAMP expansion |

1.3.359 LCDDAC_CR0

LCD Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_CR0: 0x40005868

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|--------|---|---|------------------|------|----------|---|
| SW Access:Reset | R/W:0 | NA:000 | | | R/W:0 | NA:0 | R/W:00 | |
| HW Access | R | NA | | | R | NA | R | |
| Name | lp_en | | | | continuous_drive | | bias_sel | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------------|--|
| 7 | lp_en | Setting this bit allows the UDB to gate the Low Power Ack for the LCD Subsystem (lcd_lp_ack_n); When set to 0, the LCD subsystem LP ack is directly driven by the lpreq from the power manager See Table 1-192. |
| 3 | continuous_drive | This bit allows the LCDDAC to remain active when the chip goes to sleep. In this mode, the LCD-DAC drives the LCD pins while the LCD Driver is in bypass mode See Table 1-191. |
| 1:0 | bias_sel[1:0] | Selects the LCD bias/multiplex ratio See Table 1-190. |

Table 1-190. Bit field encoding: LCDDAC_BIAS_SELECT_ENUM

| Value | Name | Description |
|-------|-------------------------------|---|
| 2'b00 | LCDDAC_BIAS_SELECT_1DIV3 | v0=2.0-supply; v1=0.666*v0; v2=0.333*v0; v3=0.666*v0; v4=0.333*v0; Multiplex ratios=2:1,3:1,4:1 |
| 2'b01 | LCDDAC_BIAS_SELECT_1DIV4 | v0=2.0-supply; v1=0.750*v0; v2=0.500*v0; v3=0.500*v0; v4=0.250*v0; Multiplex ratio=8:1 |
| 2'b10 | LCDDAC_BIAS_SELECT_1DIV5 | v0=2.0-supply; v1=0.800*v0; v2=0.600*v0; v3=0.400*v0; v4=0.200*v0; Multiplex ratio=16:1 |
| 2'b11 | LCDDAC_BIAS_SELECT_1DIV5_ALSO | v0=2.0-supply; v1=0.800*v0; v2=0.600*v0; v3=0.400*v0; v4=0.200*v0; Multiplex ratio=16:1 |

Table 1-191. Bit field encoding: LCDDAC_CONTINUOUS_DRIVE_ENUM

| Value | Name | Description |
|-------|------------------------------------|--|
| 1'b0 | LCDDAC_CONTINUOUS_DRIVE_CANCATCHZ | LCDDAC is powered down when the chip is in sleep |
| 1'b1 | LCDDAC_CONTINUOUS_DRIVE_LIVINGDEAD | LCDDAC is active when the chip is in sleep |

Table 1-192. Bit field encoding: LCD_LP_EN_ENUM

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.359 LCDDAC_CR0 (continued)

Table 1-192. Bit field encoding: LCD_LP_EN_ENUM

| | | |
|------|-------------------|-------------------------|
| 1'b0 | LCD_LP_EN_DISABLE | LCD UDB LP Ack Disabled |
| | D | |
| 1'b1 | LCD_LP_EN_ENABLED | LCD UDB LP Ack Enabled |

1.3.360 LCDDAC_CR1

LCDDAC Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_CR1: 0x40005869

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------|--------------|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0 | R/W:000000 | | | | | |
| HW Access | NA | R | R | | | | | |
| Name | | nc | contrast_ctl | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------------|--|
| 6 | nc | Not connected |
| 5:0 | contrast_ctl[5:0] | LCD Contrast control setting. Bit6 Not Connected; Step size is 27.3 mV @ 3.0 V supply and 50 mV @ 5.5 V supply; Min V0 should be 2 V. To achieve this, use code value 6'h00 for 5.5 V supply and 6'h21 for 3 V supply. Max V0 is equal to supply level for code value 6'h3f |

[See Table 1-193.](#)

Table 1-193. Bit field encoding: LCDDAC_D_ENUM

| Value | Name | Description |
|-------|--------------|-------------|
| 6'h0 | LCDDAC_D_MIN | Minimum |
| 6'h3f | LCDDAC_D_MAX | Max |

1.3.361 LCDDRV_CR

LCD Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDRV_CR: 0x4000586A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|-------|--------|--------|----------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | bypass_en | pts | invert | mode_0 | dispBlnk |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|--|
| 4 | bypass_en | <p>This bit enables bypassing the LCD Driver, so that the LCDDAC is driving the LCD glass. The LCDDAC continuous_drive bit is also set to allow the LCDDAC to remain active when the chip goes to sleep.</p> <p>See Table 1-194.</p> |
| 3 | pts | <p>pts (pull-to-supply) signal enables the LCD Driver to be able to drive to supply level. In normal operation, the output of the LCD Driver is limited to VIO-0.5V whereas when the pts mode is enabled, the output can reach to VIO.</p> <p>See Table 1-198.</p> |
| 2 | invert | <p>Invert LCD Display (invert display data on all pins configured as segments)</p> <p>See Table 1-196.</p> |
| 1 | mode_0 | <p>LCD Driver mode[0]; mode[2:1] come from DSI</p> <p>HiDrive modes: HiDrive mode is used to refresh or to write new data to the LCD glass. Reason for different drive strengths is to save power and reduce AC coupling. There are cases where common drivers face more load than segment drivers. For these cases stronger commons should be selected. Also, to reduce AC coupling, the common drivers should be stronger than segment drivers (assuming number of common pins are less than segment pins). For cases where there is a big glass with number of common pins is close to or equal to segment pins, com=4x and seg=4x should be used to reduce charge times LoDrive modes: The purpose of this mode is to sustain the voltage on the LCD in the case of a leakage. In the case of higher leakage due to glass type, glass size or environment temperature; stronger LoDrive mode can be used.</p> <p>Control Bits Mode Drive Strength mode[2:0]</p> <p>000 HiDrive seg=1x, com=1x 001 HiDrive seg=1x, com=2x 010 HiDrive seg=1x, com=4x 011 HiDrive seg=2x, com=2x 100 HiDrive seg=2x, com=4x 101 HiDrive seg=4x, com=4x 110 LoDrive seg=1x, com=1x 111 LoDrive seg=2x, com=2x</p> <p>See Table 1-197.</p> |

1.3.361 LCDDRV_CR (continued)

0 dispbink LCD Display Blank

[See Table 1-195.](#)

Table 1-194. Bit field encoding: LCD_BYPASS_EN_ENUM

| Value | Name | Description |
|-------|---------------------------------------|-------------|
| 1'b0 | LCD_BYPASS_EN_LCD DRV_DRIVES_GLASS | Normal mode |
| 1'b1 | LCD_BYPASS_EN_LCD DAC_DRIVES_GLASS | Bypass mode |

Table 1-195. Bit field encoding: LCD_DISPBLNK_ENUM

| Value | Name | Description |
|-------|--------------------|---|
| 1'b0 | LCD_DISPBLNK_HIZ | When in a low power mode, set output buffer in LCD Drivers to hi impedance. This leaves intact the last image driven to the LCD display (charge will slowly leak off and the image will fade unless updated). |
| 1'b1 | LCD_DISPBLNK_BLANK | When in a low power mode, set output buffer in LCD Drivers to ground. Blanks the LCD display. |

Table 1-196. Bit field encoding: LCD_INVERT_ENUM

| Value | Name | Description |
|-------|--------------------|------------------|
| 1'b0 | LCD_INVERT_DISABLE | Normal display |
| 1'b1 | LCD_INVERT_ENABLE | Inverted display |

Table 1-197. Bit field encoding: LCD_MODE_0_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | LCD_MODE_0_0 | Depends on other signals |
| 1'b1 | LCD_MODE_0_1 | Depends on other signals |

Table 1-198. Bit field encoding: LCD_PTS_ENUM

| Value | Name | Description |
|-------|-----------|-----------------------------------|
| 1'b0 | LCD_PTS_0 | normal operation, VOUT = VIO-0.5V |
| 1'b1 | LCD_PTS_1 | pts mode enabled, VOUT = VIO |

1.3.362 LCDTMR_CFG

LCD Timer Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDTMR_CFG: 0x4000586B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---------|----------|
| SW Access:Reset | R/W:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | R | | | | | | R | R |
| Name | period | | | | | | clk_sel | en_timer |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 7:2 | period[5:0] | LCD timer period / lcd_int period; change only when LCD timer is disabled |
| 1 | clk_sel | LCD timer clock source selection bit; change only when LCD timer is disabled See Table 1-199. |
| 0 | en_timer | LCD timer enable bit See Table 1-200. |

Table 1-199. Bit field encoding: LCD_CLK_SEL_ENUM

| Value | Name | Description |
|-------|--------------------|---|
| 1'b0 | LCD_CLK_SEL_ILO_1K | ILO 1K |
| 1'b1 | LCD_CLK_SEL_ONEPP | onepps (One Pulse Per Second) from 32k External Watch Crystal |

Table 1-200. Bit field encoding: LCD_EN_TIMER_ENUM

| Value | Name | Description |
|-------|--------------------|-----------------------|
| 1'b0 | LCD_EN_TIMER_DISAB | LCD Timer is disabled |
| 1'b1 | LCD_EN_TIMER_ENAB | LCD Timer is enabled |

1.3.363 BG_CR0

Bandgap Precision Reference Control 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BG_CR0: 0x4000586C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------------|-----------------|----------|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:00 | |
| HW Access | NA | | | | R | R | R | |
| Name | | | | | bg_vda_res_en | bg_vda_swabusl0 | cmp_mxvn | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 3 | bg_vda_res_en | Bandgap VDA See Table 1-201. |
| 2 | bg_vda_swabusl0 | Switch Control for VDA Bandgap output to abusl0 connection See Table 1-202. |
| 1:0 | cmp_mxvn[1:0] | Mux for comparator reference cmp1_vref See Table 1-203. |

Table 1-201. Bit field encoding: BG_VDA_RES_EN_ENUM

| Value | Name | Description |
|-------|---------------------------|-------------|
| 1'h0 | BG_VDA_RES_EN_VD A | VDA |
| 1'h1 | BG_VDA_RES_EN_HAL FVDA | VDA/2 |

Table 1-202. Bit field encoding: BG_VDA_SWABUSL0_ENUM

| Value | Name | Description |
|-------|--------------------------------|--------------------------------------|
| 1'h0 | BG_VDA_SWABUSL0_ DISCONNECT | not connected |
| 1'h1 | BG_VDA_SWABUSL0_ CONNECT | Connect VDA Bandgap output to abusl0 |

Table 1-203. Bit field encoding: CMP_MXVN_ENUM

| Value | Name | Description |
|-------|---------------|-----------------------------------|
| 2'h0 | CMP_MXVN_NC | not connected (NC) |
| 2'h1 | CMP_MXVN_VDA | Bandgap VREF_VDA output selected |
| 2'h2 | CMP_MXVN_CMP1 | Bandgap VREF_CMP1 output selected |
| 2'h2 | CMP_MXVN_RSVD | Reserved |

0x4000586d

1.3.364 BG_RSVD

Bandgap Precision Reference Reserved Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BG_RSVD: 0x4000586D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|-------------|
| 7:0 | RSVD[7:0] | Reserved |

1.3.365 BG_DFT0

Bandgap Precision Reference DFT Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BG_DFT0: 0x4000586E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------------|------------|-----------|-------------|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:00 | |
| HW Access | NA | | | R | R | R | R | |
| Name | | | | bg_dft_vsel | bg_dft_sel | bg_dft_en | bg_dft_isel | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------------|---|
| 4 | bg_dft_vsel | Mux for DFT to select either vgnnd or the reference voltage See Table 1-207. |
| 3 | bg_dft_sel | BG_DFT_OUT mux selection - V_DFT (voltage) or I_DFT (current) See Table 1-206. |
| 2 | bg_dft_en | DFT enable for bandgap See Table 1-204. |
| 1:0 | bg_dft_isel[1:0] | Mux for DFT to select the current signals See Table 1-205. |

Table 1-204. Bit field encoding: BG_DFT_EN_ENUM

| Value | Name | Description |
|-------|-------------------|-------------|
| 1'b0 | BG_DFT_EN_DISABLE | disabled |
| 1'b1 | BG_DFT_EN_ENABLE | enabled |

Table 1-205. Bit field encoding: BG_DFT_ISEL

| Value | Name | Description |
|-------|--------------------|--|
| 2'h0 | BG_DFT_ISEL_IPTAT | iptat |
| 2'h1 | BG_DFT_ISEL_ICTAT | ictat |
| 2'h2 | BG_DFT_ISEL_INL | digital output for trimming inl temperature cross over point |
| 2'h3 | BG_DFT_ISEL_IBG10U | ibg10u |

Table 1-206. Bit field encoding: BG_DFT_SEL_ENUM

| Value | Name | Description |
|-------|--------------|-------------|
| 1'b0 | BG_DFT_SEL_V | voltage |
| 1'b1 | BG_DFT_SEL_I | current |

Table 1-207. Bit field encoding: BG_DFT_VSEL_ENUM

| Value | Name | Description |
|-------|------------------|-------------|
| 1'b0 | BG_DFT_VSEL_VOUT | VOUT |
| 1'b1 | BG_DFT_VSEL_VGND | vgnd |

1.3.366 BG_DFT1

Bandgap Precision Reference DFT Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BG_DFT1: 0x4000586F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | bgregfs_dft_sel | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------------------|---|
| 3:0 | bgregfs_dft_sel[3:0] | BGREFS_DFT_OUT (routed to DFT_MUX3) mux selection |

[See Table 1-208.](#)

Table 1-208. Bit field encoding: BGREFS_DFT_SEL_ENUM

| Value | Name | Description |
|-------|--|-------------|
| 4'h0 | BGREFS_DFT_SEL_VG vgnd | ND_0x0 |
| 4'h1 | BGREFS_DFT_SEL_VR 1.2V (VREF_LVI_HVI) | EF_LVI_HVI |
| 4'h2 | BGREFS_DFT_SEL_VR 0.8 V (VREF_BOOST) | EF_BOOST |
| 4'h3 | BGREFS_DFT_SEL_VR 0.256V (VREF_DAC) | EF_DAC |
| 4'h4 | BGREFS_DFT_SEL_VR 1.024V (VREF_XOSC) | EF_XOSC |
| 4'h5 | BGREFS_DFT_SEL_VR 0.6V (VREF_TSENSE) | EF_TSENSE |
| 4'h6 | BGREFS_DFT_SEL_VR 1.024V (VREF_PRES) | EF_PRES |
| 4'h7 | BGREFS_DFT_SEL_VR 1.024V (VREF_SC0) | EF_SC0 |
| 4'h8 | BGREFS_DFT_SEL_VR 0.8V (VREF_IMO) | EF_IMO |
| 4'h9 | BGREFS_DFT_SEL_V0 0.256V (trim buffer) | P256 |
| 4'hA | BGREFS_DFT_SEL_VG vgnd | ND_0xA |
| 4'hB | BGREFS_DFT_SEL_V0 0.7V (trim buffer) | P7 |
| 4'hC | BGREFS_DFT_SEL_VG vgnd | ND_0xC |
| 4'hD | BGREFS_DFT_SEL_V1 1.024 (buffer amp) | P024 |

1.3.366 BG_DFT1 (continued)

Table 1-208. Bit field encoding: BGREFS_DFT_SEL_ENUM

| | |
|------|---|
| 4'hE | BGREFS_DFT_SEL_VG vgn ND_0xE |
| 4'hF | BGREFS_DFT_SEL_VR 0.8V (VREF_LDO) EF_LDO |

1.3.367 CAPSL_CFG0

Capsense Reference Driver Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSL_CFG0: 0x40005870

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|---|---------|--------|---|-------|--------|
| SW Access:Reset | R/W:0 | NA:00 | | R/W:0 | R/W:00 | | R/W:0 | R/W:0 |
| HW Access | R | NA | | R | R | | R | R |
| Name | mxcmp | | | ch_cont | refsel | | boost | out_en |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 7 | mxcmp | Reference Buffer channel to comparator vp mux select See Table 1-211. |
| 4 | ch_cont | Reference Buffer Channel Selection Control See Table 1-210. |
| 3:2 | refsel[1:0] | Reference Selection See Table 1-213. |
| 1 | boost | High power mode See Table 1-209. |
| 0 | out_en | Reference Buffer Output enable See Table 1-212. |

Table 1-209. Bit field encoding: CS_BOOST_ENUM

| Value | Name | Description |
|-------|-----------------|---|
| 1'b0 | CS_BOOST_NORMAL | Normal Drive (typically 10-60pF) |
| 1'b1 | CS_BOOST_HIGH | High Drive (typical load = 0.1 to 20nF) |

Table 1-210. Bit field encoding: CS_CH_CONT_ENUM

| Value | Name | Description |
|-------|---------------|-------------------------|
| 1'b0 | CS_CH_CONT_VS | Ch2: Vssa path |
| 1'b1 | CS_CH_CONT_AG | Ch1: Analog Global Path |

Table 1-211. Bit field encoding: CS_MXCMP_ENUM

| Value | Name | Description |
|-------|-------------|---|
| 1'b0 | CS_MXCMP_AG | Analog Global path connected to comparator vp mux (ch1) |
| 1'b1 | CS_MXCMP_VS | Vssa path connected to comparator vp mux (ch2) |

Table 1-212. Bit field encoding: CS_OUT_EN_ENUM

| Value | Name | Description |
|-------|---------------|-------------|
| 1'b0 | CS_OUT_EN_HIZ | tristate |

1.3.367 CAPSL_CFG0 (continued)

Table 1-212. Bit field encoding: CS_OUT_EN_ENUM

| | | |
|------|--------------|-----------|
| 1'b1 | CS_OUT_EN_ON | connected |
|------|--------------|-----------|

Table 1-213. Bit field encoding: CS_REFSEL_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 2'h0 | CS_REFSEL_1P024 | 1.024 V Bandgap Reference |
| 2'h1 | CS_REFSEL_1P2 | 1.2 V Bandgap Reference |
| 2'h2 | CS_REFSEL_TREFSEL | dac2_vout (left CapSense); dac3_vout (right CapSense) |
| | 1 | |
| 2'h3 | CS_REFSEL_TREFSEL | dac2_vout (left CapSense); dac3_vout (right CapSense) |
| | 1_ALSO | |

1.3.368 CAPSL_CFG1

Capsense IO Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSL_CFG1: 0x40005871

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|---------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | io_ctrl | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|------------------------------------|
| 1:0 | io_ctrl[1:0] | Capsense Pull-up/Pull-down control |
| | | See Table 1-214. |

Table 1-214. Bit field encoding: CS_IO_CTRL

| Value | Name | Description |
|-------|--------------------|--|
| 2'h0 | CS_IO_CTRL_DEFAULT | Neither pull-up or pull-down (default) |
| 2'h1 | CS_IO_CTRL_PU | Capsense Pull-up mode |
| 2'h2 | CS_IO_CTRL_NONE | Neither pull-up or pull-down |
| 2'h3 | CS_IO_CTRL_PD | Capsense Pull-down mode |

1.3.369 CAPSR_CFG0

Capsense Reference Driver Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSR_CFG0: 0x40005872

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|---|---------|--------|---|-------|--------|
| SW Access:Reset | R/W:0 | NA:00 | | R/W:0 | R/W:00 | | R/W:0 | R/W:0 |
| HW Access | R | NA | | R | R | | R | R |
| Name | mxcmp | | | ch_cont | refsel | | boost | out_en |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 7 | mxcmp | Reference Buffer channel to comparator vp mux select See Table 1-217. |
| 4 | ch_cont | Reference Buffer Channel Selection Control See Table 1-216. |
| 3:2 | refsel[1:0] | Reference Selection See Table 1-219. |
| 1 | boost | High power mode See Table 1-215. |
| 0 | out_en | Reference Buffer Output enable See Table 1-218. |

Table 1-215. Bit field encoding: CS_BOOST_ENUM

| Value | Name | Description |
|-------|-----------------|---|
| 1'b0 | CS_BOOST_NORMAL | Normal Drive (typically 10-60pF) |
| 1'b1 | CS_BOOST_HIGH | High Drive (typical load = 0.1 to 20nF) |

Table 1-216. Bit field encoding: CS_CH_CONT_ENUM

| Value | Name | Description |
|-------|---------------|-------------------------|
| 1'b0 | CS_CH_CONT_VS | Ch2: Vssa path |
| 1'b1 | CS_CH_CONT_AG | Ch1: Analog Global Path |

Table 1-217. Bit field encoding: CS_MXCMP_ENUM

| Value | Name | Description |
|-------|-------------|---|
| 1'b0 | CS_MXCMP_AG | Analog Global path connected to comparator vp mux (ch1) |
| 1'b1 | CS_MXCMP_VS | Vssa path connected to comparator vp mux (ch2) |

Table 1-218. Bit field encoding: CS_OUT_EN_ENUM

| Value | Name | Description |
|-------|---------------|-------------|
| 1'b0 | CS_OUT_EN_HIZ | tristate |

1.3.369 CAPSR_CFG0 (continued)

Table 1-218. Bit field encoding: CS_OUT_EN_ENUM

| | | |
|------|--------------|-----------|
| 1'b1 | CS_OUT_EN_ON | connected |
|------|--------------|-----------|

Table 1-219. Bit field encoding: CS_REFSEL_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 2'h0 | CS_REFSEL_1P024 | 1.024 V Bandgap Reference |
| 2'h1 | CS_REFSEL_1P2 | 1.2 V Bandgap Reference |
| 2'h2 | CS_REFSEL_TREFSEL | dac2_vout (left CapSense); dac3_vout (right CapSense) |
| | 1 | |
| 2'h3 | CS_REFSEL_TREFSEL | dac2_vout (left CapSense); dac3_vout (right CapSense) |
| | 1_ALSO | |

1.3.370 CAPSR_CFG1

Capsense IO Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSR_CFG1: 0x40005873

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|---------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | io_ctrl | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|--|
| 1:0 | io_ctrl[1:0] | Capsense Pull-up/Pull-down control See Table 1-220. |

Table 1-220. Bit field encoding: CS_IO_CTRL

| Value | Name | Description |
|-------|--------------------|--|
| 2'h0 | CS_IO_CTRL_DEFAULT | Neither pull-up or pull-down (default) |
| 2'h1 | CS_IO_CTRL_PU | Capsense Pull-up mode |
| 2'h2 | CS_IO_CTRL_NONE | Neither pull-up or pull-down |
| 2'h3 | CS_IO_CTRL_PD | Capsense Pull-down mode |

1.3.371 PUMP_CR0

Pump Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PUMP_CR0: 0x40005876

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------------|----------------|---------------|------|----------------|---------------|--------------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | NA:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | R | R | R | NA | R | R | R |
| Name | | pump_amx_selclk | pump_amx_force | pump_amx_auto | | pump_ag_selclk | pump_ag_force | pump_ag_auto |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 6 | pump_amx_selclk | Analog Mux Bus Pump Clock Selection See Table 1-222. |
| 5 | pump_amx_force | force pumping - if block enabled enable pump regardless of voltage state |
| 4 | pump_amx_auto | enable autopumping - if block enabled pump when low voltage detected |
| 2 | pump_ag_selclk | Analog Global Pump Clock Selection See Table 1-221. |
| 1 | pump_ag_force | force pumping - if block enabled enable pump regardless of voltage state |
| 0 | pump_ag_auto | enable autopumping - if block enabled pump when low voltage detected |

Table 1-221. Bit field encoding: PUMP_AG_SELCLK_ENUM

| Value | Name | Description |
|-------|-------------------------|-------------------------------|
| 1'b0 | PUMP_AG_SELCLK_EXTERNAL | External (DSI) clock selected |
| 1'b1 | PUMP_AG_SELCLK_INTERNAL | Pump internal clock selected |

Table 1-222. Bit field encoding: PUMP_AMX_SELCLK_ENUM

| Value | Name | Description |
|-------|--------------------------|-------------------------------|
| 1'b0 | PUMP_AMX_SELCLK_EXTERNAL | External (DSI) clock selected |
| 1'b1 | PUMP_AMX_SELCLK_INTERNAL | Pump internal clock selected |

1.3.372 PUMP_CR1

Pump Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PUMP_CR1: 0x40005877

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------------|--------------------|-------------------|------------------|------|------------------|-----------------|----------------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | NA | R | R | R |
| Name | npump_sc_selclk | npump_opamp_selclk | npump_opamp_force | npump_opamp_auto | | npump_dsm_selclk | npump_dsm_force | npump_dsm_auto |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------------|--|
| 7 | npump_sc_selclk | Switched Cap Negative Pump Clock Selection See Table 1-225. |
| 6 | npump_opamp_selclk | Opamp Negative Pump Clock Selection See Table 1-224. |
| 5 | npump_opamp_force | force pumping - if block enabled enable pump regardless of voltage state |
| 4 | npump_opamp_auto | enable autopumping - if block enabled pump when low voltage detected |
| 2 | npump_dsm_selclk | DSM Negative Pump Clock Selection See Table 1-223. |
| 1 | npump_dsm_force | force pumping - if block enabled enable pump regardless of voltage state |
| 0 | npump_dsm_auto | enable autopumping - if block enabled pump when low voltage detected |

Table 1-223. Bit field encoding: NPUMP_DSM_SELCLK_ENUM

| Value | Name | Description |
|-------|---------------------------|---------------------------------------|
| 1'b0 | NPUMP_DSM_SELCLK_EXTERNAL | External (DSI) clock selected |
| 1'b1 | NPUMP_DSM_SELCLK_INTERNAL | Negative pump internal clock selected |

Table 1-224. Bit field encoding: NPUMP_OPAMP_SELCLK_ENUM

| Value | Name | Description |
|-------|-----------------------------|---------------------------------------|
| 1'b0 | NPUMP_OPAMP_SELCLK_EXTERNAL | External (DSI) clock selected |
| 1'b1 | NPUMP_OPAMP_SELCLK_INTERNAL | Negative pump internal clock selected |

Table 1-225. Bit field encoding: NPUMP_SC_SELCLK_ENUM

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.372 PUMP_CR1 (continued)

Table 1-225. Bit field encoding: NPUMP_SC_SELCLK_ENUM

| | |
|------|--|
| 1'b0 | NPUMP_SC_SELCLK_E External (DSI) clock selected XTERNAL |
| 1'b1 | NPUMP_SC_SELCLK_I Negative pump internal clock selected NTERNAL |

1.3.373 LPF0_CR0

Low Pass Filter Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF0_CR0: 0x40005878

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------|-------|------|-------|--------|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | NA:0 | R/W:0 | R/W:00 | |
| HW Access | NA | | R | R | NA | R | R | |
| Name | | | csel | rsel | | swout | swin | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|---|
| 5 | csel | Capacitance Selection See Table 1-226. |
| 4 | rsel | Resistance Selection See Table 1-227. |
| 2 | swout | Output Switch Control See Table 1-229. |
| 1:0 | swin[1:0] | Input Switch Control See Table 1-228. |

Table 1-226. Bit field encoding: LPF_CSEL_ENUM

| Value | Name | Description |
|-------|-------------|-------------|
| 1'b0 | LPF_CSEL_1X | 5pF |
| 1'b1 | LPF_CSEL_2X | 10pF |

Table 1-227. Bit field encoding: LPF_RSEL_ENUM

| Value | Name | Description |
|-------|-------------|--|
| 1'b0 | LPF_RSEL_1X | 1x; 7 units; $7 \times 29778.62\text{ohms} = 0.208\text{ MOhm}$ |
| 1'b1 | LPF_RSEL_5X | 5x; 35 units; $35 \times 29778.62\text{ohms} = 1.04\text{ MOhm}$ |

Table 1-228. Bit field encoding: LPF_SWIN_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 2'h0 | LPF_SWIN_NC | inputs not connected |
| 2'h1 | LPF_SWIN_AG0 | Analog Global 0 connected LPF0 (left): AGLO LPF1 (right): AGR0 |
| 2'h2 | LPF_SWIN_AMX | Analog Muxbus connected LPF0 (left): AMUXBUSL LPF1 (right): AMUXBUSR |
| 2'h3 | LPF_SWIN_BOTH | Both Analog Global and Analog Mux Bus connected (other end of the wire can be disconnected through the port control) |

1.3.373 LPF0_CR0 (continued)

Table 1-229. Bit field encoding: LPF_SWOUT_ENUM

| Value | Name | Description |
|-------|-----------------|---|
| 1'h0 | LPF_SWOUT_NC | LPF output not connected |
| 1'h1 | LPF_SWOUT_ABUS0 | LPF output connected to Analog local bus 0 LPF0 (left): ABUSL0 LPF1 (right): ABUSR0 |

1.3.374 LPF0_RSVD

LPF Reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF0_RSVD: 0x40005879

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|-------------|
| 7:0 | RSVD[7:0] | Reserved |

1.3.375 LPF1_CR0

Low Pass Filter Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF1_CR0: 0x4000587A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------|-------|------|-------|--------|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | NA:0 | R/W:0 | R/W:00 | |
| HW Access | NA | | R | R | NA | R | R | |
| Name | | | csel | rsel | | swout | swin | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|---|
| 5 | csel | Capacitance Selection See Table 1-230. |
| 4 | rsel | Resistance Selection See Table 1-231. |
| 2 | swout | Output Switch Control See Table 1-233. |
| 1:0 | swin[1:0] | Input Switch Control See Table 1-232. |

Table 1-230. Bit field encoding: LPF_CSEL_ENUM

| Value | Name | Description |
|-------|-------------|-------------|
| 1'b0 | LPF_CSEL_1X | 5pF |
| 1'b1 | LPF_CSEL_2X | 10pF |

Table 1-231. Bit field encoding: LPF_RSEL_ENUM

| Value | Name | Description |
|-------|-------------|---|
| 1'b0 | LPF_RSEL_1X | 1x; 7 units; 7*29778.62ohms = 0.208 MOhm |
| 1'b1 | LPF_RSEL_5X | 5x; 35 units; 35*29778.62ohms = 1.04 MOhm |

Table 1-232. Bit field encoding: LPF_SWIN_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 2'h0 | LPF_SWIN_NC | inputs not connected |
| 2'h1 | LPF_SWIN_AG0 | Analog Global 0 connected LPF0 (left): AGL0 LPF1 (right): AGR0 |
| 2'h2 | LPF_SWIN_AMX | Analog Muxbus connected LPF0 (left): AMUXBUSL LPF1 (right): AMUXBUSR |
| 2'h3 | LPF_SWIN_BOTH | Both Analog Global and Analog Mux Bus connected (other end of the wire can be disconnected through the port control) |

1.3.375 LPF1_CR0 (continued)

Table 1-233. Bit field encoding: LPF_SWOUT_ENUM

| Value | Name | Description |
|-------|-----------------|---|
| 1'h0 | LPF_SWOUT_NC | LPF output not connected |
| 1'h1 | LPF_SWOUT_ABUS0 | LPF output connected to Analog local bus 0 LPF0 (left): ABUSL0 LPF1 (right): ABUSR0 |

0x4000587b

1.3.376 LPF1_RSVD

LPF Reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF1_RSVD: 0x4000587B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|-------------|
| 7:0 | RSVD[7:0] | Reserved |

1.3.377 ANAIF_CFG_MISC_CR0

MISC Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ANAIF_CFG_MISC_CR0: 0x4000587C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|-------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | enpdb |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|---|
| 0 | enpdb | Analog Switch Enable Pull Down Bar (active low enable) - if enabled, all unused/opened analog routing switches will have their center nodes pulled down See Table 1-234. |

Table 1-234. Bit field encoding: ENPDB_ENUM

| Value | Name | Description |
|-------|---------------|--------------------------------|
| 1'b0 | ENPDB_ENABLE | Enable analog switch pulldown |
| 1'b1 | ENPDB_DISABLE | Disable analog switch pulldown |

1.3.378 DSM[0..0]_CR0

Delta Sigma Modulator Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR0: 0x40005880

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|--------|---|--------|---|
| SW Access:Reset | NA:0000 | | | | R/W:00 | | R/W:00 | |
| HW Access | NA | | | | R | | R | |
| Name | | | | | nonov | | qlev | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 3:2 | nonov[1:0] | Non overlap delay of clock phases See Table 1-235. |
| 1:0 | qlev[1:0] | Quantization Level choice for modulator See Table 1-236. |

Table 1-235. Bit field encoding: NONOV_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------|
| 2'h0 | NONOV_LOW | low (1.57ns, typ) |
| 2'h1 | NONOV_MEDIUM | medium (3.54ns, typ) |
| 2'h2 | NONOV_HIGH | high (6.47ns, typ) |
| 2'h3 | NONOV_VERYHIGH | very high (9.91ns, typ) |

Table 1-236. Bit field encoding: QLEV_ENUM

| Value | Name | Description |
|-------|-------------|----------------------|
| 2'b00 | QLEV_2 | 2 level quantization |
| 2'b01 | QLEV_3 | 3 level quantization |
| 2'b10 | QLEV_9 | 9 level quantization |
| 2'b11 | QLEV_9_ALSO | 9 level quantization |

1.3.379 DSM[0..0]_CR1

Delta Sigma Modulator Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR1: 0x40005881

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------|-------|-----------|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:00000 | | | | |
| HW Access | NA | R | R | R | | | | |
| Name | | dpmode | oden | odet_th | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|---|
| 6 | dpmode | Datapath mode See Table 1-237. |
| 5 | oden | Overload detect scheme enable |
| 4:0 | odet_th[4:0] | Overload detection threshold. If the number of continuous 1s or 0s coming out of quantizer exceeds this number overload detection flag is set |

Table 1-237. Bit field encoding: DPMODE_ENUM

| Value | Name | Description |
|-------|------------------|-------------|
| 1'h0 | DPMODE_NORMAL | normal |
| 1'h1 | DPMODE_LOWOFFSET | low offset |

1.3.380 DSM[0..0]_CR2

Delta Sigma Modulator Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR2: 0x40005882

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|-----------|-----------|-----------|-------------|---------|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | R | R | R | R | R | R | | |
| Name | mx_reset | reset3_en | reset2_en | reset1_en | mod_chop_en | fchop | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 7 | mx_reset | select DSM reset source See Table 1-239. |
| 6 | reset3_en | allow third stage integrating capacitance to be reset See Table 1-242. |
| 5 | reset2_en | allow second stage integrating capacitance to be reset See Table 1-241. |
| 4 | reset1_en | Allow first stage integrating capacitance to be reset See Table 1-240. |
| 3 | mod_chop_en | Enable Modulator Chopping |
| 2:0 | fchop[2:0] | Chopping Frequency Selection. The Fclock is simply frequency clock See Table 1-238. |

Table 1-238. Bit field encoding: FCHOP_ENUM

| Value | Name | Description |
|-------|--------------|-------------|
| 3'h0 | FCHOP_DIV2 | Fclock/2 |
| 3'h1 | FCHOP_DIV4 | Fclock/4 |
| 3'h2 | FCHOP_DIV8 | Fclock/8 |
| 3'h3 | FCHOP_DIV16 | Fclock/16 |
| 3'h4 | FCHOP_DIV32 | Fclock/32 |
| 3'h5 | FCHOP_DIV64 | Fclock/64 |
| 3'h6 | FCHOP_DIV128 | Fclock/128 |
| 3'h7 | FCHOP_DIV256 | Fclock/256 |

Table 1-239. Bit field encoding: MXSELRESET_ENUM

| Value | Name | Description |
|-------|--------------|-----------------------------------|
| 1'b0 | MXSELRESET_0 | Select Decimator for reset source |
| 1'b1 | MXSELRESET_1 | Select UDB for reset source |

1.3.380 DSM[0..0]_CR2 (continued)

Table 1-240. Bit field encoding: RESET1_EN_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 1'b0 | RESET1_EN_DISABLE | First stage integrating capacitance cannot be reset (use when in overload, to allow for first order operation) |
| 1'b1 | RESET1_EN_ENABLE | First stage integrating capacitance can be reset |

Table 1-241. Bit field encoding: RESET2_EN_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 1'b0 | RESET2_EN_DISABLE | second stage integrating capacitance cannot be reset (use when in overload, to allow for second order operation, assuming the reset1_en bit is also cleared) |
| 1'b1 | RESET2_EN_ENABLE | second stage integrating capacitance can be reset |

Table 1-242. Bit field encoding: RESET3_EN_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 1'b0 | RESET3_EN_DISABLE | third stage integrating capacitance cannot be reset (use only for debug purposes) |
| 1'b1 | RESET3_EN_ENABLE | third stage integrating capacitance can be reset |

1.3.381 DSM[0..0]_CR3

Delta Sigma Modulator Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR3: 0x40005883

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|------|---------|-------------|-------------|---|---|---|
| SW Access:Reset | R/W:0 | NA:0 | R/W:0 | R/W:0 | R/W:0000 | | | |
| HW Access | R | NA | R | R | R | | | |
| Name | sign | | mx_dout | modbitin_en | mx_modbitin | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------------|--|
| 7 | sign | Invert sign of input See Table 1-246. |
| 5 | mx_dout | Select DSM dout routed to UDB See Table 1-244. |
| 4 | modbitin_en | modbitin enable See Table 1-243. |
| 3:0 | mx_modbitin[3:0] | Select modbitin input Reserved inputs are tied to 0 See Table 1-245. |

Table 1-243. Bit field encoding: MODBITIN_EN_ENUM

| Value | Name | Description |
|-------|--------------------|--|
| 1'b0 | MODBITIN_EN_DISABL | Do not allow modbit input to be mixed with modulator input |
| 1'b1 | MODBITIN_EN_ENABL | Allow modbit input to be mixed with modulator input |

Table 1-244. Bit field encoding: MX_DOUT_ENUM

| Value | Name | Description |
|-------|----------------|--|
| 1'b0 | MX_DOUT_8BIT | Select reg OUT0=dout[7:0] (synced; w/o post processing) |
| 1'b1 | MX_DOUT_2SCOMP | Select reg OUT1={2'b0,ovdcause,ovdflag,dout2scomp} (synced; overload cause, overload flag, dout 2s complement) |

Table 1-245. Bit field encoding: MX_MODBITIN_ENUM

| Value | Name | Description |
|-------|------------------|-------------|
| 4'h0 | MX_MODBITIN_LUT0 | lut0_out |
| 4'h1 | MX_MODBITIN_LUT1 | lut1_out |
| 4'h2 | MX_MODBITIN_LUT2 | lut2_out |
| 4'h3 | MX_MODBITIN_LUT3 | lut3_out |

1.3.381 DSM[0..0]_CR3 (continued)

Table 1-245. Bit field encoding: MX_MODBITIN_ENUM

| | | |
|------|--------------------|--|
| 4'h4 | MX_MODBITIN_LUT4 | lut4_out (doesn't exist on Leopard, tied to 0) |
| 4'h5 | MX_MODBITIN_LUT5 | lut5_out (doesn't exist on Leopard, tied to 0) |
| 4'h6 | MX_MODBITIN_LUT6 | lut6_out (doesn't exist on Leopard, tied to 0) |
| 4'h7 | MX_MODBITIN_LUT7 | lut7_out (doesn't exist on Leopard, tied to 0) |
| 4'h8 | MX_MODBITIN_UDB | UDB |
| 4'h9 | MX_MODBITIN_CONST | constant 1 |
| | | 1 |
| 4'ha | MX_MODBITIN_CONST | constant 0 |
| | | 0 |
| 4'hb | MX_MODBITIN_0xB_RS | Reserved |
| | | VD |
| 4'hc | MX_MODBITIN_0xC_R | Reserved |
| | | SVD |
| 4'hd | MX_MODBITIN_0xD_R | Reserved |
| | | SVD |
| 4'he | MX_MODBITIN_0xE_RS | Reserved |
| | | VD |
| 4'hf | MX_MODBITIN_0xF_RS | Reserved |
| | | VD |

Table 1-246. Bit field encoding: SIGN_ENUM

| Value | Name | Description |
|-------|----------------|---|
| 1'b0 | SIGN_NONINVERT | keep original polarity for the input |
| 1'b1 | SIGN_INVERT | Invert sign of input (use when trying to chop once and then average the offset value out) |

1.3.382 DSM[0..0]_CR4

Delta Sigma Modulator Control Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR4: 0x40005884

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|-------------|---|---|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0000000 | | | | | | |
| HW Access | R | R | | | | | | |
| Name | fcap1_en | fcap1 | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 7 | fcap1_en | Enable/Disable Capacitance path meant for DFT (Design for Testability) of the first integrator's integrating capacitance path See Table 1-248. |
| 6:0 | fcap1[6:0] | binary weighted first stage integrating capacitance See Table 1-247. |

Table 1-247. Bit field encoding: FCAP1_ENUM

| Value | Name | Description |
|------------|------------|-------------------------|
| 7'b0 | FCAP1_MIN | 0 fF |
| 7'b1111111 | FCAP1_MAX | Max Value = 12.7 pF |
| 7'b0000001 | FCAP1_BIT0 | fcap[0] set -> +100 fF |
| 7'b0000010 | FCAP1_BIT1 | fcap[1] set -> +200 fF |
| 7'b0000100 | FCAP1_BIT2 | fcap[2] set -> +400 fF |
| 7'b0001000 | FCAP1_BIT3 | fcap[3] set -> +800 fF |
| 7'b0010000 | FCAP1_BIT4 | fcap[4] set -> +1600 fF |
| 7'b0100000 | FCAP1_BIT5 | fcap[5] set -> +3200 fF |
| 7'b1000000 | FCAP1_BIT6 | fcap[6] set -> +6400 fF |

Table 1-248. Bit field encoding: FCAP1_EN_ENUM

| Value | Name | Description |
|-------|------------------|--|
| 1'h0 | FCAP1_EN_DISABLE | Disable the DFT 100fF capacitance path |
| 1'h1 | FCAP1_EN_ENABLE | Enable the DFT 100fF capacitance path |

1.3.383 DSM[0..0]_CR5

Delta Sigma Modulator Control Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR5: 0x40005885

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|-------------|---|---|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0000000 | | | | | | |
| HW Access | R | R | | | | | | |
| Name | ipcap1_en | ipcap1 | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 7 | ipcap1_en | Enable/Disable Capacitance path meant for DFT (Design for Testability) of the first integrator's input sampling path See Table 1-250. |
| 6:0 | ipcap1[6:0] | Binary weighted first stage integrating capacitance See Table 1-249. |

Table 1-249. Bit field encoding: IPCAP1_ENUM

| Value | Name | Description |
|------------|-------------|---------------------------|
| 7'b0 | IPCAP1_MIN | 0 fF |
| 7'b1111111 | IPCAP1_MAX | Max Value = 12.7 pF |
| 7'b0000001 | IPCAP1_BIT0 | ipcap1[0] set -> +100 fF |
| 7'b0000010 | IPCAP1_BIT1 | ipcap1[1] set -> +200 fF |
| 7'b0000100 | IPCAP1_BIT2 | ipcap1[2] set -> +400 fF |
| 7'b0001000 | IPCAP1_BIT3 | ipcap1[3] set -> +800 fF |
| 7'b0010000 | IPCAP1_BIT4 | ipcap1[4] set -> +1600 fF |
| 7'b0100000 | IPCAP1_BIT5 | ipcap1[5] set -> +3200 fF |
| 7'b1000000 | IPCAP1_BIT6 | ipcap1[6] set -> +6400 fF |

Table 1-250. Bit field encoding: IPCAP1_EN_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 1'h0 | IPCAP1_EN_DISABLE | Disable the DFT 100fF capacitance path |
| 1'h1 | IPCAP1_EN_ENABLE | Enable the DFT 100fF capacitance path |

1.3.384 DSM[0..0]_CR6

Delta Sigma Modulator Control Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR6: 0x40005886

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------|------------|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0 | R/W:000000 | | | | | |
| HW Access | NA | R | R | | | | | |
| Name | | daccap_en | daccap | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|---|
| 6 | daccap_en | Enable/Disable Capacitance path meant for DFT (Design for Testability) of the DAC Reference sampling path See Table 1-252. |
| 5:0 | daccap[5:0] | Binary weighted first stage DAC capacitance See Table 1-251. |

Table 1-251. Bit field encoding: DACCAP_ENUM

| Value | Name | Description |
|-----------|-------------|--------------------------------------|
| 6'b000001 | DACCAP_BIT0 | daccap[0] set -> add 12*8= +96 fF |
| 6'b000010 | DACCAP_BIT1 | daccap[1] set -> add 24*8= +192 fF |
| 6'b000100 | DACCAP_BIT2 | daccap[2] set -> add 50*8= +400 fF |
| 6'b001000 | DACCAP_BIT3 | daccap[3] set -> add 100*8= +800 fF |
| 6'b010000 | DACCAP_BIT4 | daccap[4] set -> add 200*8= +1600 fF |
| 6'b100000 | DACCAP_BIT5 | daccap[5] set -> add 400*8= +3200 fF |

Table 1-252. Bit field encoding: DACCAP_EN_ENUM

| Value | Name | Description |
|-------|-------------------|---------------------------------------|
| 1'h0 | DACCAP_EN_DISABLE | Disable the DFT 12fF capacitance path |
| 1'h1 | DACCAP_EN_ENABLE | Enable the DFT 12fF capacitance path |

1.3.385 DSM[0..0]_CR7

Delta Sigma Modulator Control Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR7: 0x40005887

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|----------|--------------|-------------|-----------|---------|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | R | R | R | R | R | R | | |
| Name | fcap2_en | fcap3_en | ipcap1offset | fcap1offset | rescap_en | rescap | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|---|
| 7 | fcap2_en | Enable/Disable additional 50fF capacitance path in the second integrators integrating capacitance path See Table 1-254. |
| 6 | fcap3_en | Enable/Disable additional capacitance path in the third integrator's integrating capacitance path See Table 1-255. |
| 5 | ipcap1offset | Offset capacitance for the input sampling capacitance in the first stage integrator See Table 1-256. |
| 4 | fcap1offset | Offset Capacitance for the integrating capacitance in the first stage integrator See Table 1-253. |
| 3 | rescap_en | Reserved The resonator loop feature has been disabled in the design; programming these bits does not produce any change in the ADC outcome |
| 2:0 | rescap[2:0] | Reserved The resonator loop feature has been disabled in the design; programming these bits does not produce any change in the ADC outcome |

Table 1-253. Bit field encoding: FCAP1OFFSET_ENUM

| Value | Name | Description |
|-------|---------------|----------------------------------|
| 1'b0 | FCAP1OFFSET_0 | Don't add offset capacitance |
| 1'b1 | FCAP1OFFSET_1 | Add offset capacitance of 3.4 pF |

Table 1-254. Bit field encoding: FCAP2_EN_ENUM

| Value | Name | Description |
|-------|------------------|--|
| 1'h0 | FCAP2_EN_DISABLE | Disable the additional 50fF capacitance path |
| 1'h1 | FCAP2_EN_ENABLE | Enable the additional 50fF capacitance path |

1.3.385 DSM[0..0]_CR7 (continued)

Table 1-255. Bit field encoding: FCAP3_EN_ENUM

| Value | Name | Description |
|-------|------------------|---|
| 1'h0 | FCAP3_EN_DISABLE | Disable the additional 100fF capacitance path |
| 1'h1 | FCAP3_EN_ENABLE | Enable the 100fF capacitance path |

Table 1-256. Bit field encoding: IPCAP1OFFSET_ENUM

| Value | Name | Description |
|-------|----------------|----------------------------------|
| 1'b0 | IPCAP1OFFSET_0 | Don't add offset capacitance |
| 1'b1 | IPCAP1OFFSET_1 | Add offset capacitance of 4.8 pF |

1.3.386 DSM[0..0]_CR8

Delta Sigma Modulator Control Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR8: 0x40005888

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---------|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0 | R/W:000 | | | R/W:0000 | | | |
| HW Access | R | R | | | R | | | |
| Name | ipcap2_en | ipcap2 | | | fcap2 | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 7 | ipcap2_en | Enable/Disable additional 50fF capacitance path in the second integrator's input sampling path See Table 1-259. |
| 6:4 | ipcap2[2:0] | The second integrator's input sampling capacitance (0-350fF, 50fF step) See Table 1-258. |
| 3:0 | fcap2[3:0] | The second stage integrating capacitance (0-750fF, 50fF step) See Table 1-257. |

Table 1-257. Bit field encoding: FCAP2_ENUM

| Value | Name | Description |
|-------|-----------------|-------------|
| 4'h0 | FCAP2_0FEMPTO | 0fF |
| 4'h1 | FCAP2_50FEMPTO | 50fF |
| 4'h2 | FCAP2_100FEMPTO | 100fF |
| 4'h3 | FCAP2_150FEMPTO | 150fF |
| 4'h4 | FCAP2_200FEMPTO | 200fF |
| 4'h5 | FCAP2_250FEMPTO | 250fF |
| 4'h6 | FCAP2_300FEMPTO | 300fF |
| 4'h7 | FCAP2_350FEMPTO | 350fF |
| 4'h8 | FCAP2_400FEMPTO | 400fF |
| 4'h9 | FCAP2_450FEMPTO | 450fF |
| 4'ha | FCAP2_500FEMPTO | 500fF |
| 4'hb | FCAP2_550FEMPTO | 550fF |
| 4'hc | FCAP2_600FEMPTO | 600fF |
| 4'hd | FCAP2_650FEMPTO | 650fF |
| 4'he | FCAP2_700FEMPTO | 700fF |
| 4'hf | FCAP2_750FEMPTO | 750fF |

Table 1-258. Bit field encoding: IPCAP2_ENUM

| Value | Name | Description |
|-------|------------------|-------------|
| 3'h0 | IPCAP2_0FEMPTO | 0fF |
| 3'h1 | IPCAP2_50FEMPTO | 50fF |
| 3'h2 | IPCAP2_100FEMPTO | 100fF |
| 3'h3 | IPCAP2_150FEMPTO | 150fF |

1.3.386 DSM[0..0]_CR8 (continued)

Table 1-258. Bit field encoding: IPCAP2_ENUM

| | | |
|------|------------------|-------|
| 3'h4 | IPCAP2_200FEMPTO | 200fF |
| 3'h5 | IPCAP2_250FEMPTO | 250fF |
| 3'h6 | IPCAP2_300FEMPTO | 300fF |
| 3'h7 | IPCAP2_350FEMPTO | 350fF |

Table 1-259. Bit field encoding: IPCAP2_EN_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 1'h0 | IPCAP2_EN_DISABLE | Disable the additional 50fF capacitance path |
| 1'h1 | IPCAP2_EN_ENABLE | Enable the additional 50fF capacitance path |

1.3.387 DSM[0..0]_CR9

Delta Sigma Modulator Control Register 9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR9: 0x40005889

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---------|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0 | R/W:000 | | | R/W:0000 | | | |
| HW Access | R | R | | | R | | | |
| Name | ipcap3_en | ipcap3 | | | fcap3 | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|---|
| 7 | ipcap3_en | Enable/Disable additional 50fF capacitance path in the third integrator's input sampling path See Table 1-262. |
| 6:4 | ipcap3[2:0] | The third integrator's input sampling capacitance (0-350fF in 50fF step) See Table 1-261. |
| 3:0 | fcap3[3:0] | The third stage integrating capacitance (0-750fF, 50fF step) See Table 1-260. |

Table 1-260. Bit field encoding: FCAP3_ENUM

| Value | Name | Description |
|-------|------------------|-------------|
| 4'h0 | FCAP3_0FEMPTO | 0fF |
| 4'h1 | FCAP3_100FEMPTO | 100fF |
| 4'h2 | FCAP3_200FEMPTO | 200fF |
| 4'h3 | FCAP3_300FEMPTO | 300fF |
| 4'h4 | FCAP3_400FEMPTO | 400fF |
| 4'h5 | FCAP3_500FEMPTO | 500fF |
| 4'h6 | FCAP3_600FEMPTO | 600fF |
| 4'h7 | FCAP3_700FEMPTO | 700fF |
| 4'h8 | FCAP3_800FEMPTO | 800fF |
| 4'h9 | FCAP3_900FEMPTO | 900fF |
| 4'ha | FCAP3_1000FEMPTO | 1000fF |
| 4'hb | FCAP3_1100FEMPTO | 1100fF |
| 4'hc | FCAP3_1200FEMPTO | 1200fF |
| 4'hd | FCAP3_1300FEMPTO | 1300fF |
| 4'he | FCAP3_1400FEMPTO | 1400fF |
| 4'hf | FCAP3_1500FEMPTO | 1500fF |

Table 1-261. Bit field encoding: IPCAP3_ENUM

| Value | Name | Description |
|-------|------------------|-------------|
| 3'h0 | IPCAP3_0FEMPTO | 0fF |
| 3'h1 | IPCAP3_50FEMPTO | 50fF |
| 3'h2 | IPCAP3_100FEMPTO | 100fF |
| 3'h3 | IPCAP3_150FEMPTO | 150fF |

1.3.387 DSM[0..0]_CR9 (continued)

Table 1-261. Bit field encoding: IPCAP3_ENUM

| | | |
|------|------------------|-------|
| 3'h4 | IPCAP3_200FEMPTO | 200fF |
| 3'h5 | IPCAP3_250FEMPTO | 250fF |
| 3'h6 | IPCAP3_300FEMPTO | 300fF |
| 3'h7 | IPCAP3_350FEMPTO | 350fF |

Table 1-262. Bit field encoding: IPCAP3_EN_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 1'h0 | IPCAP3_EN_DISABLE | Disable the additional 50fF capacitance path |
| 1'h1 | IPCAP3_EN_ENABLE | Enable the additional 50fF capacitance path |

1.3.388 DSM[0..0]_CR10

Delta Sigma Modulator Control Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR10: 0x4000588A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---------|---|---|------------|---------|---|---|
| SW Access:Reset | R/W:0 | R/W:000 | | | R/W:0 | R/W:000 | | |
| HW Access | R | R | | | R | R | | |
| Name | sumcap1_en | sumcap1 | | | sumcap2_en | sumcap2 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|---|
| 7 | sumcap1_en | Enabling/Disabling the the additional 50fF capacitance path that lies between first integrator output and summer input (feed-forward) path See Table 1-264. |
| 6:4 | sumcap1[2:0] | The summer capacitance that lies on the feed-forward path from the first integrator output (0fF to 350fF in 50fF step) See Table 1-263. |
| 3 | sumcap2_en | Enabling/Disabling the additional 50fF capacitance path that lies between the second integrator output and summer input (feed-forward) path See Table 1-266. |
| 2:0 | sumcap2[2:0] | The summer capacitance that lies on the feed-forward path from the second integrator output (0fF to 350fF in 50fF step) See Table 1-265. |

Table 1-263. Bit field encoding: SUMCAP1_ENUM

| Value | Name | Description |
|-------|-------------------|-------------|
| 3'h0 | SUMCAP1_0FEMPTO | 0fF |
| 3'h1 | SUMCAP1_50FEMPTO | 50fF |
| 3'h2 | SUMCAP1_100FEMPTO | 100fF |
| 3'h3 | SUMCAP1_150FEMPTO | 150fF |
| 3'h4 | SUMCAP1_200FEMPTO | 200fF |
| 3'h5 | SUMCAP1_250FEMPTO | 250fF |
| 3'h6 | SUMCAP1_300FEMPTO | 300fF |
| 3'h7 | SUMCAP1_350FEMPTO | 350fF |

1.3.388 DSM[0..0]_CR10 (continued)

Table 1-264. Bit field encoding: SUMCAP1_EN_ENUM

| Value | Name | Description |
|-------|------------------------|--|
| 1'h0 | SUMCAP1_EN_DISABL E | Disable the additional 50fF capacitance path |
| 1'h1 | SUMCAP1_EN_ENABL E | Enable the additional 50fF capacitance path |

Table 1-265. Bit field encoding: SUMCAP2_ENUM

| Value | Name | Description |
|-------|-----------------------|-------------|
| 3'h0 | SUMCAP2_0FEMPTO | 0fF |
| 3'h1 | SUMCAP2_50FEMPTO | 50fF |
| 3'h2 | SUMCAP2_100FEMPT O | 100fF |
| 3'h3 | SUMCAP2_150FEMPT O | 150fF |
| 3'h4 | SUMCAP2_200FEMPT O | 200fF |
| 3'h5 | SUMCAP2_250FEMPT O | 250fF |
| 3'h6 | SUMCAP2_300FEMPT O | 300fF |
| 3'h7 | SUMCAP2_350FEMPT O | 350fF |

Table 1-266. Bit field encoding: SUMCAP2_EN_ENUM

| Value | Name | Description |
|-------|------------------------|--|
| 1'h0 | SUMCAP2_EN_DISABL E | Disable the additional 50fF capacitance path |
| 1'h1 | SUMCAP2_EN_ENABL E | Enable the additional 50fF capacitance path |

1.3.389 DSM[0..0]_CR11

Delta Sigma Modulator Control Register 11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR11: 0x4000588B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---------|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0 | R/W:000 | | | R/W:0000 | | | |
| HW Access | R | R | | | R | | | |
| Name | sumcap3_en | sumcap3 | | | sumcapfb | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------------|--|
| 7 | sumcap3_en | Enabling/Disabling the additional 50fF path that lies between the third integrator output and summer input (feed-forward) path See Table 1-268. |
| 6:4 | sumcap3[2:0] | The summer capacitance that lies on the feed-forward path from the third integrator output (0fF to 350fF in 50fF step) See Table 1-267. |
| 3:0 | sumcapfb[3:0] | The summer feedback capacitance (0fF to 750F in 50fF step) See Table 1-269. |

Table 1-267. Bit field encoding: SUMCAP3_ENUM

| Value | Name | Description |
|-------|------------------|-------------|
| 3'h0 | SUMCAP3_0FEMPTO | 0fF |
| 3'h1 | SUMCAP3_50FEMPTO | 50fF |
| 3'h2 | SUMCAP3_100FEMPT | 100fF |
| | O | |
| 3'h3 | SUMCAP3_150FEMPT | 150fF |
| | O | |
| 3'h4 | SUMCAP3_200FEMPT | 200fF |
| | O | |
| 3'h5 | SUMCAP3_250FEMPT | 250fF |
| | O | |
| 3'h6 | SUMCAP3_300FEMPT | 300fF |
| | O | |
| 3'h7 | SUMCAP3_350FEMPT | 350fF |
| | O | |

Table 1-268. Bit field encoding: SUMCAP3_EN_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 1'h0 | SUMCAP3_EN_DISABL | Disable the additional 50fF capacitance path |
| | E | |

1.3.389 DSM[0..0]_CR11 (continued)

Table 1-268. Bit field encoding: SUMCAP3_EN_ENUM

| | | |
|------|------------------|---|
| 1'h1 | SUMCAP3_EN_ENABL | Enable the additional 50fF capacitance path |
| | E | |

Table 1-269. Bit field encoding: SUMCAPFB_ENUM

| Value | Name | Description |
|-------|-------------------|-------------|
| 4'h0 | SUMCAPFB_0FEMPTO | 0fF |
| 4'h1 | SUMCAPFB_50FEMPT | 50fF |
| | O | |
| 4'h2 | SUMCAPFB_100FEMPT | 100fF |
| | O | |
| 4'h3 | SUMCAPFB_150FEMPT | 150fF |
| | O | |
| 4'h4 | SUMCAPFB_200FEMPT | 200fF |
| | O | |
| 4'h5 | SUMCAPFB_250FEMPT | 250fF |
| | O | |
| 4'h6 | SUMCAPFB_300FEMPT | 300fF |
| | O | |
| 4'h7 | SUMCAPFB_350FEMPT | 350fF |
| | O | |
| 4'h8 | SUMCAPFB_400FEMPT | 400fF |
| | O | |
| 4'h9 | SUMCAPFB_450FEMPT | 450fF |
| | O | |
| 4'ha | SUMCAPFB_500FEMPT | 500fF |
| | O | |
| 4'hb | SUMCAPFB_550FEMPT | 550fF |
| | O | |
| 4'hc | SUMCAPFB_600FEMPT | 600fF |
| | O | |
| 4'hd | SUMCAPFB_650FEMPT | 650fF |
| | O | |
| 4'he | SUMCAPFB_700FEMPT | 700fF |
| | O | |
| 4'hf | SUMCAPFB_750FEMPT | 750fF |
| | O | |

1.3.390 DSM[0..0]_CR12

Delta Sigma Modulator Control Register 12

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR12: 0x4000588C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|-------------|-----------|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:00000 | | | | |
| HW Access | NA | R | R | R | | | | |
| Name | | sumcapfb_en | sumcapin_en | sumcapin | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------------|--|
| 6 | sumcapfb_en | Enabling/Disabling the DFT path that lies on the feedback path of the active summer See Table 1-270. |
| 5 | sumcapin_en | Enabling/Disabling the DFT path that lies between input of the sigma delta modulator and the summer input. See Table 1-272. |
| 4:0 | sumcapin[4:0] | The summer capacitance that lies on the path where the input signal is summed (50fF to 1.6pF in 50fF step) See Table 1-271. |

Table 1-270. Bit field encoding: SUMCAPFB_EN_ENUM

| Value | Name | Description |
|-------|-------------------|---------------------------------------|
| 1'h0 | SUMCAPFB_EN_DISAB | Disable the DFT 50fF capacitance path |
| | LE | |
| 1'h1 | SUMCAPFB_EN_ENAB | Enable the DFT 50fF capacitance path |
| | LE | |

Table 1-271. Bit field encoding: SUMCAPIN_ENUM

| Value | Name | Description |
|-------|--------------------|-------------|
| 5'h00 | SUMCAPIN_0FEMPTO | 0fF |
| 5'h01 | SUMCAPIN_50FEMPTO | 50fF |
| 5'h02 | SUMCAPIN_100FEMPTO | 100fF |
| | O | |
| 5'h03 | SUMCAPIN_150FEMPTO | 150fF |
| | O | |
| 5'h04 | SUMCAPIN_200FEMPTO | 200fF |
| | O | |
| 5'h05 | SUMCAPIN_250FEMPTO | 250fF |
| | O | |
| 5'h06 | SUMCAPIN_300FEMPTO | 300fF |
| | O | |

1.3.390 DSM[0..0]_CR12 (continued)

Table 1-271. Bit field encoding: SUMCAPIN_ENUM

| | | |
|-------|-------------------|--------|
| 5'h07 | SUMCAPIN_350FEMPT | 350fF |
| | O | |
| 5'h08 | SUMCAPIN_400FEMPT | 400fF |
| | O | |
| 5'h09 | SUMCAPIN_450FEMPT | 450fF |
| | O | |
| 5'h0a | SUMCAPIN_500FEMPT | 500fF |
| | O | |
| 5'h0b | SUMCAPIN_550FEMPT | 550fF |
| | O | |
| 5'h0c | SUMCAPIN_600FEMPT | 600fF |
| | O | |
| 5'h0d | SUMCAPIN_650FEMPT | 650fF |
| | O | |
| 5'h0e | SUMCAPIN_700FEMPT | 700fF |
| | O | |
| 5'h0f | SUMCAPIN_750FEMPT | 750fF |
| | O | |
| 5'h10 | SUMCAPIN_800FEMPT | 800fF |
| | O | |
| 5'h11 | SUMCAPIN_850FEMPT | 850fF |
| | O | |
| 5'h12 | SUMCAPIN_900FEMPT | 900fF |
| | O | |
| 5'h13 | SUMCAPIN_950FEMPT | 950fF |
| | O | |
| 5'h14 | SUMCAPIN_1000FEMP | 1000fF |
| | TO | |
| 5'h15 | SUMCAPIN_1050FEMP | 1050fF |
| | TO | |
| 5'h16 | SUMCAPIN_1100FEMP | 1100fF |
| | TO | |
| 5'h17 | SUMCAPIN_1150FEMP | 1150fF |
| | TO | |
| 5'h18 | SUMCAPIN_1200FEMP | 1200fF |
| | TO | |
| 5'h19 | SUMCAPIN_1250FEMP | 1250fF |
| | TO | |
| 5'h1a | SUMCAPIN_1300FEMP | 1300fF |
| | TO | |
| 5'h1b | SUMCAPIN_1350FEMP | 1350fF |
| | TO | |
| 5'h1c | SUMCAPIN_1400FEMP | 1400fF |
| | TO | |
| 5'h1d | SUMCAPIN_1450FEMP | 1450fF |
| | TO | |
| 5'h1e | SUMCAPIN_1500FEMP | 1500fF |
| | TO | |
| 5'h1f | SUMCAPIN_1550FEMP | 1550fF |
| | TO | |

Table 1-272. Bit field encoding: SUMCAPIN_EN_ENUM

| Value | Name | Description |
|-------|-------------------------|---------------------------------------|
| 1'h0 | SUMCAPIN_EN_DISAB LE | Disable the DFT 50fF capacitance path |
| 1'h1 | SUMCAPIN_EN_ENABL E | Enable the DFT 50fF capacitance path |

1.3.391 DSM[0..0]_CR13

Delta Sigma Modulator Control Register 13

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR13: 0x4000588D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|--------------------------------|
| 7:0 | RSVD[7:0] | Reserved |
| | | Reserved for refsels expansion |

1.3.392 DSM[0..0]_CR14

Delta Sigma Modulator Control Register 14

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR14: 0x4000588E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|------|---------|---|---|
| SW Access:Reset | R/W:0000 | | | | NA:0 | R/W:000 | | |
| HW Access | R | | | | NA | R | | |
| Name | opamp1_bw | | | | | power1 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------------|---|
| 7:4 | opamp1_bw[3:0] | First Stage Opamp Bandwidth Control (Risk Mitigation not for User control). Table gives value for Modulator input bw[3:0] See Table 1-273. |
| 2:0 | power1[2:0] | First Stage Opamp Power level control See Table 1-274. |

Table 1-273. Bit field encoding: OPAMP1_BW_ENUM

| Value | Name | Description |
|-------|---------------|--------------------------|
| 4'h0 | OPAMP1_BW_0x0 | (default) |
| 4'h1 | OPAMP1_BW_0x1 | (used with 1.5X power) |
| 4'h2 | OPAMP1_BW_0x2 | reserved |
| 4'h3 | OPAMP1_BW_0x3 | (used with 2X power) |
| 4'h4 | OPAMP1_BW_0x4 | reserved |
| 4'h5 | OPAMP1_BW_0x5 | reserved |
| 4'h6 | OPAMP1_BW_0x6 | reserved |
| 4'h7 | OPAMP1_BW_0x7 | (used with 2.5X power) |
| 4'h8 | OPAMP1_BW_0x8 | (higher BW, 1.25X power) |
| 4'h9 | OPAMP1_BW_0x9 | (lower noise) |
| 4'ha | OPAMP1_BW_0xA | reserved |
| 4'hb | OPAMP1_BW_0xB | reserved |
| 4'hc | OPAMP1_BW_0xC | reserved |
| 4'hd | OPAMP1_BW_0xD | reserved |
| 4'he | OPAMP1_BW_0xE | reserved |
| 4'hf | OPAMP1_BW_0xF | reserved |

Table 1-274. Bit field encoding: POWER1_ENUM

| Value | Name | Description |
|-------|----------|---------------------|
| 3'h0 | POWER1_0 | Low (44uA) |
| 3'h1 | POWER1_1 | Medium (123uA) |
| 3'h2 | POWER1_2 | High (492uA) |
| 3'h3 | POWER1_3 | 1.5X (750uA) |
| 3'h4 | POWER1_4 | 2X (1mA) |
| 3'h5 | POWER1_5 | C/2 @ 3MSPS (277uA) |

1.3.392 DSM[0..0]_CR14 (continued)

Table 1-274. Bit field encoding: POWER1_ENUM

| | | |
|------|----------|---------------------|
| 3'h6 | POWER1_6 | C/4 @ 3MSPS (185uA) |
| 3'h7 | POWER1_7 | 2.5X (1.5mA) |

1.3.393 DSM[0..0]_CR15

Delta Sigma Modulator Control Register 15

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR15: 0x4000588F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|------|----------|---|---|
| SW Access:Reset | NA:00 | | R/W:00 | | NA:0 | R/W:000 | | |
| HW Access | NA | | R | | NA | R | | |
| Name | | | power_comp | | | power2_3 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 5:4 | power_comp[1:0] | The power control for the quantizer block See Table 1-276. |
| 2:0 | power2_3[2:0] | The power control for the second and third integrator stages See Table 1-275. |

Table 1-275. Bit field encoding: POWER2_3_ENUM

| Value | Name | Description |
|-------|-----------------|---------------|
| 3'h0 | POWER2_3_LOW | LOW (4uA) |
| 3'h1 | POWER2_3_MEDIUM | MEDIUM (17uA) |
| 3'h2 | POWER2_3_HIGH | HIGH (68uA) |
| 3'h3 | POWER2_3_1P5X | 1.5X (100uA) |
| 3'h4 | POWER2_3_2X | 2X (135uA) |
| 3'h5 | POWER2_3_HIGH_5 | HIGH (68uA) |
| 3'h6 | POWER2_3_HIGH_6 | HIGH (68uA) |
| 3'h7 | POWER2_3_HIGH_7 | HIGH (68uA) |

Table 1-276. Bit field encoding: POWER_COMP_ENUM

| Value | Name | Description |
|-------|------------------|------------------|
| 2'h0 | POWER_COMP_VERYL | very low (2.2uA) |
| | OW | |
| 2'h1 | POWER_COMP_NORM | Normal (8.6uA) |
| | AL | |
| 2'h2 | POWER_COMP_6MHZ | 6MHz (17uA) |
| 2'h3 | POWER_COMP_12MHZ | 12MHz (35uA) |

1.3.394 DSM[0..0]_CR16

Delta Sigma Modulator Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR16: 0x40005890

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------|---|---|-------|-----------|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | R/W:0 | R/W:000 | | |
| HW Access | NA | R | | | R | R | | |
| Name | | power_sum | | | en_cp | cp_pwrctl | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------------|--|
| 6:4 | power_sum[2:0] | The power control for the summer block See Table 1-278. |
| 3 | en_cp | Enable charge pump |
| 2:0 | cp_pwrctl[2:0] | Charge Pump Power Control Modes See Table 1-277. |

Table 1-277. Bit field encoding: CP_PWRCTL_ENUM

| Value | Name | Description |
|-------|------------------|---|
| 3'h0 | CP_PWRCTL_TURBO | Charge pump operating in Turbo Power (560uA) mode |
| 3'h1 | CP_PWRCTL_2X | Charge pump operating in 6MHz (300uA) mode |
| 3'h2 | CP_PWRCTL_HIGH | Charge pump operating in High power (170uA) mode |
| 3'h3 | CP_PWRCTL_MEDIUM | Charge pump operating in Medium power (70uA) mode |
| 3'h4 | CP_PWRCTL_LOW | Charge pump operating in Low Power (30uA) mode |
| 3'h5 | CP_PWRCTL_5 | Reserved |
| 3'h6 | CP_PWRCTL_6 | Reserved |
| 3'h7 | CP_PWRCTL_7 | Reserved |

Table 1-278. Bit field encoding: POWER_SUM_ENUM

| Value | Name | Description |
|-------|------------------|---------------|
| 3'h0 | POWER_SUM_LOW | LOW (4uA) |
| 3'h1 | POWER_SUM_MEDIUM | MEDIUM (17uA) |
| 3'h2 | POWER_SUM_HIGH | HIGH (68uA) |
| 3'h3 | POWER_SUM_1P5X | 1.5X (100uA) |
| 3'h4 | POWER_SUM_2X | 2X (135uA) |
| 3'h5 | POWER_SUM_HIGH_5 | HIGH (68uA) |
| 3'h6 | POWER_SUM_HIGH_6 | HIGH (68uA) |
| 3'h7 | POWER_SUM_HIGH_7 | HIGH (68uA) |

1.3.395 DSM[0..0]_CR17

Delta Sigma Modulator Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR17: 0x40005891

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------------|---|--------------|---|---------------|---|------------|-------------|
| SW Access:Reset | R/W:00 | | R/W:00 | | R/W:00 | | R/W:0 | R/W:0 |
| HW Access | R | | R | | R | | R | R |
| Name | pwr_ctrl_vref_inn | | pwr_ctrl_vcm | | pwr_ctrl_vref | | en_buf_vcm | en_buf_vref |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------------------|---|
| 7:6 | pwr_ctrl_vref_inn[1:0] | Power control modes for REFBUF1 (the reference buffer that connects ADC reference to the negative input MUX of the channel) See Table 1-283. |
| 5:4 | pwr_ctrl_vcm[1:0] | Power Control for the Voltage Common Mode Buffer for the Sigma Delta ADC See Table 1-281. |
| 3:2 | pwr_ctrl_vref[1:0] | Power Control for the Voltage Reference Buffer for the Sigma Delta ADC See Table 1-282. |
| 1 | en_buf_vcm | Enable/Disable control for ADC (Internal)Reference Buffer See Table 1-279. |
| 0 | en_buf_vref | Enable/Disable control for ADC (Internal)Reference Buffer See Table 1-280. |

Table 1-279. Bit field encoding: EN_BUF_VCM_ENUM

| Value | Name | Description |
|-------|--------------|---|
| 1'h0 | EN_BUF_VCM_0 | The ADC Output common mode (VCM) voltage buffer is powered down |
| 1'h1 | EN_BUF_VCM_1 | The ADC Output common mode (VCM) voltage buffer is NOT powered down |

Table 1-280. Bit field encoding: EN_BUF_VREF_ENUM

| Value | Name | Description |
|-------|---------------|---|
| 1'h0 | EN_BUF_VREF_0 | The Internal Reference Voltage Buffer is powered down |
| 1'h1 | EN_BUF_VREF_1 | The Internal Reference Voltage Buffer is NOT powered down |

Table 1-281. Bit field encoding: PWR_CTRL_VCM_ENUM

| Value | Name | Description |
|-------|----------------|--|
| 2'h0 | PWR_CTRL_VCM_0 | VCM Buffer is operating in Low Power (18 uA) mode |
| 2'h1 | PWR_CTRL_VCM_1 | VCM Buffer is operating in Medium Power (28 uA) mode |
| 2'h2 | PWR_CTRL_VCM_2 | VCM Buffer is operating in High Power (55 uA) mode |
| 2'h3 | PWR_CTRL_VCM_3 | VCM Buffer is operating in Turbo Power (114 uA) mode |

1.3.395 DSM[0..0]_CR17 (continued)

Table 1-282. Bit field encoding: PWR_CTRL_VREF_ENUM

| Value | Name | Description |
|-------|-----------------|---|
| 2'h0 | PWR_CTRL_VREF_0 | VREF Buffer is operating in Low Power (26 uA) mode |
| 2'h1 | PWR_CTRL_VREF_1 | VREF Buffer is operating in Medium Power (32 uA) mode |
| 2'h2 | PWR_CTRL_VREF_2 | VREF Buffer is operating in High Power (118 uA) mode |
| 2'h3 | PWR_CTRL_VREF_3 | VREF Buffer is operating in Turbo Power (232 uA) mode |

Table 1-283. Bit field encoding: PWR_CTRL_VREF_INN_ENUM

| Value | Name | Description |
|-------|--------------------------|---|
| 2'h0 | PWR_CTRL_VREF_INN_LOW | VREF Buffer (Input mux path) is operating in Low Power (26uA) mode |
| 2'h1 | PWR_CTRL_VREF_INN_MEDIUM | VREF Buffer (Input mux path) is operating in Medium Power (32uA) mode |
| 2'h2 | PWR_CTRL_VREF_INN_HIGH | VREF Buffer (Input mux path) is operating in High Power (118uA) mode |
| 2'h3 | PWR_CTRL_VREF_INN_TURBO | VREF Buffer (Input mux path) is operating in Turbo Power (232uA) mode |

1.3.396 DSM[0..0]_REF0

Delta Sigma Modulator Reference Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF0: 0x40005892

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|------|-----------------|-----------------|---------|---|---|
| SW Access:Reset | R/W:00 | | NA:0 | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | R | | NA | R | R | R | | |
| Name | vcmsel | | | vref_res_div_en | en_buf_vref_inn | refmux | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|---|
| 7:6 | vcmsel[1:0] | Output common mode selection for modulator See Table 1-285. |
| 4 | vref_res_div_en | If enabled it allows the resistor divided value of (VDDA/3 or VDDA/4) to a selectable voltage for the RefMux |
| 3 | en_buf_vref_inn | Enable/Disable control for ADC (internal) REFBUF1 Buffer; This buffers the ADC reference before being sent to INN Mux; See IROS DSM chapter |
| 2:0 | refmux[2:0] | Mux control that allows for selecting one among the various available internal reference values See Table 1-284. |

Table 1-284. Bit field encoding: REFMUX_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | REFMUX_0 | No Selection made for VCM |
| 3'h1 | REFMUX_1 | VDAC0 output is the reference for the DSM |
| 3'h2 | REFMUX_2 | VDDA/4 is selected as the reference for the DSM (VDDA is the external voltage supply) |
| 3'h3 | REFMUX_3 | VDDA/3 is selected as the reference for the DSM (VDDA is the external voltage supply) |
| 3'h4 | REFMUX_4 | internal precision bandgap reference of 1.024 (typ) is selected as the DSM reference |
| 3'h5 | REFMUX_5 | internal precision bandgap reference of 1.2V (typ) is selected as the DSM reference |
| 3'h6 | REFMUX_6 | N/A |
| 3'h7 | REFMUX_7 | N/A |

Table 1-285. Bit field encoding: VCMSEL_ENUM

| Value | Name | Description |
|-------|----------|--|
| 2'h0 | VCMSEL_0 | No selection is made for VCM |
| 2'h1 | VCMSEL_1 | 0.8V from bandgap trim buffer is being selected as VCM (output common mode) for the DSM opamps |
| 2'h2 | VCMSEL_2 | 0.7V from bandgap trim buffer is being selected as VCM (output common mode) |
| 2'h3 | VCMSEL_3 | Vssd being selected as VCM (output common mode) for the DSM opamps |

1.3.397 DSM[0..0]_REF1

Delta Sigma Modulator Reference Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF1: 0x40005893

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|------------------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | dac_gnd_sel I |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 0 | dac_gnd_sel | Selects DSM Reference DAC Capacitor Ground See Table 1-286. |

Table 1-286. Bit field encoding: DSM_DAC_GND_SEL_ENUM

| Value | Name | Description |
|-------|-------------------------|-------------------------------|
| 1'b0 | DSM_DAC_GND_SEL_I NT | select DSM internal vssa |
| 1'b1 | DSM_DAC_GND_SEL_ EXT | select external ground (AGL6) |

1.3.398 DSM[0..0]_REF2

Delta Sigma Modulator Reference Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF2: 0x40005894

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | s7_en | s6_en | s5_en | s4_en | s3_en | s2_en | s1_en | s0_en |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 7 | s7_en | If Set, closes the S7 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 6 | s6_en | If Set, closes the S6 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 5 | s5_en | If Set, closes the S5 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 4 | s4_en | If Set, closes the S4 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 3 | s3_en | If Set, closes the S3 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 2 | s2_en | If Set, closes the S2 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 1 | s1_en | If Set, closes the S1 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 0 | s0_en | If Set, closes the S0 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |

1.3.399 DSM[0..0]_REF3

Delta Sigma Modulator Reference Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF3: 0x40005895

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|--------|--------|--------|-------|-------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R | R | R | R | R | R |
| Name | | | s13_en | s12_en | s11_en | s10_en | s9_en | s8_en |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|---|
| 5 | s13_en | If Set, closes the S13 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 4 | s12_en | If Set, closes the S12 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 3 | s11_en | If Set, closes the S11 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 2 | s10_en | If Set, closes the S10 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 1 | s9_en | If Set, closes the S9 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |
| 0 | s8_en | If Set, closes the S8 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel |

1.3.400 DSM[0..0]_DEMO

Delta Sigma Modulator Dynamic Element Matching Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_DEMO: 0x40005896

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------------|-------------|--------|---------------|---------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | demtest_src | adc_test_en | en_dem | en_scrambler1 | en_scrambler0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------------|--|
| 4 | demtest_src | Select demtest source See Table 1-288. |
| 3 | adc_test_en | Enable/Disable All test modes in Sigma Delta Channel See Table 1-287. |
| 2 | en_dem | Enable DEM See Table 1-289. |
| 1 | en_scrambler1 | Enable Scrambler 1 See Table 1-291. |
| 0 | en_scrambler0 | Enable Scrambler 0 See Table 1-290. |

Table 1-287. Bit field encoding: ADC_TEST_EN_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'h0 | ADC_TEST_EN_0 | Disable all test modes for the sigma delta channel |
| 1'h1 | ADC_TEST_EN_1 | Enable all test modes for the sigma delta channel |

Table 1-288. Bit field encoding: DEMTEST_SRC_ENUM

| Value | Name | Description |
|-------|-----------------|---|
| 1'h0 | DEMTEST_SRC_REG | ANAIF register source selected - DSM#_DEM1.demtest[7:0] |
| 1'h1 | DEMTEST_SRC_UDB | UDB array source selected - dsi_anaif_dft[7:0] |

Table 1-289. Bit field encoding: EN_DEM_ENUM

| Value | Name | Description |
|-------|----------------|-------------|
| 1'h0 | EN_DEM_DISABLE | Disable DEM |
| 1'h1 | EN_DEM_ENABLE | Enable DEM |

Table 1-290. Bit field encoding: EN_SCRAMBLER0_ENUM

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.400 DSM[0..0]_DEMO (continued)

Table 1-290. Bit field encoding: EN_SCRAMBLER0_ENUM

| | | |
|------|---------------------------|---------------------|
| 1'h0 | EN_SCRAMBLER0_DIS ABLE | Disable Scrambler 0 |
| 1'h1 | EN_SCRAMBLER0_EN ABLE | Enable Scrambler 0 |

Table 1-291. Bit field encoding: EN_SCRAMBLER1_ENUM

| Value | Name | Description |
|-------|---------------------------|---------------------|
| 1'h0 | EN_SCRAMBLER1_DIS ABLE | Disable Scrambler 1 |
| 1'h1 | EN_SCRAMBLER1_EN ABLE | Enable Scrambler 1 |

1.3.401 DSM[0..0]_DEM1

Delta Sigma Modulator Dynamic Element Matching Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_DEM1: 0x40005897

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | demtest | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | demtest[7:0] | Register control for the DAC unit elements inside the first integrator. This can be used when bit DSM.DEM0[3], <code>adc_test_en</code> , is set. If the <code>adc_test_en</code> is not set the the control logic inside the modulator determines how the DAC unit elements are controlled. This is meant for static testing purposes |

1.3.402 DSM[0..0]_TST0

Delta Sigma Modulator Test Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_TST0: 0x40005898

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------------|---|---|-------------|---|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | R/W:0000 | | | |
| HW Access | NA | R | | | R | | | |
| Name | | dig_test_sel | | | refsel_ctrl | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------------|---|
| 6:4 | dig_test_sel[2:0] | To test various digital outputs to digital muxes (for DFT) See Table 1-292. |
| 3:0 | refsel_ctrl[3:0] | This is the 4-bit encoded value which selects one among the 15 important DFT observable points inside the DSM. 4'h0 (0000) through 4'ha (1010) selects between various tap points in the quantizer resistor ladder. 4'hb (1011) through 4'he (1110) selects special points inside the DSM See Table 1-293. |

Table 1-292. Bit field encoding: DIG_TEST_SEL_ENUM

| Value | Name | Description |
|-------|----------------|---|
| 3'h0 | DIG_TEST_SEL_0 | test_dig_out = vhi |
| 3'h1 | DIG_TEST_SEL_1 | test_dig_out = hi |
| 3'h2 | DIG_TEST_SEL_2 | test_dig_out = med |
| 3'h3 | DIG_TEST_SEL_3 | test_dig_out = low |
| 3'h4 | DIG_TEST_SEL_4 | test_dig_out = sign |
| 3'h5 | DIG_TEST_SEL_5 | test_dig_out = reset_ov |
| 3'h6 | DIG_TEST_SEL_6 | test_dig_out = TESTMODE & Phi1 (sampling clock phase) |
| 3'h7 | DIG_TEST_SEL_7 | test_dig_out = TESTMODE & fchclk (chopping clock) |

Table 1-293. Bit field encoding: REFSEL_CTRL_ENUM

| Value | Name | Description |
|-------|----------------|--|
| 4'h0 | REFSEL_CTRL_0 | (9/32)*Vref |
| 4'h1 | REFSEL_CTRL_1 | (11/32)*Vref |
| 4'h2 | REFSEL_CTRL_2 | (12/32)*Vref |
| 4'h3 | REFSEL_CTRL_3 | (13/32)*Vref |
| 4'h4 | REFSEL_CTRL_4 | (15/32)*Vref |
| 4'h5 | REFSEL_CTRL_5 | (16/32)*Vref |
| 4'h6 | REFSEL_CTRL_6 | (17/32)*Vref |
| 4'h7 | REFSEL_CTRL_7 | (19/32)*Vref |
| 4'h8 | REFSEL_CTRL_8 | (20/32)*Vref |
| 4'h9 | REFSEL_CTRL_9 | (21/32)*Vref |
| 4'ha | REFSEL_CTRL_10 | (23/32)*Vref |
| 4'hb | REFSEL_CTRL_11 | Selects VICM (Input Common Mode) applied to DSM to be available at Ref_out DFT point |

1.3.402 DSM[0..0]_TST0 (continued)

Table 1-293. Bit field encoding: REFSEL_CTRL_ENUM

| | | |
|------|----------------|---|
| 4'hc | REFSEL_CTRL_12 | Selects Vb0 (2nd and 3rd integrator Opamp Bias Voltage) inside the DSM to Ref_out DFT point |
| 4'hd | REFSEL_CTRL_13 | Selects VRCM (Half of applied Reference) inside the DSM to Ref_out DFT point |
| 4'he | REFSEL_CTRL_14 | Selects vbias0_int, an internal bias point from inside the DSM to Ref_out DFT point |
| 4'hf | REFSEL_CTRL_15 | Not a valid selection |

1.3.403 DSM[0..0]_TST1

Delta Sigma Modulator Test Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_TST1: 0x40005899

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|-------------|
| 7:0 | RSVD[7:0] | Reserved |

1.3.404 DSM[0..0]_BUF0

Delta Sigma Modulator Buffer Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF0: 0x4000589A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|--------------|----------|----------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | rail_rail_en | bypass_p | enable_p |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|---|
| 2 | rail_rail_en | Selects Rail-to-Rail Mode See Table 1-296. |
| 1 | bypass_p | Remove positive half of the buffer from signal path See Table 1-294. |
| 0 | enable_p | Buffer Positive Half Enable See Table 1-295. |

Table 1-294. Bit field encoding: BYPASS_P_ENUM

| Value | Name | Description |
|-------|------------|---|
| 1'b0 | BYPASS_P_0 | The buffer in the positive half remains on the signal path (Refer Fig 33-2) |
| 1'b1 | BYPASS_P_1 | bypass the buffer on the positive half of the signal path (Refer Fig 33-2) |

Table 1-295. Bit field encoding: ENABLE_P_ENUM

| Value | Name | Description |
|-------|------------|------------------------------------|
| 1'b0 | ENABLE_P_0 | power down buffer in positive half |
| 1'b1 | ENABLE_P_1 | enable positive half of buffer |

Table 1-296. Bit field encoding: RAIL_RAIL_EN_ENUM

| Value | Name | Description |
|-------|---------------------|-------------------------|
| 1'h0 | RAIL_RAIL_EN_DISABL | Level shifted mode E |
| 1'h1 | RAIL_RAIL_EN_ENABL | Rail-to-Rail mode E |

1.3.405 DSM[0..0]_BUF1

Delta Sigma Modulator Buffer Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF1: 0x4000589B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|--------|---|----------|----------|
| SW Access:Reset | NA:0000 | | | | R/W:00 | | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | | R | R |
| Name | | | | | gain | | bypass_n | enable_n |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|---|
| 3:2 | gain[1:0] | Gain settings of 1,2,4,8 are supported See Table 1-299. |
| 1 | bypass_n | Remove negative half of the buffer from signal path See Table 1-297. |
| 0 | enable_n | Buffer Negative Half Enable See Table 1-298. |

Table 1-297. Bit field encoding: BYPASS_N_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 1'b0 | BYPASS_N_DISABLE_ | The buffer in the negative half remains on the signal path (Refer Fig 33-2) |
| 1'b1 | BYPASS_N_ENABLE_B | bypass the buffer on the negative half of the signal path (Refer Fig 33-2) |

Table 1-298. Bit field encoding: ENABLE_N_ENUM

| Value | Name | Description |
|-------|------------|------------------------------------|
| 1'b0 | ENABLE_N_0 | power down buffer in negative half |
| 1'b1 | ENABLE_P_1 | enable negative half of buffer |

Table 1-299. Bit field encoding: GAIN_ENUM

| Value | Name | Description |
|-------|---------|-------------|
| 2'h0 | GAIN_1X | 1x |
| 2'h1 | GAIN_2X | 2x |
| 2'h2 | GAIN_4X | 4x |
| 2'h3 | GAIN_8X | 8x |

1.3.406 DSM[0..0]_BUF2

Delta Sigma Modulator Buffer Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF2: 0x4000589C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|------------------|-----------------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | add_extra_r c | lowpower_e n |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|---|
| 1 | add_extra_rc | If enabled an additional RC is included at the output of the buffer differentially, to lower noise at the expense of settling else normal settling. |
| 0 | lowpower_en | Enables the lower power mode of operation. The normal power mode implies 600uA typical current consumption per opamp in the buffer. See Table 1-300. |

Table 1-300. Bit field encoding: LOWPOWER_EN_ENUM

| Value | Name | Description |
|-------|------------------------|---|
| 1'h0 | LOWPOWER_EN_NOR MAL | Input buffer operated in normal power mode |
| 1'h1 | LOWPOWER_EN_LOW | Input buffer operated in low (1/4th of normal power) power mode |

1.3.407 DSM[0..0]_BUF3

Delta Sigma Modulator Buffer Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF3: 0x4000589D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-------------|-----------|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:000 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | buf_chop_en | buf_fchop | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------------|---|
| 3 | buf_chop_en | Enable/ Disable Chopping of the input buffer (TYPE A or B as selected in DSM_BUF0 register) See Table 1-301. |
| 2:0 | buf_fchop[2:0] | Input Buffer Chopping frequency control See Table 1-302. |

Table 1-301. Bit field encoding: BUF_CHOP_EN_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BUF_CHOP_EN_0 | Disable Chopping of the input buffer (type is as determined by |
| 1'b1 | BUF_CHOP_EN_1 | Enable Chopping of the input buffer |

Table 1-302. Bit field encoding: BUF_FCHOP_ENUM

| Value | Name | Description |
|-------|-------------|------------------------------|
| 3'h0 | BUF_FCHOP_0 | chopping frequency is fs/2 |
| 3'h1 | BUF_FCHOP_1 | chopping frequency is fs/4 |
| 3'h2 | BUF_FCHOP_2 | chopping frequency is fs/8 |
| 3'h3 | BUF_FCHOP_3 | chopping frequency is fs/16 |
| 3'h4 | BUF_FCHOP_4 | chopping frequency is fs/32 |
| 3'h5 | BUF_FCHOP_5 | chopping frequency is fs/64 |
| 3'h6 | BUF_FCHOP_6 | chopping frequency is fs/128 |
| 3'h7 | BUF_FCHOP_7 | chopping frequency is fs/256 |

1.3.408 DSM[0..0]_MISC

Delta Sigma Modulator Miscellaneous register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_MISC: 0x4000589E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|----------|------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | | | | R | R | NA | R |
| Name | | | | | swvn_src | swvp_src | | sel_iclk_cp |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|---|
| 3 | swvn_src | negative input routing control source See Table 1-303. |
| 2 | swvp_src | positive input routing control source See Table 1-304. |
| 0 | sel_iclk_cp | Select Charge Pump Internal Clock See Table 1-305. |

Table 1-303. Bit field encoding: DSM_SWVN_SRC_ENUM

| Value | Name | Description |
|-------|------------------|-----------------------------|
| 1'b0 | DSM_SWVN_SRC_REG | ANAIF DSM routing registers |
| 1'b1 | DSM_SWVN_SRC_UDB | UDB |

Table 1-304. Bit field encoding: DSM_SWVP_SRC_ENUM

| Value | Name | Description |
|-------|------------------|-----------------------------|
| 1'b0 | DSM_SWVP_SRC_REG | ANAIF DSM routing registers |
| 1'b1 | DSM_SWVP_SRC_UDB | UDB |

Table 1-305. Bit field encoding: SEL_ICLK_CP_ENUM

| Value | Name | Description |
|-------|--------------------|---|
| 1'b0 | SEL_ICLK_CP_EXTER | External (DSI) Charge Pump Clock selected |
| | NAL | |
| 1'b1 | SEL_ICLK_CP_INTERN | Internal Charge Pump Clock selected |
| | AL | |

1.3.409 DSM[0..0]_RSVD1

Delta Sigma Modulator RSVD 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_RSVD1: 0x4000589F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|-------------|
| 7:0 | RSVD[7:0] | Reserved |

1.3.410 SAR[0..1]_CSR0

SAR status and control register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR0: 0x40005900

SAR1_CSR0: 0x40005908

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|------------|--------------|-------|--------|----------|---------|
| SW Access:Reset | R/W:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | | R | R | R | R | R | R |
| Name | icont | | reset_soft | coherency_en | hiz | mx_sof | sof_mode | sof_bit |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|--|
| 7:6 | icont[1:0] | current control See Table 1-306. |
| 5 | reset_soft | firmware reset (not autoclearing) - can be used to stop a conversion See Table 1-310. |
| 4 | coherency_en | Coherency Locking enable See Table 1-307. |
| 3 | hiz | Sample time HiZ See Table 1-308. |
| 2 | mx_sof | Start-of-Frame (sof) source selection See Table 1-309. |
| 1 | sof_mode | Start-of-Frame (sof) mode See Table 1-312. |
| 0 | sof_bit | Start-of-Frame (sof) register source; enable conversion; (NOTE: autoclearing upon receipt of eof_sync when sof_mode==edge-sensitive) See Table 1-311. |

Table 1-306. Bit field encoding: ICONT_ENUM

| Value | Name | Description |
|-------|---------|------------------------|
| 2'h0 | ICONT_0 | Full current |
| 2'h1 | ICONT_1 | 1/2 of maximum current |
| 2'h2 | ICONT_2 | 1/3 of maximum current |
| 2'h3 | ICONT_3 | 1/4 of maximum current |

Table 1-307. Bit field encoding: SAR_COHERENCY_EN_ENUM

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.410 SAR[0..1]_CSR0 (continued)

Table 1-307. Bit field encoding: SAR_COHERENCY_EN_ENUM

| | | |
|------|-------------------------|--|
| 1'b0 | SAR_COHERENCY_EN_NOLOCK | Coherency locking off |
| 1'b1 | SAR_COHERENCY_EN_LOCK | Coherency Locking on Coherency locking blocks SAR data output registers if only one of the two registers has been read |

Table 1-308. Bit field encoding: SAR_HIZ_ENUM

| Value | Name | Description |
|-------|----------------|---|
| 1'b0 | SAR_HIZ_CLEAR | Clear DAC value at beginning of sampling |
| 1'b1 | SAR_HIZ_RETAIN | Retain DAC value at beginning of sampling |

Table 1-309. Bit field encoding: SAR_MX_SOF_ENUM

| Value | Name | Description |
|-------|----------------|-----------------|
| 1'b0 | SAR_MX_SOF_BIT | source: sof_bit |
| 1'b1 | SAR_MX_SOF_UDB | source: UDB |

Table 1-310. Bit field encoding: SAR_RESET_SOFT_ENUM

| Value | Name | Description |
|-------|--------------------------|-----------------------|
| 1'b0 | SAR_RESET_SOFT_NOTACTIVE | reset soft not active |
| 1'b1 | SAR_RESET_SOFT_ACTIVE | reset soft active |

Table 1-311. Bit field encoding: SAR_SOF_BIT_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | SAR_SOF_BIT_0 | disable conversion |
| 1'b1 | SAR_SOF_BIT_1 | Enable conversion |

Table 1-312. Bit field encoding: SAR_SOF_MODE_ENUM

| Value | Name | Description |
|-------|--------------------|----------------------------|
| 1'b0 | SAR_SOF_MODE_LEVEL | level-sensitive sof source |
| 1'b1 | SAR_SOF_MODE_EDGE | edge-sensitive sof source |

@0x40005900 + [0..1 * 0x8] + 0x1

1.3.411 SAR[0..1]_CSR1

SAR status and control register 1

Reset: Reset Signals Listed Below

Register : Address

SAR0_CSR1: 0x40005901

SAR1_CSR1: 0x40005909

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|----------|----------|----------|----------|------|
| SW Access:Reset | R/W:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | RC:0 |
| HW Access | R | | | R | R | R | R | R/W |
| Name | muxref | | | swvp_src | swvn_src | irq_mode | irq_mask | eof |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|---|
| 7:5 | muxref[2:0] | SAR reference mux control See Table 1-316. |
| 4 | swvp_src | SAR positive input routing control source See Table 1-318. |
| 3 | swvn_src | SAR negative input routing control source See Table 1-317. |
| 2 | irq_mode | interrupt mode See Table 1-315. |
| 1 | irq_mask | Enable interrupt request from eof See Table 1-314. |
| 0 | eof | End Of Frame - clear-on-read sticky bit See Table 1-313. |

Reset Table

| resetsignal | field(s) |
|---|---|
| System reset for retention flops [reset_all_retention] | irq_mask, irq_mode, swvn_src, swvp_src, muxref[2:0] |
| Domain reset for non-retention flops [reset_all_nonretention] | eof |

Table 1-313. Bit field encoding: SAR_EOF_ENUM

| Value | Name | Description |
|-------|-----------|------------------|
| 1'b0 | SAR_EOF_0 | data_out NOT new |

1.3.411 SAR[0..1]_CSR1 (continued)

Table 1-313. Bit field encoding: SAR_EOF_ENUM

| | | |
|------|-----------|----------------------------|
| 1'b1 | SAR_EOF_1 | End-of-Frame; data_out new |
|------|-----------|----------------------------|

Table 1-314. Bit field encoding: SAR_IRQ_MASK_ENUM

| Value | Name | Description |
|-------|------------------|-------------|
| 1'b0 | SAR_IRQ_MASK_DIS | disabled |
| 1'b1 | SAR_IRQ_MASK_EN | enabled |

Table 1-315. Bit field encoding: SAR_IRQ_MODE_ENUM

| Value | Name | Description |
|-------|-------------------|-------------|
| 1'b0 | SAR_IRQ_MODE_LEVE | level |
| | L | |
| 1'b1 | SAR_IRQ_MODE_EDG | edge |
| | E | |

Table 1-316. Bit field encoding: SAR_MUXREF_ENUM

| Value | Name | Description |
|-------|--------------|--|
| 3'h0 | SAR_MUXREF_0 | Not Used |
| 3'h1 | SAR_MUXREF_1 | Not Used |
| 3'h2 | SAR_MUXREF_2 | vda/2 (also set en_resvda bit in CSR3) |
| 3'h3 | SAR_MUXREF_3 | vdac |
| 3'h4 | SAR_MUXREF_4 | BG vref1 (1.024V) |
| 3'h5 | SAR_MUXREF_5 | BG vref2 (1.2V) |
| 3'h6 | SAR_MUXREF_6 | Not Used |
| 3'h7 | SAR_MUXREF_7 | Not Used |

Table 1-317. Bit field encoding: SAR_SWVN_SRC_ENUM

| Value | Name | Description |
|-------|------------------|-----------------------------|
| 1'b0 | SAR_SWVN_SRC_REG | ANAIF SAR routing registers |
| 1'b1 | SAR_SWVN_SRC_UDB | UDB |

Table 1-318. Bit field encoding: SAR_SWVP_SRC_ENUM

| Value | Name | Description |
|-------|------------------|-----------------------------|
| 1'b0 | SAR_SWVP_SRC_REG | ANAIF SAR routing registers |
| 1'b1 | SAR_SWVP_SRC_UDB | UDB |

1.3.412 SAR[0..1]_CSR2

SAR status and control register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR2: 0x40005902

SAR1_CSR2: 0x4000590A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|------------------|---|---|------------------|---|---|
| SW Access:Reset | R/W:00 | | R/W:000 | | | R/W:000 | | |
| HW Access | R | | R | | | R | | |
| Name | resolution | | sample_width_msb | | | sample_width_lsb | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------------|--|
| 7:6 | resolution[1:0] | 8b,10b,12b resolution selection (data_out is LSBit aligned (right-shifted) according to the resolution mode) See Table 1-319. |
| 5:3 | sample_width_msb[2:0] | Sample time down counter start value MSB |
| 2:0 | sample_width_lsb[2:0] | Sample time down counter start value LSB See Table 1-320. |

Table 1-319. Bit field encoding: SAR_RESOLUTION_ENUM

| Value | Name | Description |
|-------|----------------------------------|--|
| 2'h0 | SAR_RESOLUTION_12 BIT_DEFAULT | 12-bit conversion = data_out[11:0] |
| 2'h1 | SAR_RESOLUTION_8BI T | 8-bit conversion = data_out[7:0] (data_out[11:8] = 4'b0) |
| 2'h2 | SAR_RESOLUTION_10 BIT | 10-bit conversion = data_out[9:0] (data_out[11:10] = 2'b0) |
| 2'h3 | SAR_RESOLUTION_12 BIT_ALSO | 12-bit conversion = data_out[11:0] |

Table 1-320. Bit field encoding: SAR_SAMPLE_WIDTH_LSB_ENUM

| Value | Name | Description |
|-------|------------------------------|--------------------------------------|
| 3'h0 | SAR_SAMPLE_WIDTH_ LSB_MIN | minimum sample time: +1 clock cycle |
| 3'h7 | SAR_SAMPLE_WIDTH_ LSB_MAX | maximum sample time: +8 clock cycles |

1.3.413 SAR[0..1]_CSR3

SAR status and control register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR3: 0x40005903

SAR1_CSR3: 0x4000590B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------|--------------|---|---------------|---|------------|-------------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:00 | | R/W:00 | | R/W:0 | R/W:0 |
| HW Access | NA | R | R | | R | | R | R |
| Name | | en_resvda | pwr_ctrl_vcm | | pwr_ctrl_vref | | en_buf_vcm | en_buf_vref |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------------|--|
| 6 | en_resvda | Enable SAR vda resister ladder divider See Table 1-323. |
| 5:4 | pwr_ctrl_vcm[1:0] | SAR VCM reference power control See Table 1-324. |
| 3:2 | pwr_ctrl_vref[1:0] | SAR VREF reference power control See Table 1-325. |
| 1 | en_buf_vcm | Enable SAR VCM reference buffer See Table 1-321. |
| 0 | en_buf_vref | Enable SAR VREF reference buffer See Table 1-322. |

Table 1-321. Bit field encoding: SAR_EN_BUF_VCM_ENUM

| Value | Name | Description |
|-------|-------------------|---------------|
| 1'b0 | SAR_EN_BUF_VCM_DI | disabled S |
| 1'b1 | SAR_EN_BUF_VCM_E | enabled N |

Table 1-322. Bit field encoding: SAR_EN_BUF_VREF_ENUM

| Value | Name | Description |
|-------|-------------------|----------------|
| 1'b0 | SAR_EN_BUF_VREF_D | disabled IS |
| 1'b1 | SAR_EN_BUF_VREF_E | enabled N |

Table 1-323. Bit field encoding: SAR_EN_RESVDA_ENUM

| Value | Name | Description |
|-------|-------------------|------------------------------|
| 1'b0 | SAR_EN_RESVDA_DIS | disabled (reference = Vdda) |
| 1'b1 | SAR_EN_RESVDA_EN | enabled (reference = Vdda/2) |

1.3.413 SAR[0..1]_CSR3 (continued)

Table 1-324. Bit field encoding: SAR_PWR_CTRL_VCM_ENUM

| Value | Name | Description |
|-------|------------------------|-------------|
| 2'h0 | SAR_PWR_CTRL_VCM _0 | Not used |
| 2'h1 | SAR_PWR_CTRL_VCM _1 | Not used |
| 2'h2 | SAR_PWR_CTRL_VCM _2 | Not used |
| 2'h3 | SAR_PWR_CTRL_VCM _3 | Not used |

Table 1-325. Bit field encoding: SAR_PWR_CTRL_VREF_ENUM

| Value | Name | Description |
|-------|--------------------------|-------------|
| 2'h0 | SAR_PWR_CTRL_VREF F_0 | Max power |
| 2'h1 | SAR_PWR_CTRL_VREF F_1 | divide by 2 |
| 2'h2 | SAR_PWR_CTRL_VREF F_2 | divide by 3 |
| 2'h3 | SAR_PWR_CTRL_VREF F_3 | divide by 4 |

1.3.414 SAR[0..1]_CSR4

SAR status and control register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR4: 0x40005904

SAR1_CSR4: 0x4000590C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|------------|------------|------------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | R | R | R | R | R | R | R |
| Name | | dft_outc_2 | dft_outc_1 | dft_outc_0 | dft_inc_3 | dft_inc_2 | dft_inc_1 | dft_inc_0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|--|
| 6 | dft_outc_2 | DFT observe point enable See Table 1-327. |
| 5 | dft_outc_1 | DFT observe point enable See Table 1-327. |
| 4 | dft_outc_0 | DFT observe point enable See Table 1-327. |
| 3 | dft_inc_3 | DFT control point enable See Table 1-326. |
| 2 | dft_inc_2 | DFT control point enable See Table 1-326. |
| 1 | dft_inc_1 | DFT control point enable See Table 1-326. |
| 0 | dft_inc_0 | DFT control point enable See Table 1-326. |

Table 1-326. Bit field encoding: SAR_DFT_INC_ENUM

| Value | Name | Description |
|-------|--------------------|----------------------------|
| 1'b0 | SAR_DFT_INC_DISABL | dft control point disabled |
| | ED | |
| 1'b1 | SAR_DFT_INC_ENABL | dft control point enabled |
| | ED | |

Table 1-327. Bit field encoding: SAR_DFT_OUTC_ENUM

| Value | Name | Description |
|-------|-------------------|----------------------------|
| 1'b0 | SAR_DFT_OUTC_DISA | dft observe point disabled |
| | BLED | |

1.3.414 SAR[0..1]_CSR4 (continued)

Table 1-327. Bit field encoding: SAR_DFT_OUTC_ENUM

| | | |
|------|------------------|---------------------------|
| 1'b1 | SAR_DFT_OUTC_ENA | dft observe point enabled |
| | BLED | |

1.3.415 SAR[0..1]_CSR5

SAR status and control register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR5: 0x40005905

SAR1_CSR5: 0x4000590D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---------|-------|-------------|--------------|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0000 | | | |
| HW Access | R | R | R | R | R | | | |
| Name | overrun_det_en | dly_inc | dcen | en_csel_dft | sel_csel_dft | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------------|---|
| 7 | overrun_det_en | Enable data overrun detection See Table 1-331. |
| 6 | dly_inc | Control for delay circuits See Table 1-329. |
| 5 | dcen | Short AC coupling in comparator for DFT See Table 1-328. |
| 4 | en_csel_dft | Enable for sel_csel_dft See Table 1-330. |
| 3:0 | sel_csel_dft[3:0] | To use this test value set en_csel_dft See Table 1-332. |

Table 1-328. Bit field encoding: SAR_DCEN_ENUM

| Value | Name | Description |
|-------|------------|-------------|
| 1'b0 | SAR_DCEN_0 | not shorted |
| 1'b1 | SAR_DCEN_1 | shorted |

Table 1-329. Bit field encoding: SAR_DLY_INC_ENUM

| Value | Name | Description |
|-------|---------------|-------------|
| 1'b0 | SAR_DLY_INC_0 | low delay |
| 1'b1 | SAR_DLY_INC_1 | high delay |

Table 1-330. Bit field encoding: SAR_EN_CSEL_DFT_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 1'b0 | SAR_EN_CSEL_DFT_D | Normal mode ISABLED |
| 1'b1 | SAR_EN_CSEL_DFT_E | Test mode; sel_csel_dft[3:0] used NABLED |

1.3.415 SAR[0..1]_CSR5 (continued)

Table 1-331. Bit field encoding: SAR_OVERRUN_DET_EN_ENUM

| Value | Name | Description |
|-------|------------------------|-------------|
| 1'b0 | SAR_OVERRUN_DET_EN_DIS | disabled |
| 1'b1 | SAR_OVERRUN_DET_EN_EN | enabled |

Table 1-332. Bit field encoding: SAR_SEL_CSEL_DFT_ENUM

| Value | Name | Description |
|-------|----------------------|--------------|
| 4'h0 | SAR_SEL_CSEL_DFT_MIN | min csel_dft |
| 4'hf | SAR_SEL_CSEL_DFT_MAX | max csel_dft |

1.3.416 SAR[0..1]_CSR6

SAR status and control register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR6: 0x40005906

SAR1_CSR6: 0x4000590E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ref_s | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 7:0 | ref_s[7:0] | Enable reference switch. ref_s[6:5], ref_s[1:0] are unused. Refer to SAR section of the TRM Book1 for details See Table 1-333. |

Table 1-333. Bit field encoding: SAR_REF_S_ENUM

| Value | Name | Description |
|-------|-----------|--|
| 8'h04 | EXT_VREF | External Vref when SAR[0..1]_CSR3[0] is set to 1'b0 |
| 8'h18 | INT_VREF1 | Internal Vref with no bypass cap when SAR[0..1]_CSR3[0] is set to 1'b1 |
| 8'h04 | INT_VREF2 | Internal reference with bypass cap when SAR[0..1]_CSR3[0] is set to 1'b1 |
| 8'h80 | VDDA_VREF | Vdda as reference when SAR[0..1]_CSR3[0] is set to 1'b0 |

1.3.417 SC0_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW0: 0x40005A00

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vin_ag7 | vin_ag6 | vin_ag5 | vin_ag4 | vin_ag3 | vin_ag2 | vin_ag1 | vin_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 7 | vin_ag7 | Connect SC signal input VIN to analog global of same side See Table 1-334. |
| 6 | vin_ag6 | Connect SC signal input VIN to analog global of same side See Table 1-334. |
| 5 | vin_ag5 | Connect SC signal input VIN to analog global of same side See Table 1-334. |
| 4 | vin_ag4 | Connect SC signal input VIN to analog global of same side See Table 1-334. |
| 3 | vin_ag3 | Connect SC signal input VIN to analog global of same side See Table 1-334. |
| 2 | vin_ag2 | Connect SC signal input VIN to analog global of same side See Table 1-334. |
| 1 | vin_ag1 | Connect SC signal input VIN to analog global of same side See Table 1-334. |
| 0 | vin_ag0 | Connect SC signal input VIN to analog global of same side See Table 1-334. |

Table 1-334. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.418 SC0_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW2: 0x40005A02

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|-----------|------|-----------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | | | | R | R | NA | R |
| Name | | | | | vin_abus3 | vin_abus2 | | vin_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|--|
| 3 | vin_abus3 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-335. |
| 2 | vin_abus2 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-335. |
| 0 | vin_abus0 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-335. |

Table 1-335. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.419 SC0_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW3: 0x40005A03

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------------|--------|---|---|------------|---------|
| SW Access:Reset | NA:00 | | R/W:0 | NA:000 | | | R/W:0 | R/W:0 |
| HW Access | NA | | R | NA | | | R | R |
| Name | | | vref_bgvref | | | | vin_bgvref | vin_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|---|
| 5 | vref_bgvref | Connect SC signal input VREF to Bandgap Voltage Reference See Table 1-337. |
| 1 | vin_bgvref | Connect SC signal input VIN to Bandgap Voltage Reference See Table 1-337. |
| 0 | vin_amx | Connect SC signal input VIN to Analog Mux Bus See Table 1-336. |

Table 1-336. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-337. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

1.3.420 SC0_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW4: 0x40005A04

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|----------|------|----------|------|----------|------|----------|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | vref_ag6 | | vref_ag4 | | vref_ag2 | | vref_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|--|
| 6 | vref_ag6 | Connect SC signal input VREF to analog global of same side See Table 1-338. |
| 4 | vref_ag4 | Connect SC signal input VREF to analog global of same side See Table 1-338. |
| 2 | vref_ag2 | Connect SC signal input VREF to analog global of same side See Table 1-338. |
| 0 | vref_ag0 | Connect SC signal input VREF to analog global of same side See Table 1-338. |

Table 1-338. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.421 SC0_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW6: 0x40005A06

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|------------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | vref_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 0 | vref_abus0 | Connect SC signal input VREF to analog (local) bus of the same side See Table 1-339. |

Table 1-339. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.422 SC0_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW7: 0x40005A07

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|--------|-------|---|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:00 | |
| HW Access | NA | | | | | R/W | NA | |
| Name | | | | | | vin_vo | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 2 | vin_vo | Connect SC signal input VIN to VO of opposite SC See Table 1-340. |

Table 1-340. Bit field encoding: VIN_VO_ENUM

| Value | Name | Description |
|-------|----------|----------------------------------|
| 1'b0 | VIN_VO_0 | not connected |
| 1'b1 | VIN_VO_1 | Connect VIN to VO of opposite SC |

1.3.423 SC0_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW8: 0x40005A08

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|------|--------|------|--------|------|--------|------|
| SW Access:Reset | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | R | NA | R | NA | R | NA | R | NA |
| Name | vo_ag7 | | vo_ag5 | | vo_ag3 | | vo_ag1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vo_ag7 | Connect voltage output to analog global of same side (see field instance name) See Table 1-341. |
| 5 | vo_ag5 | Connect voltage output to analog global of same side (see field instance name) See Table 1-341. |
| 3 | vo_ag3 | Connect voltage output to analog global of same side (see field instance name) See Table 1-341. |
| 1 | vo_ag1 | Connect voltage output to analog global of same side (see field instance name) See Table 1-341. |

Table 1-341. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.424 SC0_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW10: 0x40005A0A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|------|----------|------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | NA | | | | R | NA | R | NA |
| Name | | | | | vo_abus3 | | vo_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 3 | vo_abus3 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-342. |
| 1 | vo_abus1 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-342. |

Table 1-342. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.425 SC0_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CLK: 0x40005A0B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------------|-------------|--------|---------|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | NA | | R/W | R | R | R | | |
| Name | | | dyn_cntl_en | bypass_sync | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 5 | dyn_cntl_en | Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-345. |
| 4 | bypass_sync | Bypass Synchronization See Table 1-343. |
| 3 | clk_en | Clock gating control See Table 1-344. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-346. |

Table 1-343. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-344. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-345. Bit field encoding: DYN_CNTL_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | DYN_CNTL_DIS | Dynamic Control Disabled |
| 1'b1 | DYN_CNTL_EN | Dynamic Control Enabled |

Table 1-346. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|------------------------------|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |

1.3.425 SC0_CLK (continued)

Table 1-346. Bit field encoding: MX_CLK_ENUM

| | | |
|------|----------|---|
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.426 SC0_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_BST: 0x40005A0C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------------|------------|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:000 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | bst_clk_en | mx_bst_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 3 | bst_clk_en | Clock gating control See Table 1-347. |
| 2:0 | mx_bst_clk[2:0] | Clock Selection See Table 1-348. |

Table 1-347. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-348. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.427 SC1_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW0: 0x40005A10

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vin_ag7 | vin_ag6 | vin_ag5 | vin_ag4 | vin_ag3 | vin_ag2 | vin_ag1 | vin_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 7 | vin_ag7 | Connect SC signal input VIN to analog global of same side See Table 1-349. |
| 6 | vin_ag6 | Connect SC signal input VIN to analog global of same side See Table 1-349. |
| 5 | vin_ag5 | Connect SC signal input VIN to analog global of same side See Table 1-349. |
| 4 | vin_ag4 | Connect SC signal input VIN to analog global of same side See Table 1-349. |
| 3 | vin_ag3 | Connect SC signal input VIN to analog global of same side See Table 1-349. |
| 2 | vin_ag2 | Connect SC signal input VIN to analog global of same side See Table 1-349. |
| 1 | vin_ag1 | Connect SC signal input VIN to analog global of same side See Table 1-349. |
| 0 | vin_ag0 | Connect SC signal input VIN to analog global of same side See Table 1-349. |

Table 1-349. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.428 SC1_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW2: 0x40005A12

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|-----------|------|-----------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | | | | R | R | NA | R |
| Name | | | | | vin_abus3 | vin_abus2 | | vin_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|--|
| 3 | vin_abus3 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-350. |
| 2 | vin_abus2 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-350. |
| 0 | vin_abus0 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-350. |

Table 1-350. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.429 SC1_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW3: 0x40005A13

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------------|--------|---|---|------------|---------|
| SW Access:Reset | NA:00 | | R/W:0 | NA:000 | | | R/W:0 | R/W:0 |
| HW Access | NA | | R | NA | | | R | R |
| Name | | | vref_bgvref | | | | vin_bgvref | vin_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|---|
| 5 | vref_bgvref | Connect SC signal input VREF to Bandgap Voltage Reference See Table 1-352. |
| 1 | vin_bgvref | Connect SC signal input VIN to Bandgap Voltage Reference See Table 1-352. |
| 0 | vin_amx | Connect SC signal input VIN to Analog Mux Bus See Table 1-351. |

Table 1-351. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-352. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

1.3.430 SC1_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW4: 0x40005A14

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|----------|------|----------|------|----------|------|----------|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | vref_ag6 | | vref_ag4 | | vref_ag2 | | vref_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|--|
| 6 | vref_ag6 | Connect SC signal input VREF to analog global of same side See Table 1-353. |
| 4 | vref_ag4 | Connect SC signal input VREF to analog global of same side See Table 1-353. |
| 2 | vref_ag2 | Connect SC signal input VREF to analog global of same side See Table 1-353. |
| 0 | vref_ag0 | Connect SC signal input VREF to analog global of same side See Table 1-353. |

Table 1-353. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.431 SC1_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW6: 0x40005A16

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|------------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | vref_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 0 | vref_abus0 | Connect SC signal input VREF to analog (local) bus of the same side See Table 1-354. |

Table 1-354. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.432 SC1_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW7: 0x40005A17

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|--------|-------|---|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:00 | |
| HW Access | NA | | | | | R/W | NA | |
| Name | | | | | | vin_vo | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 2 | vin_vo | Connect SC signal input VIN to VO of opposite SC See Table 1-355. |

Table 1-355. Bit field encoding: VIN_VO_ENUM

| Value | Name | Description |
|-------|----------|----------------------------------|
| 1'b0 | VIN_VO_0 | not connected |
| 1'b1 | VIN_VO_1 | Connect VIN to VO of opposite SC |

1.3.433 SC1_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW8: 0x40005A18

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|------|--------|------|--------|------|--------|------|
| SW Access:Reset | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | R | NA | R | NA | R | NA | R | NA |
| Name | vo_ag7 | | vo_ag5 | | vo_ag3 | | vo_ag1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vo_ag7 | Connect voltage output to analog global of same side (see field instance name) See Table 1-356. |
| 5 | vo_ag5 | Connect voltage output to analog global of same side (see field instance name) See Table 1-356. |
| 3 | vo_ag3 | Connect voltage output to analog global of same side (see field instance name) See Table 1-356. |
| 1 | vo_ag1 | Connect voltage output to analog global of same side (see field instance name) See Table 1-356. |

Table 1-356. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.434 SC1_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW10: 0x40005A1A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|------|----------|------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | NA | | | | R | NA | R | NA |
| Name | | | | | vo_abus3 | | vo_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 3 | vo_abus3 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-357. |
| 1 | vo_abus1 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-357. |

Table 1-357. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.435 SC1_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_CLK: 0x40005A1B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------------|-----------------|--------|---------|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | NA | | R/W | R | R | R | | |
| Name | | | dyn_cntl_en | bypass_syn c | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 5 | dyn_cntl_en | Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-360. |
| 4 | bypass_sync | Bypass Synchronization See Table 1-358. |
| 3 | clk_en | Clock gating control See Table 1-359. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-361. |

Table 1-358. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-359. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-360. Bit field encoding: DYN_CNTL_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | DYN_CNTL_DIS | Dynamic Control Disabled |
| 1'b1 | DYN_CNTL_EN | Dynamic Control Enabled |

Table 1-361. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|------------------------------|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |

1.3.435 SC1_CLK (continued)

Table 1-361. Bit field encoding: MX_CLK_ENUM

| | | |
|------|----------|---|
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.436 SC1_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_BST: 0x40005A1C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------------|------------|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:000 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | bst_clk_en | mx_bst_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 3 | bst_clk_en | Clock gating control See Table 1-362. |
| 2:0 | mx_bst_clk[2:0] | Clock Selection See Table 1-363. |

Table 1-362. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-363. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.437 SC2_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW0: 0x40005A20

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vin_ag7 | vin_ag6 | vin_ag5 | vin_ag4 | vin_ag3 | vin_ag2 | vin_ag1 | vin_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 7 | vin_ag7 | Connect SC signal input VIN to analog global of same side See Table 1-364. |
| 6 | vin_ag6 | Connect SC signal input VIN to analog global of same side See Table 1-364. |
| 5 | vin_ag5 | Connect SC signal input VIN to analog global of same side See Table 1-364. |
| 4 | vin_ag4 | Connect SC signal input VIN to analog global of same side See Table 1-364. |
| 3 | vin_ag3 | Connect SC signal input VIN to analog global of same side See Table 1-364. |
| 2 | vin_ag2 | Connect SC signal input VIN to analog global of same side See Table 1-364. |
| 1 | vin_ag1 | Connect SC signal input VIN to analog global of same side See Table 1-364. |
| 0 | vin_ag0 | Connect SC signal input VIN to analog global of same side See Table 1-364. |

Table 1-364. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.438 SC2_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW2: 0x40005A22

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|-----------|-----------|------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | NA:0 |
| HW Access | NA | | | | R | R | R | NA |
| Name | | | | | vin_abus3 | vin_abus2 | vin_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|--|
| 3 | vin_abus3 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-365. |
| 2 | vin_abus2 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-365. |
| 1 | vin_abus1 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-365. |

Table 1-365. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.439 SC2_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW3: 0x40005A23

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------------|--------|---|---|------------|---------|
| SW Access:Reset | NA:00 | | R/W:0 | NA:000 | | | R/W:0 | R/W:0 |
| HW Access | NA | | R | NA | | | R | R |
| Name | | | vref_bgvref | | | | vin_bgvref | vin_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|---|
| 5 | vref_bgvref | Connect SC signal input VREF to Bandgap Voltage Reference See Table 1-367. |
| 1 | vin_bgvref | Connect SC signal input VIN to Bandgap Voltage Reference See Table 1-367. |
| 0 | vin_amx | Connect SC signal input VIN to Analog Mux Bus See Table 1-366. |

Table 1-366. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-367. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

1.3.440 SC2_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW4: 0x40005A24

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|------|----------|------|----------|------|----------|------|
| SW Access:Reset | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | R | NA | R | NA | R | NA | R | NA |
| Name | vref_ag7 | | vref_ag5 | | vref_ag3 | | vref_ag1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|--|
| 7 | vref_ag7 | Connect SC signal input VREF to analog global of same side See Table 1-368. |
| 5 | vref_ag5 | Connect SC signal input VREF to analog global of same side See Table 1-368. |
| 3 | vref_ag3 | Connect SC signal input VREF to analog global of same side See Table 1-368. |
| 1 | vref_ag1 | Connect SC signal input VREF to analog global of same side See Table 1-368. |

Table 1-368. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.441 SC2_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW6: 0x40005A26

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|------------|------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | NA:0 |
| HW Access | NA | | | | | | R | NA |
| Name | | | | | | | vref_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 1 | vref_abus1 | Connect SC signal input VREF to analog (local) bus of the same side See Table 1-369. |

Table 1-369. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.442 SC2_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW7: 0x40005A27

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|--------|-------|---|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:00 | |
| HW Access | NA | | | | | R/W | NA | |
| Name | | | | | | vin_vo | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 2 | vin_vo | Connect SC signal input VIN to VO of opposite SC See Table 1-370. |

Table 1-370. Bit field encoding: VIN_VO_ENUM

| Value | Name | Description |
|-------|----------|----------------------------------|
| 1'b0 | VIN_VO_0 | not connected |
| 1'b1 | VIN_VO_1 | Connect VIN to VO of opposite SC |

1.3.443 SC2_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW8: 0x40005A28

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------|------|--------|------|--------|------|--------|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | vo_ag6 | | vo_ag4 | | vo_ag2 | | vo_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 6 | vo_ag6 | Connect voltage output to analog global of same side (see field instance name) See Table 1-371. |
| 4 | vo_ag4 | Connect voltage output to analog global of same side (see field instance name) See Table 1-371. |
| 2 | vo_ag2 | Connect voltage output to analog global of same side (see field instance name) See Table 1-371. |
| 0 | vo_ag0 | Connect voltage output to analog global of same side (see field instance name) See Table 1-371. |

Table 1-371. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.444 SC2_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW10: 0x40005A2A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|----------|------|----------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | | | | | R | NA | R |
| Name | | | | | | vo_abus2 | | vo_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 2 | vo_abus2 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-372. |
| 0 | vo_abus0 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-372. |

Table 1-372. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.445 SC2_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_CLK: 0x40005A2B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------------|-------------|--------|---------|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | NA | | R/W | R | R | R | | |
| Name | | | dyn_cntl_en | bypass_sync | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 5 | dyn_cntl_en | Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-375. |
| 4 | bypass_sync | Bypass Synchronization See Table 1-373. |
| 3 | clk_en | Clock gating control See Table 1-374. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-376. |

Table 1-373. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-374. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-375. Bit field encoding: DYN_CNTL_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | DYN_CNTL_DIS | Dynamic Control Disabled |
| 1'b1 | DYN_CNTL_EN | Dynamic Control Enabled |

Table 1-376. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|------------------------------|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |

1.3.445 SC2_CLK (continued)

Table 1-376. Bit field encoding: MX_CLK_ENUM

| | | |
|------|----------|---|
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.446 SC2_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_BST: 0x40005A2C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------------|------------|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:000 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | bst_clk_en | mx_bst_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 3 | bst_clk_en | Clock gating control See Table 1-377. |
| 2:0 | mx_bst_clk[2:0] | Clock Selection See Table 1-378. |

Table 1-377. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-378. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.447 SC3_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW0: 0x40005A30

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vin_ag7 | vin_ag6 | vin_ag5 | vin_ag4 | vin_ag3 | vin_ag2 | vin_ag1 | vin_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 7 | vin_ag7 | Connect SC signal input VIN to analog global of same side See Table 1-379. |
| 6 | vin_ag6 | Connect SC signal input VIN to analog global of same side See Table 1-379. |
| 5 | vin_ag5 | Connect SC signal input VIN to analog global of same side See Table 1-379. |
| 4 | vin_ag4 | Connect SC signal input VIN to analog global of same side See Table 1-379. |
| 3 | vin_ag3 | Connect SC signal input VIN to analog global of same side See Table 1-379. |
| 2 | vin_ag2 | Connect SC signal input VIN to analog global of same side See Table 1-379. |
| 1 | vin_ag1 | Connect SC signal input VIN to analog global of same side See Table 1-379. |
| 0 | vin_ag0 | Connect SC signal input VIN to analog global of same side See Table 1-379. |

Table 1-379. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.448 SC3_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW2: 0x40005A32

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|-----------|-----------|------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | NA:0 |
| HW Access | NA | | | | R | R | R | NA |
| Name | | | | | vin_abus3 | vin_abus2 | vin_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|--|
| 3 | vin_abus3 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-380. |
| 2 | vin_abus2 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-380. |
| 1 | vin_abus1 | Connect SC signal input VIN to analog (local) bus of the same side See Table 1-380. |

Table 1-380. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.449 SC3_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW3: 0x40005A33

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------------|--------|---|---|------------|---------|
| SW Access:Reset | NA:00 | | R/W:0 | NA:000 | | | R/W:0 | R/W:0 |
| HW Access | NA | | R | NA | | | R | R |
| Name | | | vref_bgvref | | | | vin_bgvref | vin_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|---|
| 5 | vref_bgvref | Connect SC signal input VREF to Bandgap Voltage Reference See Table 1-382. |
| 1 | vin_bgvref | Connect SC signal input VIN to Bandgap Voltage Reference See Table 1-382. |
| 0 | vin_amx | Connect SC signal input VIN to Analog Mux Bus See Table 1-381. |

Table 1-381. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-382. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

1.3.450 SC3_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW4: 0x40005A34

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|------|----------|------|----------|------|----------|------|
| SW Access:Reset | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | R | NA | R | NA | R | NA | R | NA |
| Name | vref_ag7 | | vref_ag5 | | vref_ag3 | | vref_ag1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|--|
| 7 | vref_ag7 | Connect SC signal input VREF to analog global of same side See Table 1-383. |
| 5 | vref_ag5 | Connect SC signal input VREF to analog global of same side See Table 1-383. |
| 3 | vref_ag3 | Connect SC signal input VREF to analog global of same side See Table 1-383. |
| 1 | vref_ag1 | Connect SC signal input VREF to analog global of same side See Table 1-383. |

Table 1-383. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.451 SC3_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW6: 0x40005A36

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|------------|------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | NA:0 |
| HW Access | NA | | | | | | R | NA |
| Name | | | | | | | vref_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 1 | vref_abus1 | Connect SC signal input VREF to analog (local) bus of the same side See Table 1-384. |

Table 1-384. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.452 SC3_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW7: 0x40005A37

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|--------|-------|---|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:00 | |
| HW Access | NA | | | | | R/W | NA | |
| Name | | | | | | vin_vo | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 2 | vin_vo | Connect SC signal input VIN to VO of opposite SC See Table 1-385. |

Table 1-385. Bit field encoding: VIN_VO_ENUM

| Value | Name | Description |
|-------|----------|----------------------------------|
| 1'b0 | VIN_VO_0 | not connected |
| 1'b1 | VIN_VO_1 | Connect VIN to VO of opposite SC |

1.3.453 SC3_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW8: 0x40005A38

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------|------|--------|------|--------|------|--------|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | vo_ag6 | | vo_ag4 | | vo_ag2 | | vo_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 6 | vo_ag6 | Connect voltage output to analog global of same side (see field instance name) See Table 1-386. |
| 4 | vo_ag4 | Connect voltage output to analog global of same side (see field instance name) See Table 1-386. |
| 2 | vo_ag2 | Connect voltage output to analog global of same side (see field instance name) See Table 1-386. |
| 0 | vo_ag0 | Connect voltage output to analog global of same side (see field instance name) See Table 1-386. |

Table 1-386. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.454 SC3_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW10: 0x40005A3A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|----------|------|----------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | | | | | R | NA | R |
| Name | | | | | | vo_abus2 | | vo_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 2 | vo_abus2 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-387. |
| 0 | vo_abus0 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-387. |

Table 1-387. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.455 SC3_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_CLK: 0x40005A3B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------------|-----------------|--------|---------|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | NA | | R/W | R | R | R | | |
| Name | | | dyn_cntl_en | bypass_syn c | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 5 | dyn_cntl_en | Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-390. |
| 4 | bypass_sync | Bypass Synchronization See Table 1-388. |
| 3 | clk_en | Clock gating control See Table 1-389. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-391. |

Table 1-388. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-389. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-390. Bit field encoding: DYN_CNTL_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | DYN_CNTL_DIS | Dynamic Control Disabled |
| 1'b1 | DYN_CNTL_EN | Dynamic Control Enabled |

Table 1-391. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|------------------------------|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |

1.3.455 SC3_CLK (continued)

Table 1-391. Bit field encoding: MX_CLK_ENUM

| | | |
|------|----------|---|
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.456 SC3_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_BST: 0x40005A3C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------------|------------|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:000 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | bst_clk_en | mx_bst_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 3 | bst_clk_en | Clock gating control See Table 1-392. |
| 2:0 | mx_bst_clk[2:0] | Clock Selection See Table 1-393. |

Table 1-392. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-393. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.457 DAC0_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW0: 0x40005A80

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|-------|-------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | v_ag1 | v_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 1 | v_ag1 | Connect voltage output to analog global of same side (see field instance name) See Table 1-394. |
| 0 | v_ag0 | Connect voltage output to analog global of same side (see field instance name) See Table 1-394. |

Table 1-394. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.458 DAC0_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW2: 0x40005A82

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|------|---------|------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | NA | | | | R | NA | R | NA |
| Name | | | | | v_abus3 | | v_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 3 | v_abus3 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-395. |
| 1 | v_abus1 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-395. |

Table 1-395. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.459 DAC0_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW3: 0x40005A83

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|---|-------|--------|---|---|-------|
| SW Access:Reset | R/W:0 | NA:00 | | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | R | NA | | R | NA | | | R |
| Name | iout | | | i_amx | | | | v_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 7 | iout | Connect current output to pad See Table 1-397. |
| 4 | i_amx | Connect current output to Analog Mux Bus See Table 1-396. |
| 0 | v_amx | Connect voltage output to Analog Mux Bus See Table 1-396. |

Table 1-396. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-397. Bit field encoding: IOOUT_ENUM

| Value | Name | Description |
|-------|---------------|--------------------------------------|
| 1'b0 | IOOUT_NC | not connected |
| 1'b1 | IOOUT_CONNECT | Connect to pad (see routing diagram) |

1.3.460 DAC0_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW4: 0x40005A84

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|-------|-------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | i_ag1 | i_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 1 | i_ag1 | Connect current output to analog global of same side (see field instance name) See Table 1-398. |
| 0 | i_ag0 | Connect current output to analog global of same side (see field instance name) See Table 1-398. |

Table 1-398. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.461 DAC0_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_STROBE: 0x40005A87

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|-----------|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:000 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | strobe_en | mx_strobe | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------------|---|
| 3 | strobe_en | Strobe gating control (See mx_strobe==3'h0) See Table 1-400. |
| 2:0 | mx_strobe[2:0] | Strobe source selection See Table 1-399. |

Table 1-399. Bit field encoding: MX_STROBE_ENUM

| Value | Name | Description |
|-------|--------------------------|---|
| 3'h0 | MX_STROBE_BUSWRI TE | Select bus write strobe source (Enable gater regardless of strobe_en setting) |
| 3'h1 | MX_STROBE_UDB_SR C | Select UDB strobe source |
| 3'h2 | MX_STROBE_NC_2 | NC |
| 3'h3 | MX_STROBE_NC_3 | NC |
| 3'h4 | MX_STROBE_CLK_A0_ DIG | Select clk_a0_dig |
| 3'h5 | MX_STROBE_CLK_A1_ DIG | Select clk_a1_dig |
| 3'h6 | MX_STROBE_CLK_A2_ DIG | Select clk_a2_dig |
| 3'h7 | MX_STROBE_CLK_A3_ DIG | Select clk_a3_dig |

Table 1-400. Bit field encoding: STROBE_EN_ENUM

| Value | Name | Description |
|-------|-------------|----------------|
| 1'b0 | STROBE_EN_0 | disable strobe |
| 1'b1 | STROBE_EN_1 | enable strobe |

1.3.462 DAC1_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW0: 0x40005A88

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|-------|-------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | v_ag1 | v_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 1 | v_ag1 | Connect voltage output to analog global of same side (see field instance name) See Table 1-401. |
| 0 | v_ag0 | Connect voltage output to analog global of same side (see field instance name) See Table 1-401. |

Table 1-401. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.463 DAC1_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW2: 0x40005A8A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|------|---------|------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | NA | | | | R | NA | R | NA |
| Name | | | | | v_abus3 | | v_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 3 | v_abus3 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-402. |
| 1 | v_abus1 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-402. |

Table 1-402. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.464 DAC1_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW3: 0x40005A8B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|---|-------|--------|---|---|-------|
| SW Access:Reset | R/W:0 | NA:00 | | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | R | NA | | R | NA | | | R |
| Name | iout | | | i_amx | | | | v_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 7 | iout | Connect current output to pad See Table 1-404. |
| 4 | i_amx | Connect current output to Analog Mux Bus See Table 1-403. |
| 0 | v_amx | Connect voltage output to Analog Mux Bus See Table 1-403. |

Table 1-403. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-404. Bit field encoding: IOUT_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------------------|
| 1'b0 | IOUT_NC | not connected |
| 1'b1 | IOUT_CONNECT | Connect to pad (see routing diagram) |

1.3.465 DAC1_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW4: 0x40005A8C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|-------|-------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | i_ag1 | i_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 1 | i_ag1 | Connect current output to analog global of same side (see field instance name) See Table 1-405. |
| 0 | i_ag0 | Connect current output to analog global of same side (see field instance name) See Table 1-405. |

Table 1-405. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.466 DAC1_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_STROBE: 0x40005A8F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|-----------|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:000 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | strobe_en | mx_strobe | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------------|---|
| 3 | strobe_en | Strobe gating control (See mx_strobe==3'h0) See Table 1-407. |
| 2:0 | mx_strobe[2:0] | Strobe source selection See Table 1-406. |

Table 1-406. Bit field encoding: MX_STROBE_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 3'h0 | MX_STROBE_BUSWRI | Select bus write strobe source (Enable gater regardless of strobe_en setting) |
| 3'h1 | MX_STROBE_UDB_SR | Select UDB strobe source |
| 3'h2 | MX_STROBE_NC_2 | NC |
| 3'h3 | MX_STROBE_NC_3 | NC |
| 3'h4 | MX_STROBE_CLK_A0_ | Select clk_a0_dig |
| 3'h5 | MX_STROBE_CLK_A1_ | Select clk_a1_dig |
| 3'h6 | MX_STROBE_CLK_A2_ | Select clk_a2_dig |
| 3'h7 | MX_STROBE_CLK_A3_ | Select clk_a3_dig |

Table 1-407. Bit field encoding: STROBE_EN_ENUM

| Value | Name | Description |
|-------|-------------|----------------|
| 1'b0 | STROBE_EN_0 | disable strobe |
| 1'b1 | STROBE_EN_1 | enable strobe |

1.3.467 DAC2_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW0: 0x40005A90

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------|-------|---------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | NA:0000 | | | |
| HW Access | NA | | R | R | NA | | | |
| Name | | | v_ag5 | v_ag4 | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 5 | v_ag5 | Connect voltage output to analog global of same side (see field instance name) See Table 1-408. |
| 4 | v_ag4 | Connect voltage output to analog global of same side (see field instance name) See Table 1-408. |

Table 1-408. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.468 DAC2_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW2: 0x40005A92

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|------|---------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | | | | | R | NA | R |
| Name | | | | | | v_abus2 | | v_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 2 | v_abus2 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-409. |
| 0 | v_abus0 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-409. |

Table 1-409. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.469 DAC2_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW3: 0x40005A93

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|---|-------|--------|---|---|-------|
| SW Access:Reset | R/W:0 | NA:00 | | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | R | NA | | R | NA | | | R |
| Name | iout | | | i_amx | | | | v_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 7 | iout | Connect current output to pad See Table 1-411. |
| 4 | i_amx | Connect current output to Analog Mux Bus See Table 1-410. |
| 0 | v_amx | Connect voltage output to Analog Mux Bus See Table 1-410. |

Table 1-410. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-411. Bit field encoding: IOOUT_ENUM

| Value | Name | Description |
|-------|---------------|--------------------------------------|
| 1'b0 | IOOUT_NC | not connected |
| 1'b1 | IOOUT_CONNECT | Connect to pad (see routing diagram) |

1.3.470 DAC2_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW4: 0x40005A94

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------|-------|---------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | NA:0000 | | | |
| HW Access | NA | | R | R | NA | | | |
| Name | | | i_ag5 | i_ag4 | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 5 | i_ag5 | Connect current output to analog global of same side (see field instance name) See Table 1-412. |
| 4 | i_ag4 | Connect current output to analog global of same side (see field instance name) See Table 1-412. |

Table 1-412. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.471 DAC2_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_STROBE: 0x40005A97

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|-----------|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:000 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | strobe_en | mx_strobe | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------------|---|
| 3 | strobe_en | Strobe gating control (See mx_strobe==3'h0) See Table 1-414. |
| 2:0 | mx_strobe[2:0] | Strobe source selection See Table 1-413. |

Table 1-413. Bit field encoding: MX_STROBE_ENUM

| Value | Name | Description |
|-------|--------------------------|---|
| 3'h0 | MX_STROBE_BUSWRI TE | Select bus write strobe source (Enable gater regardless of strobe_en setting) |
| 3'h1 | MX_STROBE_UDB_SR C | Select UDB strobe source |
| 3'h2 | MX_STROBE_NC_2 | NC |
| 3'h3 | MX_STROBE_NC_3 | NC |
| 3'h4 | MX_STROBE_CLK_A0_ DIG | Select clk_a0_dig |
| 3'h5 | MX_STROBE_CLK_A1_ DIG | Select clk_a1_dig |
| 3'h6 | MX_STROBE_CLK_A2_ DIG | Select clk_a2_dig |
| 3'h7 | MX_STROBE_CLK_A3_ DIG | Select clk_a3_dig |

Table 1-414. Bit field encoding: STROBE_EN_ENUM

| Value | Name | Description |
|-------|-------------|----------------|
| 1'b0 | STROBE_EN_0 | disable strobe |
| 1'b1 | STROBE_EN_1 | enable strobe |

1.3.472 DAC3_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW0: 0x40005A98

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------|-------|---------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | NA:0000 | | | |
| HW Access | NA | | R | R | NA | | | |
| Name | | | v_ag5 | v_ag4 | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 5 | v_ag5 | Connect voltage output to analog global of same side (see field instance name) See Table 1-415. |
| 4 | v_ag4 | Connect voltage output to analog global of same side (see field instance name) See Table 1-415. |

Table 1-415. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.473 DAC3_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW2: 0x40005A9A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|------|---------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | | | | | R | NA | R |
| Name | | | | | | v_abus2 | | v_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 2 | v_abus2 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-416. |
| 0 | v_abus0 | Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-416. |

Table 1-416. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.474 DAC3_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW3: 0x40005A9B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|---|-------|--------|---|---|-------|
| SW Access:Reset | R/W:0 | NA:00 | | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | R | NA | | R | NA | | | R |
| Name | iout | | | i_amx | | | | v_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 7 | iout | Connect current output to pad See Table 1-418. |
| 4 | i_amx | Connect current output to Analog Mux Bus See Table 1-417. |
| 0 | v_amx | Connect voltage output to Analog Mux Bus See Table 1-417. |

Table 1-417. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-418. Bit field encoding: IOUT_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------------------|
| 1'b0 | IOUT_NC | not connected |
| 1'b1 | IOUT_CONNECT | Connect to pad (see routing diagram) |

1.3.475 DAC3_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW4: 0x40005A9C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-------|-------|---------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | NA:0000 | | | |
| HW Access | NA | | R | R | NA | | | |
| Name | | | i_ag5 | i_ag4 | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|--|
| 5 | i_ag5 | Connect current output to analog global of same side (see field instance name) See Table 1-419. |
| 4 | i_ag4 | Connect current output to analog global of same side (see field instance name) See Table 1-419. |

Table 1-419. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.476 DAC3_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_STROBE: 0x40005A9F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|-----------|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:000 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | strobe_en | mx_strobe | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------------|---|
| 3 | strobe_en | Strobe gating control (See mx_strobe==3'h0) See Table 1-421. |
| 2:0 | mx_strobe[2:0] | Strobe source selection See Table 1-420. |

Table 1-420. Bit field encoding: MX_STROBE_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 3'h0 | MX_STROBE_BUSWRI | Select bus write strobe source (Enable gater regardless of strobe_en setting) |
| 3'h1 | MX_STROBE_UDB_SR | Select UDB strobe source |
| 3'h2 | MX_STROBE_NC_2 | NC |
| 3'h3 | MX_STROBE_NC_3 | NC |
| 3'h4 | MX_STROBE_CLK_A0_ | Select clk_a0_dig |
| 3'h5 | MX_STROBE_CLK_A1_ | Select clk_a1_dig |
| 3'h6 | MX_STROBE_CLK_A2_ | Select clk_a2_dig |
| 3'h7 | MX_STROBE_CLK_A3_ | Select clk_a3_dig |

Table 1-421. Bit field encoding: STROBE_EN_ENUM

| Value | Name | Description |
|-------|-------------|----------------|
| 1'b0 | STROBE_EN_0 | disable strobe |
| 1'b1 | STROBE_EN_1 | enable strobe |

1.3.477 CMP0_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW0: 0x40005AC0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|--------|--------|--------|--------|--------|--------|--------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vp_ag7 | vp_ag6 | vp_ag5 | vp_ag4 | vp_ag3 | vp_ag2 | vp_ag1 | vp_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vp_ag7 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-422. |
| 6 | vp_ag6 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-422. |
| 5 | vp_ag5 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-422. |
| 4 | vp_ag4 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-422. |
| 3 | vp_ag3 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-422. |
| 2 | vp_ag2 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-422. |
| 1 | vp_ag1 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-422. |
| 0 | vp_ag0 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-422. |

Table 1-422. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.478 CMP0_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW2: 0x40005AC2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|----------|----------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | vp_abus1 | vp_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 1 | vp_abus1 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-423. |
| 0 | vp_abus0 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-423. |

Table 1-423. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.479 CMP0_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW3: 0x40005AC3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|----------|----------|--------|-----------|-------|---|--------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:00 | | R/W:0 |
| HW Access | NA | R | R | R | R | NA | | R |
| Name | | vn_vref1 | vn_vref0 | vn_amx | vp_refbuf | | | vp_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|---|
| 6 | vn_vref1 | Connect negative voltage input to Voltage Reference 0 See Table 1-426. |
| 5 | vn_vref0 | Connect negative voltage input to Voltage Reference 1 See Table 1-426. |
| 4 | vn_amx | Connect negative voltage input to Analog Mux Bus See Table 1-424. |
| 3 | vp_refbuf | Connect positive voltage input to CapSense reference buffer channel See Table 1-425. |
| 0 | vp_amx | Connect positive voltage input to Analog Mux Bus See Table 1-424. |

Table 1-424. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-425. Bit field encoding: VP_REFBUF_ENUM

| Value | Name | Description |
|-------|-------------------|-------------|
| 1'b0 | VP_REFBUF_ENABLED | disable |
| 1'b1 | VP_REFBUF_DISABLE | enable |

Table 1-426. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

1.3.480 CMP0_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW4: 0x40005AC4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------|------|--------|------|--------|------|--------|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | vn_ag6 | | vn_ag4 | | vn_ag2 | | vn_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 6 | vn_ag6 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-427. |
| 4 | vn_ag4 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-427. |
| 2 | vn_ag2 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-427. |
| 0 | vn_ag0 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-427. |

Table 1-427. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.481 CMP0_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW6: 0x40005AC6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|----------|-------|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | NA:00 | |
| HW Access | NA | | | | R | R | NA | |
| Name | | | | | vn_abus3 | vn_abus2 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 3 | vn_abus3 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-428. |
| 2 | vn_abus2 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-428. |

Table 1-428. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.482 CMP0_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_CLK: 0x40005AC7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------------|--------|---------|---|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | NA | | | R | R | R | | |
| Name | | | | bypass_syn c | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 4 | bypass_sync | Bypass Synchronization See Table 1-429. |
| 3 | clk_en | Clock gating control See Table 1-430. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-431. |

Table 1-429. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-430. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-431. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.483 CMP1_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW0: 0x40005AC8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|--------|--------|--------|--------|--------|--------|--------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vp_ag7 | vp_ag6 | vp_ag5 | vp_ag4 | vp_ag3 | vp_ag2 | vp_ag1 | vp_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vp_ag7 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-432. |
| 6 | vp_ag6 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-432. |
| 5 | vp_ag5 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-432. |
| 4 | vp_ag4 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-432. |
| 3 | vp_ag3 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-432. |
| 2 | vp_ag2 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-432. |
| 1 | vp_ag1 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-432. |
| 0 | vp_ag0 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-432. |

Table 1-432. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.484 CMP1_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW2: 0x40005ACA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|----------|----------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | vp_abus1 | vp_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 1 | vp_abus1 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-433. |
| 0 | vp_abus0 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-433. |

Table 1-433. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.485 CMP1_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW3: 0x40005ACB

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|----------|----------|--------|-----------|-------|---|--------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:00 | | R/W:0 |
| HW Access | NA | R | R | R | R | NA | | R |
| Name | | vn_vref1 | vn_vref0 | vn_amx | vp_refbuf | | | vp_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|---|
| 6 | vn_vref1 | Connect negative voltage input to Voltage Reference 0 See Table 1-436. |
| 5 | vn_vref0 | Connect negative voltage input to Voltage Reference 1 See Table 1-436. |
| 4 | vn_amx | Connect negative voltage input to Analog Mux Bus See Table 1-434. |
| 3 | vp_refbuf | Connect positive voltage input to CapSense reference buffer channel See Table 1-435. |
| 0 | vp_amx | Connect positive voltage input to Analog Mux Bus See Table 1-434. |

Table 1-434. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-435. Bit field encoding: VP_REFBUF_ENUM

| Value | Name | Description |
|-------|-------------------|-------------|
| 1'b0 | VP_REFBUF_ENABLED | disable |
| 1'b1 | VP_REFBUF_DISABLE | enable |

Table 1-436. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

1.3.486 CMP1_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW4: 0x40005ACC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------|------|--------|------|--------|------|--------|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | vn_ag6 | | vn_ag4 | | vn_ag2 | | vn_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 6 | vn_ag6 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-437. |
| 4 | vn_ag4 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-437. |
| 2 | vn_ag2 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-437. |
| 0 | vn_ag0 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-437. |

Table 1-437. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.487 CMP1_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW6: 0x40005ACE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|----------|-------|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | NA:00 | |
| HW Access | NA | | | | R | R | NA | |
| Name | | | | | vn_abus3 | vn_abus2 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 3 | vn_abus3 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-438. |
| 2 | vn_abus2 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-438. |

Table 1-438. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.488 CMP1_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_CLK: 0x40005ACF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------------|--------|---------|---|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | NA | | | R | R | R | | |
| Name | | | | bypass_syn c | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 4 | bypass_sync | Bypass Synchronization See Table 1-439. |
| 3 | clk_en | Clock gating control See Table 1-440. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-441. |

Table 1-439. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-440. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-441. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.489 CMP2_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW0: 0x40005AD0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|--------|--------|--------|--------|--------|--------|--------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vp_ag7 | vp_ag6 | vp_ag5 | vp_ag4 | vp_ag3 | vp_ag2 | vp_ag1 | vp_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vp_ag7 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-442. |
| 6 | vp_ag6 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-442. |
| 5 | vp_ag5 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-442. |
| 4 | vp_ag4 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-442. |
| 3 | vp_ag3 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-442. |
| 2 | vp_ag2 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-442. |
| 1 | vp_ag1 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-442. |
| 0 | vp_ag0 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-442. |

Table 1-442. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.490 CMP2_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW2: 0x40005AD2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|----------|----------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | vp_abus1 | vp_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 1 | vp_abus1 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-443. |
| 0 | vp_abus0 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-443. |

Table 1-443. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.491 CMP2_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW3: 0x40005AD3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|----------|----------|--------|-----------|-------|---|--------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:00 | | R/W:0 |
| HW Access | NA | R | R | R | R | NA | | R |
| Name | | vn_vref1 | vn_vref0 | vn_amx | vp_refbuf | | | vp_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|---|
| 6 | vn_vref1 | Connect negative voltage input to Voltage Reference 0 See Table 1-446. |
| 5 | vn_vref0 | Connect negative voltage input to Voltage Reference 1 See Table 1-446. |
| 4 | vn_amx | Connect negative voltage input to Analog Mux Bus See Table 1-444. |
| 3 | vp_refbuf | Connect positive voltage input to CapSense reference buffer channel See Table 1-445. |
| 0 | vp_amx | Connect positive voltage input to Analog Mux Bus See Table 1-444. |

Table 1-444. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-445. Bit field encoding: VP_REFBUF_ENUM

| Value | Name | Description |
|-------|-------------------|-------------|
| 1'b0 | VP_REFBUF_ENABLED | disable |
| 1'b1 | VP_REFBUF_DISABLE | enable |

Table 1-446. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

1.3.492 CMP2_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW4: 0x40005AD4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|------|--------|------|--------|------|--------|------|
| SW Access:Reset | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | R | NA | R | NA | R | NA | R | NA |
| Name | vn_ag7 | | vn_ag5 | | vn_ag3 | | vn_ag1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vn_ag7 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-447. |
| 5 | vn_ag5 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-447. |
| 3 | vn_ag3 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-447. |
| 1 | vn_ag1 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-447. |

Table 1-447. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.493 CMP2_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW6: 0x40005AD6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|----------|-------|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | NA:00 | |
| HW Access | NA | | | | R | R | NA | |
| Name | | | | | vn_abus3 | vn_abus2 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 3 | vn_abus3 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-448. |
| 2 | vn_abus2 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-448. |

Table 1-448. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.494 CMP2_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_CLK: 0x40005AD7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------------|--------|---------|---|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | NA | | | R | R | R | | |
| Name | | | | bypass_syn c | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 4 | bypass_sync | Bypass Synchronization See Table 1-449. |
| 3 | clk_en | Clock gating control See Table 1-450. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-451. |

Table 1-449. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-450. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-451. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.495 CMP3_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW0: 0x40005AD8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|--------|--------|--------|--------|--------|--------|--------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vp_ag7 | vp_ag6 | vp_ag5 | vp_ag4 | vp_ag3 | vp_ag2 | vp_ag1 | vp_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vp_ag7 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-452. |
| 6 | vp_ag6 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-452. |
| 5 | vp_ag5 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-452. |
| 4 | vp_ag4 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-452. |
| 3 | vp_ag3 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-452. |
| 2 | vp_ag2 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-452. |
| 1 | vp_ag1 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-452. |
| 0 | vp_ag0 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-452. |

Table 1-452. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.496 CMP3_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW2: 0x40005ADA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|----------|----------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | vp_abus1 | vp_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 1 | vp_abus1 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-453. |
| 0 | vp_abus0 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-453. |

Table 1-453. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.497 CMP3_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW3: 0x40005ADB

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|----------|----------|--------|-----------|-------|---|--------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:00 | | R/W:0 |
| HW Access | NA | R | R | R | R | NA | | R |
| Name | | vn_vref1 | vn_vref0 | vn_amx | vp_refbuf | | | vp_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|---|
| 6 | vn_vref1 | Connect negative voltage input to Voltage Reference 0 See Table 1-456. |
| 5 | vn_vref0 | Connect negative voltage input to Voltage Reference 1 See Table 1-456. |
| 4 | vn_amx | Connect negative voltage input to Analog Mux Bus See Table 1-454. |
| 3 | vp_refbuf | Connect positive voltage input to CapSense reference buffer channel See Table 1-455. |
| 0 | vp_amx | Connect positive voltage input to Analog Mux Bus See Table 1-454. |

Table 1-454. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-455. Bit field encoding: VP_REFBUF_ENUM

| Value | Name | Description |
|-------|-------------------|-------------|
| 1'b0 | VP_REFBUF_ENABLED | disable |
| 1'b1 | VP_REFBUF_DISABLE | enable |

Table 1-456. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

1.3.498 CMP3_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW4: 0x40005ADC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|------|--------|------|--------|------|--------|------|
| SW Access:Reset | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | R | NA | R | NA | R | NA | R | NA |
| Name | vn_ag7 | | vn_ag5 | | vn_ag3 | | vn_ag1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vn_ag7 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-457. |
| 5 | vn_ag5 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-457. |
| 3 | vn_ag3 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-457. |
| 1 | vn_ag1 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-457. |

Table 1-457. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.499 CMP3_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW6: 0x40005ADE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|----------|-------|---|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | NA:00 | |
| HW Access | NA | | | | R | R | NA | |
| Name | | | | | vn_abus3 | vn_abus2 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 3 | vn_abus3 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-458. |
| 2 | vn_abus2 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-458. |

Table 1-458. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.500 CMP3_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_CLK: 0x40005ADF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------------|--------|---------|---|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | NA | | | R | R | R | | |
| Name | | | | bypass_syn c | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 4 | bypass_sync | Bypass Synchronization See Table 1-459. |
| 3 | clk_en | Clock gating control See Table 1-460. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-461. |

Table 1-459. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-460. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-461. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.501 DSM0_SW0

Delta Sigma Modulator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW0: 0x40005B00

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|--------|--------|--------|--------|--------|--------|--------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vp_ag7 | vp_ag6 | vp_ag5 | vp_ag4 | vp_ag3 | vp_ag2 | vp_ag1 | vp_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vp_ag7 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-462. |
| 6 | vp_ag6 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-462. |
| 5 | vp_ag5 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-462. |
| 4 | vp_ag4 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-462. |
| 3 | vp_ag3 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-462. |
| 2 | vp_ag2 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-462. |
| 1 | vp_ag1 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-462. |
| 0 | vp_ag0 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-462. |

Table 1-462. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.502 DSM0_SW2

Delta Sigma Modulator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW2: 0x40005B02

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|----------|------|----------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | | | | | R | NA | R |
| Name | | | | | | vp_abus2 | | vp_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 2 | vp_abus2 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-463. |
| 0 | vp_abus0 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-463. |

Table 1-463. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.503 DSM0_SW3

Delta Sigma Modulator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW3: 0x40005B03

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---------|-------|---|---------|------|--------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | NA:00 | | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | R | NA | | R | NA | R |
| Name | | vn_vssa | vn_vref | | | vp_vssa | | vp_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 6 | vn_vssa | Connect negative voltage input to vssa See Table 1-466. |
| 5 | vn_vref | Connect negative voltage input to Voltage Reference See Table 1-465. |
| 2 | vp_vssa | Connect positive voltage input to vssa See Table 1-466. |
| 0 | vp_amx | Connect positive voltage input to Analog Mux Bus See Table 1-464. |

Table 1-464. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-465. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

Table 1-466. Bit field encoding: VSSA_ENUM

| Value | Name | Description |
|-------|----------------|-----------------|
| 1'b0 | VSSA_NC | not connected |
| 1'b1 | VSSA_CONNECTED | Connect to vssa |

1.3.504 DSM0_SW4

Delta Sigma Modulator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW4: 0x40005B04

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|------|--------|------|--------|------|--------|------|
| SW Access:Reset | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | R | NA | R | NA | R | NA | R | NA |
| Name | vn_ag7 | | vn_ag5 | | vn_ag3 | | vn_ag1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vn_ag7 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-467. |
| 5 | vn_ag5 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-467. |
| 3 | vn_ag3 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-467. |
| 1 | vn_ag1 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-467. |

Table 1-467. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.505 DSM0_SW6

Delta Sigma Modulator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW6: 0x40005B06

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|------|----------|------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | NA | | | | R | NA | R | NA |
| Name | | | | | vn_abus3 | | vn_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 3 | vn_abus3 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-468. |
| 1 | vn_abus1 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-468. |

Table 1-468. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.506 DSM0_CLK

Delta Sigma Modulator Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CLK: 0x40005B07

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------------|--------|---------|---|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | NA | | | R | R | R | | |
| Name | | | | bypass_syn c | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 4 | bypass_sync | Bypass Synchronization See Table 1-469. |
| 3 | clk_en | Clock gating control See Table 1-470. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-471. |

Table 1-469. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-470. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-471. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |
| 3'h7 | MX_CLK_7 | Reserved |

1.3.507 SAR0_SW0

SAR Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_SW0: 0x40005B20

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|--------|--------|--------|--------|--------|--------|--------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vp_ag7 | vp_ag6 | vp_ag5 | vp_ag4 | vp_ag3 | vp_ag2 | vp_ag1 | vp_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vp_ag7 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-472. |
| 6 | vp_ag6 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-472. |
| 5 | vp_ag5 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-472. |
| 4 | vp_ag4 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-472. |
| 3 | vp_ag3 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-472. |
| 2 | vp_ag2 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-472. |
| 1 | vp_ag1 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-472. |
| 0 | vp_ag0 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-472. |

Table 1-472. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.508 SAR0_SW2

SAR Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_SW2: 0x40005B22

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|----------|------|----------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | | | | | R | NA | R |
| Name | | | | | | vp_abus2 | | vp_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 2 | vp_abus2 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-473. |
| 0 | vp_abus0 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-473. |

Table 1-473. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.509 SAR0_SW3

SAR Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_SW3: 0x40005B23

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---------|--------|------|---------|------|--------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | R | R | NA | R | NA | R |
| Name | | vn_vssa | vn_vref | vn_amx | | vp_vssa | | vp_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 6 | vn_vssa | Connect negative voltage input to vssa See Table 1-476. |
| 5 | vn_vref | Connect negative voltage input to Voltage Reference See Table 1-475. |
| 4 | vn_amx | Connect negative voltage input to Analog Mux Bus See Table 1-474. |
| 2 | vp_vssa | Connect positive voltage input to vssa See Table 1-476. |
| 0 | vp_amx | Connect positive voltage input to Analog Mux Bus See Table 1-474. |

Table 1-474. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-475. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

Table 1-476. Bit field encoding: VSSA_ENUM

| Value | Name | Description |
|-------|----------------|-----------------|
| 1'b0 | VSSA_NC | not connected |
| 1'b1 | VSSA_CONNECTED | Connect to vssa |

1.3.510 SAR0_SW4

SAR Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_SW4: 0x40005B24

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------|------|--------|------|--------|------|--------|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | vn_ag6 | | vn_ag4 | | vn_ag2 | | vn_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 6 | vn_ag6 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-477. |
| 4 | vn_ag4 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-477. |
| 2 | vn_ag2 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-477. |
| 0 | vn_ag0 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-477. |

Table 1-477. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.511 SAR0_SW6

SAR Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_SW6: 0x40005B26

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|------|----------|------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | NA | | | | R | NA | R | NA |
| Name | | | | | vn_abus3 | | vn_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 3 | vn_abus3 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-478. |
| 1 | vn_abus1 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-478. |

Table 1-478. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.512 SAR0_CLK

SAR Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CLK: 0x40005B27

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|-------------|--------|---------|---|---|
| SW Access:Reset | R/W:000 | | | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | R | | | R | R | R | | |
| Name | mx_pumpclk | | | bypass_sync | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 7:5 | mx_pumpclk[2:0] | Pump Clock Selection See Table 1-482. |
| 4 | bypass_sync | Bypass Synchronization See Table 1-479. |
| 3 | clk_en | Clock gating control See Table 1-480. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-481. |

Table 1-479. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-480. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-481. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |

1.3.512 SAR0_CLK (continued)

Table 1-481. Bit field encoding: MX_CLK_ENUM

| | | |
|------|----------|----------|
| 3'h7 | MX_CLK_7 | Reserved |
|------|----------|----------|

Table 1-482. Bit field encoding: MX_PUMPCLK_ENUM

| Value | Name | Description |
|-------|--------------|------------------------------|
| 3'h0 | MX_PUMPCLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_PUMPCLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_PUMPCLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_PUMPCLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_PUMPCLK_4 | Select UDB generated clock |
| 3'h5 | MX_PUMPCLK_5 | Reserved |
| 3'h6 | MX_PUMPCLK_6 | Reserved |
| 3'h7 | MX_PUMPCLK_7 | Reserved |

1.3.513 SAR1_SW0

SAR Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_SW0: 0x40005B28

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|--------|--------|--------|--------|--------|--------|--------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | vp_ag7 | vp_ag6 | vp_ag5 | vp_ag4 | vp_ag3 | vp_ag2 | vp_ag1 | vp_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 7 | vp_ag7 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-483. |
| 6 | vp_ag6 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-483. |
| 5 | vp_ag5 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-483. |
| 4 | vp_ag4 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-483. |
| 3 | vp_ag3 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-483. |
| 2 | vp_ag2 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-483. |
| 1 | vp_ag1 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-483. |
| 0 | vp_ag0 | Connect positive voltage input to analog global of same side (see field instance name) See Table 1-483. |

Table 1-483. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.514 SAR1_SW2

SAR Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_SW2: 0x40005B2A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|----------|------|----------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | | | | | R | NA | R |
| Name | | | | | | vp_abus2 | | vp_abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 2 | vp_abus2 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-484. |
| 0 | vp_abus0 | Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-484. |

Table 1-484. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.515 SAR1_SW3

SAR Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_SW3: 0x40005B2B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---------|--------|------|---------|------|--------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | R | R | NA | R | NA | R |
| Name | | vn_vssa | vn_vref | vn_amx | | vp_vssa | | vp_amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 6 | vn_vssa | Connect negative voltage input to vssa See Table 1-487. |
| 5 | vn_vref | Connect negative voltage input to Voltage Reference See Table 1-486. |
| 4 | vn_amx | Connect negative voltage input to Analog Mux Bus See Table 1-485. |
| 2 | vp_vssa | Connect positive voltage input to vssa See Table 1-487. |
| 0 | vp_amx | Connect positive voltage input to Analog Mux Bus See Table 1-485. |

Table 1-485. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | AMX_NC | not connected |
| 1'b1 | AMX_CONNECTED | Connect to AMUXBUS |

Table 1-486. Bit field encoding: VREF_ENUM

| Value | Name | Description |
|-------|----------------|------------------------------|
| 1'b0 | VREF_NC | not connected |
| 1'b1 | VREF_CONNECTED | Connect to Voltage Reference |

Table 1-487. Bit field encoding: VSSA_ENUM

| Value | Name | Description |
|-------|----------------|-----------------|
| 1'b0 | VSSA_NC | not connected |
| 1'b1 | VSSA_CONNECTED | Connect to vssa |

1.3.516 SAR1_SW4

SAR Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_SW4: 0x40005B2C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------|------|--------|------|--------|------|--------|
| SW Access:Reset | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | vn_ag6 | | vn_ag4 | | vn_ag2 | | vn_ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------|--|
| 6 | vn_ag6 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-488. |
| 4 | vn_ag4 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-488. |
| 2 | vn_ag2 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-488. |
| 0 | vn_ag0 | Connect negative voltage input to analog global of same side (see field instance name) See Table 1-488. |

Table 1-488. Bit field encoding: AG_ENUM

| Value | Name | Description |
|-------|--------------|--------------------------|
| 1'b0 | AG_NC | not connected |
| 1'b1 | AG_CONNECTED | Connect to Analog Global |

1.3.517 SAR1_SW6

SAR Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_SW6: 0x40005B2E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|------|----------|------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | NA:0 | R/W:0 | NA:0 |
| HW Access | NA | | | | R | NA | R | NA |
| Name | | | | | vn_abus3 | | vn_abus1 | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|---|
| 3 | vn_abus3 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-489. |
| 1 | vn_abus1 | Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-489. |

Table 1-489. Bit field encoding: ABUS_ENUM

| Value | Name | Description |
|-------|----------------|-------------------------------|
| 1'b0 | ABUS_NC | not connected |
| 1'b1 | ABUS_CONNECTED | Connect to Analog (local) Bus |

1.3.518 SAR1_CLK

SAR Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_CLK: 0x40005B2F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|-----------------|--------|---------|---|---|
| SW Access:Reset | R/W:000 | | | R/W:0 | R/W:0 | R/W:000 | | |
| HW Access | R | | | R | R | R | | |
| Name | mx_pumpclk | | | bypass_syn c | clk_en | mx_clk | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 7:5 | mx_pumpclk[2:0] | Pump Clock Selection See Table 1-493. |
| 4 | bypass_sync | Bypass Synchronization See Table 1-490. |
| 3 | clk_en | Clock gating control See Table 1-491. |
| 2:0 | mx_clk[2:0] | Clock Selection See Table 1-492. |

Table 1-490. Bit field encoding: BYPASS_SYNC_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 1'b0 | BYPASS_SYNC_0 | Synchronization not bypassed (Synchronization enabled) |
| 1'b1 | BYPASS_SYNC_1 | Synchronization bypassed (Synchronization disabled) |

Table 1-491. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|----------|---------------|
| 1'b0 | CLK_EN_0 | disable clock |
| 1'b1 | CLK_EN_1 | enable clock |

Table 1-492. Bit field encoding: MX_CLK_ENUM

| Value | Name | Description |
|-------|----------|---|
| 3'h0 | MX_CLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_CLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_CLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_CLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_CLK_4 | Select UDB generated clock. Per IROS - System timing with the UDB generated clock is not supported by default and should involve engineering to use |
| 3'h5 | MX_CLK_5 | Reserved |
| 3'h6 | MX_CLK_6 | Reserved |

1.3.518 SAR1_CLK (continued)

Table 1-492. Bit field encoding: MX_CLK_ENUM

| | | |
|------|----------|----------|
| 3'h7 | MX_CLK_7 | Reserved |
|------|----------|----------|

Table 1-493. Bit field encoding: MX_PUMPCLK_ENUM

| Value | Name | Description |
|-------|--------------|------------------------------|
| 3'h0 | MX_PUMPCLK_0 | Select clk_a0 and clk_a0_dig |
| 3'h1 | MX_PUMPCLK_1 | Select clk_a1 and clk_a1_dig |
| 3'h2 | MX_PUMPCLK_2 | Select clk_a2 and clk_a2_dig |
| 3'h3 | MX_PUMPCLK_3 | Select clk_a3 and clk_a3_dig |
| 3'h4 | MX_PUMPCLK_4 | Select UDB generated clock |
| 3'h5 | MX_PUMPCLK_5 | Reserved |
| 3'h6 | MX_PUMPCLK_6 | Reserved |
| 3'h7 | MX_PUMPCLK_7 | Reserved |

1.3.519 OPAMP0_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_MX: 0x40005B40

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|---|----------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:00 | | R/W:0000 | | | |
| HW Access | NA | | R | | R | | | |
| Name | | | mx_vn | | mx_vp | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 5:4 | mx_vn[1:0] | Mux Select VN See Table 1-494. |
| 3:0 | mx_vp[3:0] | Mux Select VP See Table 1-495. |

Table 1-494. Bit field encoding: OPAMP0_MX_VN_ENUM

| Value | Name | Description |
|-------|------------------|--------------------------------------|
| 2'h0 | OPAMP0_MX_VN_DEF | Default - Not Connected (NC) AULT |
| 2'h1 | OPAMP0_MX_VN_AG4 | Mux Selection AGL[4] |
| 2'h2 | OPAMP0_MX_VN_AG6 | Mux Selection AGL[6] |
| 2'h3 | OPAMP0_MX_VN_0x3 | Reserved (NC) |

Table 1-495. Bit field encoding: OPAMP0_MX_VP_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 4'h0 | OPAMP0_MX_VP_DEF | Default - Not Connected (NC) AULT |
| 4'h1 | OPAMP0_MX_VP_AG4 | Mux Selection: AGL[4] |
| 4'h2 | OPAMP0_MX_VP_AG5 | Mux Selection: AGL[5] |
| 4'h3 | OPAMP0_MX_VP_AG6 | Mux Selection: AGL[6] |
| 4'h4 | OPAMP0_MX_VP_AG7 | Mux Selection: AGL[7] |
| 4'h5 | OPAMP0_MX_VP_ABU | Mux Selection: ABUSL[0] S0 |
| 4'h6 | OPAMP0_MX_VP_ABU | Mux Selection: ABUSL[1] S1 |
| 4'h7 | OPAMP0_MX_VP_ABU | Mux Selection: ABUSL[2] S2 |
| 4'h8 | OPAMP0_MX_VP_ABU | Mux Selection: ABUSL[3] S3 |
| 4'h9 | OPAMP0_MX_VP_VRE | Mux Selection: OPAMP Voltage Reference F |
| 4'ha | OPAMP0_MX_VP_H_0x | Reserved (NC) A |

1.3.519 OPAMP0_MX (continued)

Table 1-495. Bit field encoding: OPAMP0_MX_VP_ENUM

| | |
|------|---------------------------------|
| 4'hb | OPAMP0_MX_VP_H_0x Reserved (NC) |
| | B |
| 4'hc | OPAMP0_MX_VP_H_0x Reserved (NC) |
| | C |
| 4'hd | OPAMP0_MX_VP_H_0x Reserved (NC) |
| | D |
| 4'he | OPAMP0_MX_VP_H_0x Reserved (NC) |
| | E |
| 4'hf | OPAMP0_MX_VP_H_0x Reserved (NC) |
| | F |

1.3.520 OPAMP0_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_SW: 0x40005B41

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|-------|-------|-------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | swinp | swinn | swfol |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|------------------------------|
| 2 | swinp | Switch Enable Positive Input |
| 1 | swinn | Switch Enable Negative Input |
| 0 | swfol | Switch Enable Follow |

1.3.521 OPAMP1_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP1_MX: 0x40005B42

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|---|----------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:00 | | R/W:0000 | | | |
| HW Access | NA | | R | | R | | | |
| Name | | | mx_vn | | mx_vp | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 5:4 | mx_vn[1:0] | Mux Select VN See Table 1-496. |
| 3:0 | mx_vp[3:0] | Mux Select VP See Table 1-497. |

Table 1-496. Bit field encoding: OPAMP1_MX_VN_ENUM

| Value | Name | Description |
|-------|------------------|--------------------------------------|
| 2'h0 | OPAMP1_MX_VN_DEF | Default - Not Connected (NC) AULT |
| 2'h1 | OPAMP1_MX_VN_AG4 | Mux Selection AGR[4] |
| 2'h2 | OPAMP1_MX_VN_AG6 | Mux Selection AGR[6] |
| 2'h3 | OPAMP1_MX_VN_0x3 | Reserved (NC) |

Table 1-497. Bit field encoding: OPAMP1_MX_VP_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 4'h0 | OPAMP1_MX_VP_DEF | Default - Not Connected (NC) AULT |
| 4'h1 | OPAMP1_MX_VP_AG4 | Mux Selection: AGR[4] |
| 4'h2 | OPAMP1_MX_VP_AG5 | Mux Selection: AGR[5] |
| 4'h3 | OPAMP1_MX_VP_AG6 | Mux Selection: AGR[6] |
| 4'h4 | OPAMP1_MX_VP_AG7 | Mux Selection: AGR[7] |
| 4'h5 | OPAMP1_MX_VP_ABU | Mux Selection: ABUSR[0] S0 |
| 4'h6 | OPAMP1_MX_VP_ABU | Mux Selection: ABUSR[1] S1 |
| 4'h7 | OPAMP1_MX_VP_ABU | Mux Selection: ABUSR[2] S2 |
| 4'h8 | OPAMP1_MX_VP_ABU | Mux Selection: ABUSR[3] S3 |
| 4'h9 | OPAMP1_MX_VP_VRE | Mux Selection: OPAMP Voltage Reference F |
| 4'ha | OPAMP1_MX_VP_H_0x | Reserved (NC) A |

1.3.521 OPAMP1_MX (continued)

Table 1-497. Bit field encoding: OPAMP1_MX_VP_ENUM

| | |
|------|--------------------------------------|
| 4'hb | OPAMP1_MX_VP_H_0x Reserved (NC) B |
| 4'hc | OPAMP1_MX_VP_H_0x Reserved (NC) C |
| 4'hd | OPAMP1_MX_VP_H_0x Reserved (NC) D |
| 4'he | OPAMP1_MX_VP_H_0x Reserved (NC) E |
| 4'hf | OPAMP1_MX_VP_H_0x Reserved (NC) F |

1.3.522 OPAMP1_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP1_SW: 0x40005B43

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|-------|-------|-------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | swinp | swinn | swfol |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|------------------------------|
| 2 | swinp | Switch Enable Positive Input |
| 1 | swinn | Switch Enable Negative Input |
| 0 | swfol | Switch Enable Follow |

1.3.523 OPAMP2_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP2_MX: 0x40005B44

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|---|----------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:00 | | R/W:0000 | | | |
| HW Access | NA | | R | | R | | | |
| Name | | | mx_vn | | mx_vp | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 5:4 | mx_vn[1:0] | Mux Select VN See Table 1-498. |
| 3:0 | mx_vp[3:0] | Mux Select VP See Table 1-499. |

Table 1-498. Bit field encoding: OPAMP2_MX_VN_ENUM

| Value | Name | Description |
|-------|------------------|------------------------------|
| 2'h0 | OPAMP2_MX_VN_DEF | Default - Not Connected (NC) |
| | AULT | |
| 2'h1 | OPAMP2_MX_VN_AG5 | Mux Selection AGL[5] |
| 2'h2 | OPAMP2_MX_VN_AG7 | Mux Selection AGL[7] |
| 2'h3 | OPAMP2_MX_VN_0x3 | Reserved (NC) |

Table 1-499. Bit field encoding: OPAMP2_MX_VP_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 4'h0 | OPAMP2_MX_VP_DEF | Default - Not Connected (NC) |
| | AULT | |
| 4'h1 | OPAMP2_MX_VP_AG4 | Mux Selection: AGL[4] |
| 4'h2 | OPAMP2_MX_VP_AG5 | Mux Selection: AGL[5] |
| 4'h3 | OPAMP2_MX_VP_AG6 | Mux Selection: AGL[6] |
| 4'h4 | OPAMP2_MX_VP_AG7 | Mux Selection: AGL[7] |
| 4'h5 | OPAMP2_MX_VP_ABU | Mux Selection: ABUSL[0] |
| | S0 | |
| 4'h6 | OPAMP2_MX_VP_ABU | Mux Selection: ABUSL[1] |
| | S1 | |
| 4'h7 | OPAMP2_MX_VP_ABU | Mux Selection: ABUSL[2] |
| | S2 | |
| 4'h8 | OPAMP2_MX_VP_ABU | Mux Selection: ABUSL[3] |
| | S3 | |
| 4'h9 | OPAMP2_MX_VP_VRE | Mux Selection: OPAMP Voltage Reference |
| | F | |
| 4'ha | OPAMP2_MX_VP_H_0x | Reserved (NC) |
| | A | |

1.3.523 OPAMP2_MX (continued)

Table 1-499. Bit field encoding: OPAMP2_MX_VP_ENUM

| | |
|------|---------------------------------|
| 4'hb | OPAMP2_MX_VP_H_0x Reserved (NC) |
| | B |
| 4'hc | OPAMP2_MX_VP_H_0x Reserved (NC) |
| | C |
| 4'hd | OPAMP2_MX_VP_H_0x Reserved (NC) |
| | D |
| 4'he | OPAMP2_MX_VP_H_0x Reserved (NC) |
| | E |
| 4'hf | OPAMP2_MX_VP_H_0x Reserved (NC) |
| | F |

1.3.524 OPAMP2_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP2_SW: 0x40005B45

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|-------|-------|-------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | swinp | swinn | swfol |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|------------------------------|
| 2 | swinp | Switch Enable Positive Input |
| 1 | swinn | Switch Enable Negative Input |
| 0 | swfol | Switch Enable Follow |

1.3.525 OPAMP3_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP3_MX: 0x40005B46

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|---|----------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:00 | | R/W:0000 | | | |
| HW Access | NA | | R | | R | | | |
| Name | | | mx_vn | | mx_vp | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|---|
| 5:4 | mx_vn[1:0] | Mux Select VN See Table 1-500. |
| 3:0 | mx_vp[3:0] | Mux Select VP See Table 1-501. |

Table 1-500. Bit field encoding: OPAMP3_MX_VN_ENUM

| Value | Name | Description |
|-------|------------------|--------------------------------------|
| 2'h0 | OPAMP3_MX_VN_DEF | Default - Not Connected (NC) AULT |
| 2'h1 | OPAMP3_MX_VN_AG5 | Mux Selection AGR[5] |
| 2'h2 | OPAMP3_MX_VN_AG7 | Mux Selection AGR[7] |
| 2'h3 | OPAMP3_MX_VN_0x3 | Reserved (NC) |

Table 1-501. Bit field encoding: OPAMP3_MX_VP_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 4'h0 | OPAMP3_MX_VP_DEF | Default - Not Connected (NC) AULT |
| 4'h1 | OPAMP3_MX_VP_AG4 | Mux Selection: AGR[4] |
| 4'h2 | OPAMP3_MX_VP_AG5 | Mux Selection: AGR[5] |
| 4'h3 | OPAMP3_MX_VP_AG6 | Mux Selection: AGR[6] |
| 4'h4 | OPAMP3_MX_VP_AG7 | Mux Selection: AGR[7] |
| 4'h5 | OPAMP3_MX_VP_ABU | Mux Selection: ABUSR[0] S0 |
| 4'h6 | OPAMP3_MX_VP_ABU | Mux Selection: ABUSR[1] S1 |
| 4'h7 | OPAMP3_MX_VP_ABU | Mux Selection: ABUSR[2] S2 |
| 4'h8 | OPAMP3_MX_VP_ABU | Mux Selection: ABUSR[3] S3 |
| 4'h9 | OPAMP3_MX_VP_VRE | Mux Selection: OPAMP Voltage Reference F |
| 4'ha | OPAMP3_MX_VP_H_0x | Reserved (NC) A |

1.3.525 OPAMP3_MX (continued)

Table 1-501. Bit field encoding: OPAMP3_MX_VP_ENUM

| | |
|------|--------------------------------------|
| 4'hb | OPAMP3_MX_VP_H_0x Reserved (NC) B |
| 4'hc | OPAMP3_MX_VP_H_0x Reserved (NC) C |
| 4'hd | OPAMP3_MX_VP_H_0x Reserved (NC) D |
| 4'he | OPAMP3_MX_VP_H_0x Reserved (NC) E |
| 4'hf | OPAMP3_MX_VP_H_0x Reserved (NC) F |

1.3.526 OPAMP3_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP3_SW: 0x40005B47

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|-------|-------|-------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | swinp | swinn | swfol |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|------------------------------|
| 2 | swinp | Switch Enable Positive Input |
| 1 | swinn | Switch Enable Negative Input |
| 0 | swfol | Switch Enable Follow |

1.3.527 LCDDAC_SW0

LCDDAC Switch Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW0: 0x40005B50

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|---|---|
| SW Access:Reset | NA:00000 | | | | | R/W:000 | | |
| HW Access | NA | | | | | R | | |
| Name | | | | | | sw0 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|------------------------------------|
| 2:0 | sw0[2:0] | Switch Control for LCD_BIAS_BUS[0] |
| | | See Table 1-502. |

Table 1-502. Bit field encoding: LCDDAC_SW0_ENUM

| Value | Name | Description |
|-------|--------------------------|--|
| 3'h0 | LCDDAC_SW0_NC | NC |
| 3'h1 | LCDDAC_SW0_LCDDA C_V0 | LCDDAC_V0 connected to LCD_BIAS_BUS[0] |
| 3'h2 | LCDDAC_SW0_ABUSR 0 | ABUSR[0] connected to LCD_BIAS_BUS[0] |
| 3'h3 | LCDDAC_SW0_3 | LCDDAC_V0 and ABUSR[0] connected to LCD_BIAS_BUS[0] |
| 3'h4 | LCDDAC_SW0_ABUSR 1 | ABUSR[1] connected to LCD_BIAS_BUS[0] |
| 3'h5 | LCDDAC_SW0_5 | LCDDAC_V0 and ABUSR[1] connected to LCD_BIAS_BUS[0] |
| 3'h6 | LCDDAC_SW0_6 | ABUSR[0] and ABUSR[1] connected to LCD_BIAS_BUS[0] |
| 3'h7 | LCDDAC_SW0_7 | LCDDAC_V0 and ABUSR[0] and ABUSR[1] connected to LCD_BIAS_BUS[0] |

1.3.528 LCDDAC_SW1

LCDDAC Switch Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW1: 0x40005B51

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|---|---|
| SW Access:Reset | NA:00000 | | | | | R/W:000 | | |
| HW Access | NA | | | | | R | | |
| Name | | | | | | sw1 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|--|
| 2:0 | sw1[2:0] | Switch Control for LCD_BIAS_BUS[1] See Table 1-503. |

Table 1-503. Bit field encoding: LCDDAC_SW1_ENUM

| Value | Name | Description |
|-------|--------------------------|--|
| 3'h0 | LCDDAC_SW1_NC | NC |
| 3'h1 | LCDDAC_SW1_LCDDA C_V1 | LCDDAC_V1 connected to LCD_BIAS_BUS[1] |
| 3'h2 | LCDDAC_SW1_ABUSL 0 | ABUSL[0] connected to LCD_BIAS_BUS[1] |
| 3'h3 | LCDDAC_SW1_3 | LCDDAC_V1 and ABUSL[0] connected to LCD_BIAS_BUS[1] |
| 3'h4 | LCDDAC_SW1_ABUSL 1 | ABUSL[1] connected to LCD_BIAS_BUS[1] |
| 3'h5 | LCDDAC_SW1_5 | LCDDAC_V1 and ABUSL[1] connected to LCD_BIAS_BUS[1] |
| 3'h6 | LCDDAC_SW1_6 | ABUSL[0] and ABUSL[1] connected to LCD_BIAS_BUS[1] |
| 3'h7 | LCDDAC_SW1_7 | LCDDAC_V1 and ABUSL[0] and ABUSL[1] connected to LCD_BIAS_BUS[1] |

1.3.529 LCDDAC_SW2

LCDDAC Switch Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW2: 0x40005B52

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|---|---|
| SW Access:Reset | NA:00000 | | | | | R/W:000 | | |
| HW Access | NA | | | | | R | | |
| Name | | | | | | sw2 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|------------------------------------|
| 2:0 | sw2[2:0] | Switch Control for LCD_BIAS_BUS[2] |
| | | See Table 1-504. |

Table 1-504. Bit field encoding: LCDDAC_SW2_ENUM

| Value | Name | Description |
|-------|--------------------------|--|
| 3'h0 | LCDDAC_SW2_NC | NC |
| 3'h1 | LCDDAC_SW2_LCDDA C_V2 | LCDDAC_V2 connected to LCD_BIAS_BUS[2] |
| 3'h2 | LCDDAC_SW2_ABUSR 2 | ABUSR[2] connected to LCD_BIAS_BUS[2] |
| 3'h3 | LCDDAC_SW2_3 | LCDDAC_V2 and ABUSR[2] connected to LCD_BIAS_BUS[2] |
| 3'h4 | LCDDAC_SW2_ABUSR 3 | ABUSR[3] connected to LCD_BIAS_BUS[2] |
| 3'h5 | LCDDAC_SW2_5 | LCDDAC_V2 and ABUSR[3] connected to LCD_BIAS_BUS[2] |
| 3'h6 | LCDDAC_SW2_6 | ABUSR[2] and ABUSR[3] connected to LCD_BIAS_BUS[2] |
| 3'h7 | LCDDAC_SW2_7 | LCDDAC_V2 and ABUSR[2] and ABUSR[3] connected to LCD_BIAS_BUS[2] |

1.3.530 LCDDAC_SW3

LCDDAC Switch Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW3: 0x40005B53

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|---|---|
| SW Access:Reset | NA:00000 | | | | | R/W:000 | | |
| HW Access | NA | | | | | R | | |
| Name | | | | | | sw3 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|--|
| 2:0 | sw3[2:0] | Switch Control for LCD_BIAS_BUS[3] See Table 1-505. |

Table 1-505. Bit field encoding: LCDDAC_SW3_ENUM

| Value | Name | Description |
|-------|--------------------------|--|
| 3'h0 | LCDDAC_SW3_NC | NC |
| 3'h1 | LCDDAC_SW3_LCDDA C_V3 | LCDDAC_V3 connected to LCD_BIAS_BUS[3] |
| 3'h2 | LCDDAC_SW3_ABUSL 2 | ABUSL[2] connected to LCD_BIAS_BUS[3] |
| 3'h3 | LCDDAC_SW3_3 | LCDDAC_V3 and ABUSL[2] connected to LCD_BIAS_BUS[3] |
| 3'h4 | LCDDAC_SW3_ABUSL 3 | ABUSL[3] connected to LCD_BIAS_BUS[3] |
| 3'h5 | LCDDAC_SW3_5 | LCDDAC_V3 and ABUSL[3] connected to LCD_BIAS_BUS[3] |
| 3'h6 | LCDDAC_SW3_6 | ABUSL[2] and ABUSL[3] connected to LCD_BIAS_BUS[3] |
| 3'h7 | LCDDAC_SW3_7 | LCDDAC_V3 and ABUSL[2] and ABUSL[3] connected to LCD_BIAS_BUS[3] |

1.3.531 LCDDAC_SW4

LCDDAC Switch Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW4: 0x40005B54

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|---|---|
| SW Access:Reset | NA:00000 | | | | | R/W:000 | | |
| HW Access | NA | | | | | R | | |
| Name | | | | | | sw4 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|------------------------------------|
| 2:0 | sw4[2:0] | Switch Control for LCD_BIAS_BUS[4] |

[See Table 1-506.](#)

Table 1-506. Bit field encoding: LCDDAC_SW4_ENUM

| Value | Name | Description |
|-------|--------------------------|--|
| 3'h0 | LCDDAC_SW4_NC | NC |
| 3'h1 | LCDDAC_SW4_LCDDA C_V4 | LCDDAC_V4 connected to LCD_BIAS_BUS[4] |
| 3'h2 | LCDDAC_SW4_AMUXB USR | AMUXBUSR connected to LCD_BIAS_BUS[4] |
| 3'h3 | LCDDAC_SW4_3 | LCDDAC_V4 and AMUXBUSR connected to LCD_BIAS_BUS[4] |
| 3'h4 | LCDDAC_SW4_AMUXB USL | AMUXBUSL connected to LCD_BIAS_BUS[4] |
| 3'h5 | LCDDAC_SW4_5 | LCDDAC_V4 and AMUXBUSL connected to LCD_BIAS_BUS[4] |
| 3'h6 | LCDDAC_SW4_6 | AMUXBUSR and AMUXBUSL connected to LCD_BIAS_BUS[4] |
| 3'h7 | LCDDAC_SW4_7 | LCDDAC_V4 and AMUXBUSR and AMUXBUSL connected to LCD_BIAS_BUS[4] |

1.3.532 SC_MISC

Switched Cap Miscellaneous Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_MISC: 0x40005B56

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------------|--------------|-------|---|--------------|--------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | NA:00 | | R/W:0 | R/W:0 |
| HW Access | NA | | R | R | NA | | R | R |
| Name | | | sc_pump_force | sc_pump_auto | | | diff_pga_1_3 | diff_pga_0_2 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------------|---|
| 5 | sc_pump_force | force pumping - if block enabled enable pump regardless of voltage state |
| 4 | sc_pump_auto | enable autopumping - if block enabled pump when low voltage detected |
| 1 | diff_pga_1_3 | Switched Cap Pair Connect for Differential Amplifier Applications See Table 1-507. |
| 0 | diff_pga_0_2 | Switched Cap Pair Connect for Differential Amplifier Applications See Table 1-507. |

Table 1-507. Bit field encoding: SC_DIFF_PGA_ENUM

| Value | Name | Description |
|-------|--------------------|--|
| 1'h0 | SC_DIFF_PGA_DISABL | Differential PGA pair connect disabled |
| 1'h1 | SC_DIFF_PGA_ENABL | Differential PGA pair connect enabled |

1.3.533 BUS_SW0

Bus Switch Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BUS_SW0: 0x40005B58

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | ag7 | ag6 | ag5 | ag4 | ag3 | ag2 | ag1 | ag0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------|---|
| 7 | ag7 | Connect Left and Right Analog Globals See Table 1-515. |
| 6 | ag6 | Connect Left and Right Analog Globals See Table 1-514. |
| 5 | ag5 | Connect Left and Right Analog Globals See Table 1-513. |
| 4 | ag4 | Connect Left and Right Analog Globals See Table 1-512. |
| 3 | ag3 | Connect Left and Right Analog Globals See Table 1-511. |
| 2 | ag2 | Connect Left and Right Analog Globals See Table 1-510. |
| 1 | ag1 | Connect Left and Right Analog Globals See Table 1-509. |
| 0 | ag0 | Connect Left and Right Analog Globals See Table 1-508. |

Table 1-508. Bit field encoding: AG0_ENUM

| Value | Name | Description |
|-------|-------------|------------------------------|
| 1'b0 | AG0_NC | Disconnect AGL[0] and AGR[0] |
| 1'b1 | AG0_CONNECT | Connect AGL[0] and AGR[0] |

Table 1-509. Bit field encoding: AG1_ENUM

| Value | Name | Description |
|-------|--------|------------------------------|
| 1'b0 | AG1_NC | Disconnect AGL[1] and AGR[1] |

1.3.533 BUS_SW0 (continued)

Table 1-509. Bit field encoding: AG1_ENUM

| | | |
|------|-------------|---------------------------|
| 1'b1 | AG1_CONNECT | Connect AGL[1] and AGR[1] |
|------|-------------|---------------------------|

Table 1-510. Bit field encoding: AG2_ENUM

| Value | Name | Description |
|-------|-------------|------------------------------|
| 1'b0 | AG2_NC | Disconnect AGL[2] and AGR[2] |
| 1'b1 | AG2_CONNECT | Connect AGL[2] and AGR[2] |

Table 1-511. Bit field encoding: AG3_ENUM

| Value | Name | Description |
|-------|-------------|------------------------------|
| 1'b0 | AG3_NC | Disconnect AGL[3] and AGR[3] |
| 1'b1 | AG3_CONNECT | Connect AGL[3] and AGR[3] |

Table 1-512. Bit field encoding: AG4_ENUM

| Value | Name | Description |
|-------|-------------|------------------------------|
| 1'b0 | AG4_NC | Disconnect AGL[4] and AGR[4] |
| 1'b1 | AG4_CONNECT | Connect AGL[4] and AGR[4] |

Table 1-513. Bit field encoding: AG5_ENUM

| Value | Name | Description |
|-------|-------------|------------------------------|
| 1'b0 | AG5_NC | Disconnect AGL[5] and AGR[5] |
| 1'b1 | AG5_CONNECT | Connect AGL[5] and AGR[5] |

Table 1-514. Bit field encoding: AG6_ENUM

| Value | Name | Description |
|-------|-------------|------------------------------|
| 1'b0 | AG6_NC | Disconnect AGL[6] and AGR[6] |
| 1'b1 | AG6_CONNECT | Connect AGL[6] and AGR[6] |

Table 1-515. Bit field encoding: AG7_ENUM

| Value | Name | Description |
|-------|-------------|------------------------------|
| 1'b0 | AG7_NC | Disconnect AGL[7] and AGR[7] |
| 1'b1 | AG7_CONNECT | Connect AGL[7] and AGR[7] |

0x40005b5a

1.3.534 BUS_SW2

Bus Switch Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BUS_SW2: 0x40005B5A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-------|-------|-------|-------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | abus3 | abus2 | abus1 | abus0 |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------|---|
| 3 | abus3 | Connect Left and Right Analog (local) Buses See Table 1-519. |
| 2 | abus2 | Connect Left and Right Analog (local) Buses See Table 1-518. |
| 1 | abus1 | Connect Left and Right Analog (local) Buses See Table 1-517. |
| 0 | abus0 | Connect Left and Right Analog (local) Buses See Table 1-516. |

Table 1-516. Bit field encoding: ABUS0_ENUM

| Value | Name | Description |
|-------|---------------|----------------------------------|
| 1'b0 | ABUS0_NC | Disconnect ABUSL[0] and ABUSR[0] |
| 1'b1 | ABUS0_CONNECT | Connect ABUSL[0] and ABUSR[0] |

Table 1-517. Bit field encoding: ABUS1_ENUM

| Value | Name | Description |
|-------|---------------|----------------------------------|
| 1'b0 | ABUS1_NC | Disconnect ABUSL[1] and ABUSR[1] |
| 1'b1 | ABUS1_CONNECT | Connect ABUSL[1] and ABUSR[1] |

Table 1-518. Bit field encoding: ABUS2_ENUM

| Value | Name | Description |
|-------|---------------|----------------------------------|
| 1'b0 | ABUS2_NC | Disconnect ABUSL[2] and ABUSR[2] |
| 1'b1 | ABUS2_CONNECT | Connect ABUSL[2] and ABUSR[2] |

Table 1-519. Bit field encoding: ABUS3_ENUM

| Value | Name | Description |
|-------|---------------|----------------------------------|
| 1'b0 | ABUS3_NC | Disconnect ABUSL[3] and ABUSR[3] |
| 1'b1 | ABUS3_CONNECT | Connect ABUSL[3] and ABUSR[3] |

1.3.535 BUS_SW3

Bus Switch Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BUS_SW3: 0x40005B5B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|--------------|---|------|-------|
| SW Access:Reset | NA:0000 | | | | R/W:00 | | NA:0 | R/W:0 |
| HW Access | NA | | | | R | | NA | R |
| Name | | | | | power2ag_sel | | | amx |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------------|--|
| 3:2 | power2ag_sel[1:0] | Connect power pins to Analog Global See Table 1-521. |
| 0 | amx | Connect Left and Righth Analog Mux Bus See Table 1-520. |

Table 1-520. Bit field encoding: AMX_ENUM

| Value | Name | Description |
|-------|-------------|--------------------------|
| 1'b0 | AMX_NC | Disconnect AMXL and AMXR |
| 1'b1 | AMX_CONNECT | Connect AMXL and AMXR |

Table 1-521. Bit field encoding: POWER2AG_SEL_ENUM

| Value | Name | Description |
|-------|------------------|--|
| 2'h0 | POWER2AG_SEL_NC | AGL[3] not connected to power pins |
| 2'h1 | POWER2AG_SEL_VDD | AGL[3] connected to vdda |
| | A | |
| 2'h2 | POWER2AG_SEL_VDD | AGL[3] connected to vddd |
| | D | |
| 2'h3 | POWER2AG_SEL_VBA | AGL[3] connected to vbat (RC filtered) |
| | T | |

1.3.536 DFT_CR0

DFT Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFT_CR0: 0x40005B5C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|--------|-------|--------|------|------------|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:0 | R/W:000 | | |
| HW Access | R | R | R | R | NA | R | | |
| Name | rsvd2 | en_tp2 | rsvd1 | en_tp1 | | tvmon1_sel | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|---|
| 7 | rsvd2 | Reserved |
| 6 | en_tp2 | enable level shifting from TP2 (test point 2) pad to analog global route AGL1 |
| 5 | rsvd1 | Reserved |
| 4 | en_tp1 | enable level shifting from TP1 (test point 1) pad to analog global route AGL0 |
| 2:0 | tvmon1_sel[2:0] | Connect power net to tvmon1 test point (Also need to select tvmon1 for DFT mux input) |

[See Table 1-522.](#)

Table 1-522. Bit field encoding: TVMON1_SEL_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 3'h0 | TVMON1_SEL_NC | tvmon1/1a test points not connected (Default) |
| 3'h1 | TVMON1_SEL_VSLEEP | tvmon1/1a test points connected to vsleep |
| 3'h2 | TVMON1_SEL_VPWRA | tvmon1/1a test points connected to vpwra |
| | A | |
| 3'h3 | TVMON1_SEL_VPWRI2 | tvmon1/1a test points connected to vpwri2c |
| | C | |
| 3'h4 | TVMON1_SEL_VPB | tvmon1/1a test points connected to vpb/vccd (vpb is shorted to vccd) |
| 3'h5 | TVMON1_SEL_VPWRA | tvmon1/1a test points connected to vpwra |
| 3'h6 | TVMON1_SEL_VNWEL | tvmon1/1a test points connected to vnwell |
| | L | |
| 3'h7 | TVMON1_SEL_NC2 | tvmon1/1a test points not connected |

1.3.537 DFT_CR1

DFT Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFT_CR1: 0x40005B5D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-----------------|----------|---|---|---|---|---|------------|---|--|
| SW Access:Reset | NA:00000 | | | | | | R/W:000 | | |
| HW Access | NA | | | | | | R | | |
| Name | | | | | | | tvmon2_sel | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|---|
| 2:0 | tvmon2_sel[2:0] | Connect power net to tvmon2 test point (Also need to select tvmon1 for DFT mux input) See Table 1-523. |

Table 1-523. Bit field encoding: TVMON2_SEL_ENUM

| Value | Name | Description |
|-------|------------------|--|
| 3'h0 | TVMON2_SEL_NC | tvmon2/2a test points not connected (Default) |
| 3'h1 | TVMON2_SEL_VNB | tvmon2/2a test points connected to vnb |
| 3'h2 | TVMON2_SEL_VREF | tvmon2/2a test points connected to bref_v800mV |
| 3'h3 | TVMON2_SEL_VSSD | tvmon2/2a test points connected to vssd |
| 3'h4 | TVMON2_SEL_NPROT | tvmon2/2a test points connected to nprot |
| 3'h5 | TVMON2_SEL_BIASN | tvmon2/2a test points connected to biasn |
| 3'h6 | TVMON2_SEL_VSSA | tvmon2/2a test points connected to vssa |
| 3'h7 | TVMON2_SEL_NC2 | tvmon2/2a test points not connected |

1.3.538 DFT_CR2

DFT Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFT_CR2: 0x40005B5E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---|---|------|---------|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | NA:0 | R/W:000 | | |
| HW Access | NA | R | | | NA | R | | |
| Name | | dft_mx1 | | | | dft_mx0 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|---|
| 6:4 | dft_mx1[2:0] | Connect test signals to AGL<7> (Analog Global Left 7) See Table 1-525. |
| 2:0 | dft_mx0[2:0] | Connect test signals to AGL<4> (Analog Global Left 4) See Table 1-524. |

Table 1-524. Bit field encoding: DFT_MX0_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 3'h0 | DFT_MX0_0 | HiZ - Not connected (NC) |
| 3'h1 | DFT_MX0_DAC0_TMUX | Connect dac0_tmux to AGL<4>_AGL4 |
| 3'h2 | DFT_MX0_DSM0_SUM | Connect dsm0_sumn_tst to AGL<4>N_TST_AGL4 |
| 3'h3 | DFT_MX0_DSM0_REF | Connect dsm0_refout to AGL<4>OUT_AGL4 |
| 3'h4 | DFT_MX0_DSM0_TST_ | Connect dsm0_tst_digout to AGL<4>DIGOUT_AGL4 |
| 3'h5 | DFT_MX0_TS_DFT_AG | Connect ts_dft (SPC Temp Sensor) to AGL<4>L4 |
| 3'h6 | DFT_MX0_FM_DFT_AG | Connect fm_dft (Flash Memory) to AGL<4>L4 |
| 3'h7 | DFT_MX0_RSVD | Reserved - HiZ - Not connected (NC) |

Table 1-525. Bit field encoding: DFT_MX1_ENUM

| Value | Name | Description |
|-------|-------------------|--|
| 3'h0 | DFT_MX1_0 | HiZ - Not connected (NC) |
| 3'h1 | DFT_MX1_DAC2_TMUX | Connect dac2_tmux to AGL<7>_AGL7 |
| 3'h2 | DFT_MX1_CMP_DFT_A | Connect cmp_dft to AGL<7> (see also cmp_mxdff[1:0])GL7 |
| 3'h3 | DFT_MX1_TVMON1_A | Connect pwrsys tvmon1 to AGL<7>GL7 |
| 3'h4 | DFT_MX1_TVMON2_A | Connect pwrsys tvmon2 to AGL<7>GL7 |

1.3.538 DFT_CR2 (continued)

Table 1-525. Bit field encoding: DFT_MX1_ENUM

| | | |
|------|--------------------|---|
| 3'h5 | DFT_MX1_DSM0_SUM | Connect dsm0_sump_tst to AGL<7> P_TST_AGL7 |
| 3'h6 | DFT_MX1_BREF_ITEST | Connect bref_itest to AGL<7> _AGL7 |
| 3'h7 | DFT_MX1_RSVD | Reserved - HiZ - Not connected (NC) |

1.3.539 DFT_CR3

DFT Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFT_CR3: 0x40005B5F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---|---|------|---------|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | NA:0 | R/W:000 | | |
| HW Access | NA | R | | | NA | R | | |
| Name | | dft_mx3 | | | | dft_mx2 | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------|--|
| 6:4 | dft_mx3[2:0] | Connect test signals to AGR<7> (Analog Global Right 7) See Table 1-527. |
| 2:0 | dft_mx2[2:0] | Connect test signals to AGR<4> (Analog Global Right 4) See Table 1-526. |

Table 1-526. Bit field encoding: DFT_MX2_ENUM

| Value | Name | Description |
|-------|--------------------------------|-------------------------------------|
| 3'h0 | DFT_MX2_0 | HiZ - Not connected (NC) |
| 3'h1 | DFT_MX2_DAC3_TMUX_AGR4 | Connect dac1_tmux to AGR<4> |
| 3'h2 | DFT_MX2_BREF_ISRC_7_AGR4 | Connect bref_isrc7 to AGR<4> |
| 3'h3 | DFT_MX2_3 | HiZ - Not connected (NC) |
| 3'h4 | DFT_MX2_S8XOSC_TP_UMP_DFT_AGR4 | Connect s8xosc_tpump_dft to AGR<4> |
| 3'h5 | DFT_MX2_TVMON1A_A_GR4 | Connect pwrsys tvmon1a to AGR<4> |
| 3'h6 | DFT_MX2_TVMON2A_A_GR4 | Connect pwrsys tvmon2a to AGR<4> |
| 3'h7 | DFT_MX2_RSVD | Reserved - HiZ - Not connected (NC) |

Table 1-527. Bit field encoding: DFT_MX3_ENUM

| Value | Name | Description |
|-------|----------------------------------|--------------------------------------|
| 3'h0 | DFT_MX3_0 | NC |
| 3'h1 | DFT_MX3_DAC1_TMUX_AGR7 | Connect dac1_tmux to AGR<7> |
| 3'h2 | DFT_MX3_S8XOSC_TE_STOUT_DFT_AGR7 | Connect s8xosc_testout_dft to AGR<7> |
| 3'h3 | DFT_MX3_BGREFS_T_MUX_AGR7 | Connect bgrefs_tmux to AGR<7> |
| 3'h4 | DFT_MX3_BG_TMUX_A_GR7 | Connect bg_tmux to AGR<7> |

1.3.539 DFT_CR3 (continued)

Table 1-527. Bit field encoding: DFT_MX3_ENUM

| | | |
|------|--------------------|---|
| 3'h5 | DFT_MX3_X32_TST_A | Connect x32_tst to AGR<7> GR7 |
| 3'h6 | DFT_MX3_PLL_VCTRLI | Connect pll_VctrlIO to AGR<7> O_AGR7 |
| 3'h7 | DFT_MX3_RSVD | Reserved - HiZ - Not connected (NC) |

1.3.540 DFT_CR4

DFT Control Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFT_CR4: 0x40005B60

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|------------|---|---|------|------------|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | NA:0 | R/W:000 | | |
| HW Access | NA | R | | | NA | R | | |
| Name | | nw_mux_sel | | | | ne_mux_sel | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 6:4 | nw_mux_sel[2:0] | Northwest IO Ring Corner Power Probe Mux Selection See Table 1-529. |
| 2:0 | ne_mux_sel[2:0] | Northeast IO Ring Corner Power Probe Mux Selection See Table 1-528. |

Table 1-528. Bit field encoding: NE_MUX_SEL_ENUM

| Value | Name | Description |
|-------|---------------|--------------------------------------|
| 3'h0 | NE_MUX_SEL_NC | NC (HiZ) |
| 3'h1 | NE_MUX_SEL_1 | vpwrao |
| 3'h2 | NE_MUX_SEL_2 | vnwell |
| 3'h3 | NE_MUX_SEL_3 | vpwrka |
| 3'h4 | NE_MUX_SEL_4 | vpwrsleep |
| 3'h5 | NE_MUX_SEL_5 | vccd |
| 3'h6 | NE_MUX_SEL_6 | vcd_lcd (South side of power switch) |
| 3'h7 | NE_MUX_SEL_7 | vccd_io (South side of power switch) |

Table 1-529. Bit field encoding: NW_MUX_SEL_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 3'h0 | NW_MUX_SEL_NC | NC (HiZ) |
| 3'h1 | NW_MUX_SEL_1 | vpwrao |
| 3'h2 | NW_MUX_SEL_2 | vnwell |
| 3'h3 | NW_MUX_SEL_3 | vpwrka |
| 3'h4 | NW_MUX_SEL_4 | vccd |
| 3'h5 | NW_MUX_SEL_5 | vccd_leopard_main_pd (South side of power switch) |
| 3'h6 | NW_MUX_SEL_6 | vccd |
| 3'h7 | NW_MUX_SEL_7 | vccd_leopard_clkpm_pd (South side of power switch) |

1.3.541 DFT_CR5

DFT Control Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFT_CR5: 0x40005B61

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|------------|---|---|------|------------|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | NA:0 | R/W:000 | | |
| HW Access | NA | R | | | NA | R | | |
| Name | | sw_mux_sel | | | | se_mux_sel | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|--|
| 6:4 | sw_mux_sel[2:0] | Southwest IO Ring Corner Power Probe Mux Selection See Table 1-531. |
| 2:0 | se_mux_sel[2:0] | Southeast IO Ring Corner Power Probe Mux Selection See Table 1-530. |

Table 1-530. Bit field encoding: SE_MUX_SEL_ENUM

| Value | Name | Description |
|-------|---------------|--|
| 3'h0 | SE_MUX_SEL_NC | NC (HiZ) |
| 3'h1 | SE_MUX_SEL_1 | vpwrao |
| 3'h2 | SE_MUX_SEL_2 | vnwell |
| 3'h3 | SE_MUX_SEL_3 | vpwrka |
| 3'h4 | SE_MUX_SEL_4 | vpwr_udb (South side of power switch) |
| 3'h5 | SE_MUX_SEL_5 | vpwr_imo (South side of power switch) |
| 3'h6 | SE_MUX_SEL_6 | vpwri2c |
| 3'h7 | SE_MUX_SEL_7 | vbleed_sysmem_0 (South side of power switch) |

Table 1-531. Bit field encoding: SW_MUX_SEL_ENUM

| Value | Name | Description |
|-------|---------------|---|
| 3'h0 | SW_MUX_SEL_NC | NC (HiZ) |
| 3'h1 | SW_MUX_SEL_1 | vpwrao |
| 3'h2 | SW_MUX_SEL_2 | vnwell |
| 3'h3 | SW_MUX_SEL_3 | vpwrka |
| 3'h4 | SW_MUX_SEL_4 | vpwr_fm (South side of power switch) |
| 3'h5 | SW_MUX_SEL_5 | vpwr_nvmpump_pos (South side of power switch) |
| 3'h6 | SW_MUX_SEL_6 | vpwr_ee (South side of power switch) |
| 3'h7 | SW_MUX_SEL_7 | vpwr_iref (South side of power switch) |

1.3.542 DAC[0..3]_D

DAC Data Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_D: 0x40005B80

DAC1_D: 0x40005B81

DAC2_D: 0x40005B82

DAC3_D: 0x40005B83

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|-----------------|
| 7:0 | data[7:0] | 8 DAC Data bits |

1.3.543 DSM[0..0]_OUT0

DSM Output Register 0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DSM0_OUT0: 0x40005B88

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | dout | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|-------------|
| 7:0 | dout[7:0] | DSM output |

1.3.544 DSM[0..0]_OUT1

DSM Output Register 1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DSM0_OUT1: 0x40005B89

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|----------|---------|------------|---|---|---|
| SW Access:Reset | NA:00 | | R:0 | R:0 | R:0000 | | | |
| HW Access | NA | | W | W | W | | | |
| Name | | | ovdcause | ovdflag | dout2scomp | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------------|---|
| 5 | ovdcause | Overload Cause See Table 1-533. |
| 4 | ovdflag | Overload detected |
| 3:0 | dout2scomp[3:0] | DSM Output Register 1 See Table 1-532. |

Table 1-532. Bit field encoding: DSM_DOUT2SCOMP_ENUM

| Value | Name | Description |
|-------|------------------|---|
| 4'h0 | DSM_DOUT2SCOMP_0 | NA (qlev=00); 0 (qlev=01); 0 (qlev=10) |
| 4'h1 | DSM_DOUT2SCOMP_1 | +1 (qlev=00); +1 (qlev=01); +1 (qlev=10) |
| 4'h2 | DSM_DOUT2SCOMP_2 | NA (qlev=00); NA (qlev=01); +2 (qlev=10) |
| 4'h3 | DSM_DOUT2SCOMP_3 | NA (qlev=00); NA (qlev=01); +3 (qlev=10) |
| 4'h4 | DSM_DOUT2SCOMP_4 | NA (qlev=00); NA (qlev=01); +4 (qlev=10) |
| 4'h5 | DSM_DOUT2SCOMP_5 | NA (qlev=00); NA (qlev=01); NA (qlev=10) |
| 4'h6 | DSM_DOUT2SCOMP_6 | NA (qlev=00); NA (qlev=01); NA (qlev=10) |
| 4'h7 | DSM_DOUT2SCOMP_7 | NA (qlev=00); NA (qlev=01); NA (qlev=10) |
| 4'h8 | DSM_DOUT2SCOMP_8 | NA (qlev=00); NA (qlev=01); NA (qlev=10) |
| 4'h9 | DSM_DOUT2SCOMP_9 | NA (qlev=00); NA (qlev=01); NA (qlev=10) |
| 4'ha | DSM_DOUT2SCOMP_1 | NA (qlev=00); NA (qlev=01); NA (qlev=10) |
| 4'hb | DSM_DOUT2SCOMP_1 | 0 NA (qlev=00); NA (qlev=01); NA (qlev=10) |
| 4'hc | DSM_DOUT2SCOMP_1 | 1 NA (qlev=00); NA (qlev=01); -4 (qlev=10) |
| 4'hd | DSM_DOUT2SCOMP_1 | 2 NA (qlev=00); NA (qlev=01); -3 (qlev=10) |
| 4'he | DSM_DOUT2SCOMP_1 | 3 NA (qlev=00); NA (qlev=01); -2 (qlev=10) |
| 4'hf | DSM_DOUT2SCOMP_1 | 4 -1 (qlev=00); -1 (qlev=01); -1 (qlev=10) |
| | | 5 |

1.3.544 DSM[0..0]_OUT1 (continued)

Table 1-533. Bit field encoding: OVDCAUSE_ENUM

| Value | Name | Description |
|-------|------------|-------------|
| 1'b0 | OVDCAUSE_0 | 0s overload |
| 1'b1 | OVDCAUSE_1 | 1s overload |

1.3.545 LUT_SR

LUT Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

LUT_SR: 0x40005B90

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|----------|----------|----------|
| SW Access:Reset | NA:0000 | | | | RC:0 | RC:0 | RC:0 | RC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | lut3_out | lut2_out | lut1_out | lut0_out |

Clear-on-read sticky status register

Register Segment: 3

| Bits | Name | Description |
|------|----------|-------------|
| 3 | lut3_out | LUT output |
| 2 | lut2_out | LUT output |
| 1 | lut1_out | LUT output |
| 0 | lut0_out | LUT output |

1.3.546 LUT_WRK1

Reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT_WRK1: 0x40005B91

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|-------------|
| 7:0 | RSVD[7:0] | Reserved |

1.3.547 LUT_MSK

LUT Interrupt ReQuest (IRQ) Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT_MSK: 0x40005B92

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|----------|----------|----------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | lut3_msk | lut2_msk | lut1_msk | lut0_msk |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|--|
| 3 | lut3_msk | Enable LUT IRQ See Table 1-534. |
| 2 | lut2_msk | Enable LUT IRQ See Table 1-534. |
| 1 | lut1_msk | Enable LUT IRQ See Table 1-534. |
| 0 | lut0_msk | Enable LUT IRQ See Table 1-534. |

Table 1-534. Bit field encoding: LUT_MSK_ENUM

| Value | Name | Description |
|-------|-----------------|-----------------|
| 1'b1 | LUT_MSK_ENABLE | enable LUT IRQ |
| 1'b0 | LUT_MSK_DISABLE | disable LUT IRQ |

1.3.548 LUT_CLK

LUT CLK Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT_CLK: 0x40005B93

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-------------|-------------|-------------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | lut3_en_clk | lut2_en_clk | lut1_en_clk | lut0_en_clk |

LUT status clk gater control

Register Segment: 3

| Bits | Name | Description |
|------|-------------|--|
| 3 | lut3_en_clk | LUT status clock gater control See Table 1-535. |
| 2 | lut2_en_clk | LUT status clock gater control See Table 1-535. |
| 1 | lut1_en_clk | LUT status clock gater control See Table 1-535. |
| 0 | lut0_en_clk | LUT status clock gater control See Table 1-535. |

Table 1-535. Bit field encoding: LUT_EN_CLK_ENUM

| Value | Name | Description |
|-------|--------------------|---|
| 1'b0 | LUT_EN_CLK_DISABLE | LUT status clock disabled |
| 1'b1 | LUT_EN_CLK_ENABLE | LUT status clock enabled (must set this bit for LUT interrupts) |

1.3.549 LUT_CPTR

LUT Capture Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT_CPTR: 0x40005B94

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-------------------|-------------------|-------------------|-------------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | lut3_capture_mode | lut2_capture_mode | lut1_capture_mode | lut0_capture_mode |

LUT status capture mode

Register Segment: 3

| Bits | Name | Description |
|------|-------------------|---|
| 3 | lut3_capture_mode | LUT status capture mode See Table 1-536. |
| 2 | lut2_capture_mode | LUT status capture mode See Table 1-536. |
| 1 | lut1_capture_mode | LUT status capture mode See Table 1-536. |
| 0 | lut0_capture_mode | LUT status capture mode See Table 1-536. |

Table 1-536. Bit field encoding: LUT_CAPTURE_MODE_ENUM

| Value | Name | Description |
|-------|------------------------|-------------------------------|
| 1'b0 | LUT_CAPTURE_MODE_EDGE | LUT status edge capture mode |
| 1'b1 | LUT_CAPTURE_MODE_LEVEL | LUT status level capture mode |

1.3.550 CMP_WRK

Comparator output working register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CMP_WRK: 0x40005B96

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|----------|----------|----------|
| SW Access:Reset | NA:0000 | | | | R:0 | R:0 | R:0 | R:0 |
| HW Access | NA | | | | W | W | W | W |
| Name | | | | | cmp3_out | cmp2_out | cmp1_out | cmp0_out |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------|-------------------|
| 3 | cmp3_out | Comparator Output |
| 2 | cmp2_out | Comparator Output |
| 1 | cmp1_out | Comparator Output |
| 0 | cmp0_out | Comparator Output |

1.3.551 CMP_TST

Comparator Test Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP_TST: 0x40005B97

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|---|------|--------------------|
| SW Access:Reset | NA:0000 | | | | R/W:00 | | NA:0 | R/W:0 |
| HW Access | NA | | | | R | | NA | R |
| Name | | | | | cmp_mxdfs | | | bypass_cm p_mux |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|----------------|---|
| 3:2 | cmp_mxdfs[1:0] | Comparator Test Point selection (Need to further select with DFT muxes) See Table 1-538. |
| 0 | bypass_cmp_mux | Selects if the input of the comparator or the output gets routed through to the output of the block See Table 1-537. |

Table 1-537. Bit field encoding: CMP_BYPASS_CMP_MUX_ENUM

| Value | Name | Description |
|-------|--------------------------------|--|
| 1'b0 | CMP_BYPASS_CMP_M UX_DISABLE | Selects the output of the comparator |
| 1'b1 | CMP_BYPASS_CMP_M UX_ENABLE | Selects the positive input of the comparator |

Table 1-538. Bit field encoding: CMP_MXDFT_ENUM

| Value | Name | Description |
|-------|-------------|-------------|
| 2'h0 | CMP_MXDFT_0 | cmp0_out_tr |
| 2'h1 | CMP_MXDFT_1 | cmp1_out_tr |
| 2'h2 | CMP_MXDFT_2 | cmp2_out_tr |
| 2'h3 | CMP_MXDFT_3 | cmp3_out_tr |

1.3.552 SC_SR

Switched Capacitor Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

SC_SR: 0x40005B98

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------------|------------|------------|------------|
| SW Access:Reset | NA:0000 | | | | RC:0 | RC:0 | RC:0 | RC:0 |
| HW Access | NA | | | | W | W | W | W |
| Name | | | | | sc3_modout | sc2_modout | sc1_modout | sc0_modout |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|-------------------------------------|
| 3 | sc3_modout | Switched Cap block modulator output |
| 2 | sc2_modout | Switched Cap block modulator output |
| 1 | sc1_modout | Switched Cap block modulator output |
| 0 | sc0_modout | Switched Cap block modulator output |

1.3.553 SC_WRK1

Reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_WRK1: 0x40005B99

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-----------|-------------|
| 7:0 | RSVD[7:0] | Reserved |

1.3.554 SC_MSK

SC IRQ Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_MSK: 0x40005B9A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---------|---------|---------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | sc3_msk | sc2_msk | sc1_msk | sc0_msk |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|---------|---|
| 3 | sc3_msk | Enable SC IRQ See Table 1-539. |
| 2 | sc2_msk | Enable SC IRQ See Table 1-539. |
| 1 | sc1_msk | Enable SC IRQ See Table 1-539. |
| 0 | sc0_msk | Enable SC IRQ See Table 1-539. |

Table 1-539. Bit field encoding: SC_MSK_ENUM

| Value | Name | Description |
|-------|----------------|----------------|
| 1'b1 | SC_MSK_ENABLE | enable SC IRQ |
| 1'b0 | SC_MSK_DISABLE | disable SC IRQ |

1.3.555 SC_CMPINV

SC comparator inversion

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_CMPINV: 0x40005B9B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------------|------------|------------|------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | sc3_cmpinv | sc2_cmpinv | sc1_cmpinv | sc0_cmpinv |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|------------|--|
| 3 | sc3_cmpinv | Switched Cap modulator comparator output inversion control See Table 1-540. |
| 2 | sc2_cmpinv | Switched Cap modulator comparator output inversion control See Table 1-540. |
| 1 | sc1_cmpinv | Switched Cap modulator comparator output inversion control See Table 1-540. |
| 0 | sc0_cmpinv | Switched Cap modulator comparator output inversion control See Table 1-540. |

Table 1-540. Bit field encoding: SC_CMPINV_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 1'b0 | SC_CMPINV_DISABLE | Switched Cap modulator comparator output not inverted |
| 1'b1 | SC_CMPINV_ENABLE | Switched Cap modulator comparator output inverted |

1.3.556 SC_CPTR

SC Capture Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_CPTR: 0x40005B9C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | sc3_capture_mode | sc2_capture_mode | sc1_capture_mode | sc0_capture_mode |

SC status capture mode

Register Segment: 3

| Bits | Name | Description |
|------|------------------|--|
| 3 | sc3_capture_mode | SC status capture mode See Table 1-541. |
| 2 | sc2_capture_mode | SC status capture mode See Table 1-541. |
| 1 | sc1_capture_mode | SC status capture mode See Table 1-541. |
| 0 | sc0_capture_mode | SC status capture mode See Table 1-541. |

Table 1-541. Bit field encoding: SC_CAPTURE_MODE_ENUM

| Value | Name | Description |
|-------|-----------------------|------------------------------|
| 1'b0 | SC_CAPTURE_MODE_EDGE | SC status edge capture mode |
| 1'b1 | SC_CAPTURE_MODE_LEVEL | SC status level capture mode |

1.3.557 SAR[0..1]_WRK0

SAR working register 0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

SAR0_WRK0: 0x40005BA0

SAR1_WRK0: 0x40005BA2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_out_7_0 | | | | | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|-------------------|---------------|
| 7:0 | data_out_7_0[7:0] | data_out[7:0] |

1.3.558 SAR[0..1]_WRK1

SAR register 1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

SAR0_WRK1: 0x40005BA1

SAR1_WRK1: 0x40005BA3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|--------|---|---|---------------|---|---|---|
| SW Access:Reset | RC:0 | NA:000 | | | R:0000 | | | |
| HW Access | R/W | NA | | | R/W | | | |
| Name | overrun_det | | | | data_out_11_8 | | | |

(no description)

Register Segment: 3

| Bits | Name | Description |
|------|--------------------|---|
| 7 | overrun_det | data overrun detection flag (read-to-clear sticky bit) is set when overrun_det_en is set and new data overwrote old data / old data not read (completely) See Table 1-542. |
| 3:0 | data_out_11_8[3:0] | data_out[11:8] |

Table 1-542. Bit field encoding: SAR_OVERRUN_DET_ENUM

| Value | Name | Description |
|-------|-------------------|---|
| 1'b0 | SAR_OVERRUN_DET_0 | no data overrun has occurred |
| 1'b1 | SAR_OVERRUN_DET_1 | data overrun has occurred - all bytes of the last data_out have not been read when new data was written |

1.3.559 ANAIF_WRK_SARS_SOF

SAR Global Start-of-frame register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ANAIF_WRK_SARS_SOF: 0x40005BA8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|-----------|-----------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | sof_bit_1 | sof_bit_0 |

PRIOR to setting the SOF bit of a SAR, you must enable the SAR's clock by programming the SAR0_CLK (SAR0) or SAR1_CLK (SAR1) register appropriately; the minimum being to set the clk_en bit to 1'b1. The default upon reset when enabling will be SAR clock source == clk_a[0], with Freq(clk_a[0]) = Freq(cpu_clk); that is, divide by one (1). Optionally, you can divide the SAR's clock frequency by programming the corresponding divider value registers (e.g. {CLKDIST_ACFG0_CFG1:CLKDIST_ACFG0_CFG0} if clk_a[0] is selected).

Register Segment: 3

| Bits | Name | Description |
|------|-----------|--|
| 1 | sof_bit_1 | Start-of-Frame (sof) register source; enable conversion; (NOTE: autoclearing upon receipt of eof_sync when sof_mode==edge-sensitive) See Table 1-543. |
| 0 | sof_bit_0 | Start-of-Frame (sof) register source; enable conversion; (NOTE: autoclearing upon receipt of eof_sync when sof_mode==edge-sensitive) See Table 1-543. |

Table 1-543. Bit field encoding: SAR_SOF_BIT_ENUM

| Value | Name | Description |
|-------|---------------|--------------------|
| 1'b0 | SAR_SOF_BIT_0 | disable conversion |
| 1'b1 | SAR_SOF_BIT_1 | Enable conversion |

1.3.560 USB_EP0_DR[0..7]

Control End point EP0 Data Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

| | |
|-------------------------|-------------------------|
| USB_EP0_DR0: 0x40006000 | USB_EP0_DR1: 0x40006001 |
| USB_EP0_DR2: 0x40006002 | USB_EP0_DR3: 0x40006003 |
| USB_EP0_DR4: 0x40006004 | USB_EP0_DR5: 0x40006005 |
| USB_EP0_DR6: 0x40006006 | USB_EP0_DR7: 0x40006007 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_byte | | | | | | | |

The Endpoint 0 Data Register (EP0_DR) is used to read and write data to the USB control endpoint. The EP0_DR register has a hardware-locking feature that prevents the CPU write when SETUP is active. The registers are locked as soon as the SETUP token is decoded and remain locked throughout the SETUP transaction and until the EP0_CR register have been read. This is to prevent over-writing new SETUP data before firmware knows it has arrived. All other endpoint data buffers do not have this locking feature. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|----------------|--|
| 7:0 | data_byte[7:0] | This register is shared for both transmit and receive. The count in the EP0_CNT register determines the number of bytes received or to be transferred. |

1.3.561 USB_CR0

USB control 0 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_CR0: 0x40006008

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|----------------|---|---|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0000000 | | | | | | |
| HW Access | R | R | | | | | | |
| Name | usb_enable | device_address | | | | | | |

The USB Control Register 0 (CR0) is used to set the PSoC3's USB address and enable the USB system resource. All bits in this register are reset to zero when a USB bus reset interrupt occurs. The IMO frequency should be set to 24MHz before USB is enabled. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|---------------------|--|
| 7 | usb_enable | This bit enables the PSoC device to respond to USB traffic. 0 - USB disabled. 1 - USB enabled. |
| 6:0 | device_address[6:0] | These bits specify the USB device address to which the SIE will respond. This address must be set by firmware and is specified by the USB Host with a SET ADDRESS command during USB enumeration. This value must be programmed by firmware when assigned during enumeration. It is not set automatically by the hardware. |

1.3.562 USB_CR1

USB control 1 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_CR1: 0x40006009

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------------|--------------|-------------|------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/WZC:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | W | R | R |
| Name | | | | | trim_offset_msb | bus_activity | enable_lock | reg_enable |

The USB Control Register 1 (CR1) is used to configure the internal regulator and the oscillator tuning capability. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------------|---|
| 3 | trim_offset_msb | This bit is enable/disable for using trim bit[7]. 0-enabled. 1-disabled. |
| 2 | bus_activity | The Bus Activity bit is a stickybit that detects any non-idle USB event that has occurred on the USB bus. Once set to High by the SIE to indicate the bus activity this bit retains its logical High value until firmware clears it. Writing a '0' to this bit clears it; writing a '1' preserves its value. 0 No activity. 1 Non-idle activity (D+ = Low) was detected since the last time the bit was cleared. Sticky (individual bits) |
| 1 | enable_lock | This bit is set to turn on the automatic frequency locking of the internal oscillator to USB traffic. Unless an external clock is being provided this bit should remain set for proper USB operation. 0 Locking disabled. 1 Locking enabled. |
| 0 | reg_enable | This bit controls the operation of the internal USB regulator. For applications with PSoC supply voltages in the 5V range this bit is set high to enable the internal regulator. For device supply voltage in the 3.3V range this bit is cleared to connect the transceiver directly to the supply. 0-Pass-through mode. Use for Vdd = 3.3V range. 1- Regulating mode. Use for Vdd = 5V range. |

1.3.563 USB_SIE_EP_INT_EN

USB SIE Data Endpoints Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP_INT_EN: 0x4000600A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | ep8_intr_en | ep7_intr_en | ep6_intr_en | ep5_intr_en | ep4_intr_en | ep3_intr_en | ep2_intr_en | ep1_intr_en |

The USB SIE Data Endpoints Interrupt Enable Register (SIE_EP_INT_EN) is used to enable/ mask the Data Endpoint Interrupts This register is clocked with the AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---|
| 7 | ep8_intr_en | EP8 Interrupt Enable. 0: Do not raise EP8 Interrupt. 1: Raise EP8 Interrupt |
| 6 | ep7_intr_en | EP7 Interrupt Enable. 0: Do not raise EP7 Interrupt. 1: Raise EP7 Interrupt |
| 5 | ep6_intr_en | EP6 Interrupt Enable. 0: Do not raise EP6 Interrupt. 1: Raise EP6 Interrupt |
| 4 | ep5_intr_en | EP5 Interrupt Enable. 0: Do not raise EP5 Interrupt. 1: Raise EP5 Interrupt |
| 3 | ep4_intr_en | EP4 Interrupt Enable. 0: Do not raise EP4 Interrupt. 1: Raise EP4 Interrupt |
| 2 | ep3_intr_en | EP3 Interrupt Enable. 0: Do not raise EP3 Interrupt. 1: Raise EP3 Interrupt |
| 1 | ep2_intr_en | EP2 Interrupt Enable. 0: Do not raise EP2 Interrupt. 1: Raise EP2 Interrupt |
| 0 | ep1_intr_en | EP1 Interrupt Enable. 0: Do not raise EP1 Interrupt. 1: Raise EP1 Interrupt |

1.3.564 USB_SIE_EP_INT_SR

SIE Data Endpoint Interrupt Status

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP_INT_SR: 0x4000600B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|----------|----------|----------|----------|----------|----------|----------|
| SW Access:Reset | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | ep8_intr | ep7_intr | ep6_intr | ep5_intr | ep4_intr | ep3_intr | ep2_intr | ep1_intr |

SIE Data Endpoint Status Register. This is an Interrupt Status Register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------|---|
| 7 | ep8_intr | EP8 Interrupt Status. 0: EP8 Interrupt not raised. 1: EP8 Interrupt Present |
| 6 | ep7_intr | EP7 Interrupt Status. 0: EP7 Interrupt not raised. 1: EP7 Interrupt Present |
| 5 | ep6_intr | EP6 Interrupt Status. 0: EP6 Interrupt not raised. 1: EP6 Interrupt Present |
| 4 | ep5_intr | EP5 Interrupt Status. 0: EP5 Interrupt not raised. 1: EP5 Interrupt Present |
| 3 | ep4_intr | EP4 Interrupt Status. 0: EP4 Interrupt not raised. 1: EP4 Interrupt Present |
| 2 | ep3_intr | EP3 Interrupt Status. 0: EP3 Interrupt not raised. 1: EP3 Interrupt Present |
| 1 | ep2_intr | EP2 Interrupt Status. 0: EP2 Interrupt not raised. 1: EP2 Interrupt Present |
| 0 | ep1_intr | EP1 Interrupt Status. 0: EP1 Interrupt not raised. 1: EP1 Interrupt Present |

1.3.565 USB_SIE_EP1_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP1_CNT0: 0x4000600C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|------------|--------|---|---|----------------|---|---|
| SW Access:Reset | R/W:0 | R/WZC:0 | NA:000 | | | R/W:000 | | |
| HW Access | R/W | W | NA | | | R/W | | |
| Name | data_toggle | data_valid | | | | data_count_msb | | |

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|---------------------|---|
| 7 | data_toggle | This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1 |
| 6 | data_valid | This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits) |
| 2:0 | data_count_msb[2:0] | These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information. |

1.3.566 USB_SIE_EP1_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP1_CNT1: 0x4000600D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_count | | | | | | | |

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater than the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | data_count[7:0] | These bits are the 8 LSb of a 11-bit counter. The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction. |



0x4000600d

1.3.567 USB_SIE_EP1_CR0

Propname Non-control endpoint's control Register

0x4000600e Domain reset for non-retention flops [reset_all_nonretention] Register : Address The Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.568 USB_USBIO_CR0

USBIO Control 0 Register

Reset: Reset Signals Listed Below

Register : Address

USB_USBIO_CR0: 0x40006010

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|---------|---|---|---|-----|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | NA:0000 | | | | R:U |
| HW Access | R | R | R | NA | | | | W |
| Name | ten | tse0 | td | | | | | rd |

The USB IO Control Register 0 (USBIO_CR0) is used for manually transmitting on the USB D+ and D- pins or reading the differential receiver. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|------|---|
| 7 | ten | USB Transmit Enable. This is used to manually transmit on the D+ and D- pins. Normally this bit should be cleared to allow the internal SIE to drive the pins. The most common reason for manually transmitting is to force a resume state on the bus. 0- Manual Transmission Off (TSE0 and TD have no effect). 1- Manual Transmission Enabled (TSE0 and TD determine the state of the D+ and Dpins). |
| 6 | tse0 | Transmit Single-Ended Zero. SE0: both D+ and D- low. No effect if TEN=0. 0- Do not force SE0. 1- Force SE0 on D+ and D-. |
| 5 | td | Transmit Data. Transmit a USB J or K state on the USB bus. No effect if TEN=0 or TSE0=1. 0- Force USB K state (D+ is low D- is high). 1- Force USB J state (D+ is high D- is low) |
| 0 | rd | Received Data. This read only bit gives the state of the USB differential receiver. 0- D+ < D- or D+ = D- = 0. |

Reset Table

| resetsignal | field(s) |
|---|------------------------|
| N/A | rd |
| System reset for retention [reset_all_retention] | td, tse0, ten flops |

1.3.569 USB_USBIO_CR2

USBIO control 2 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_USBIO_CR2: 0x40006011

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|----------|-------|-------|-------|-------|--------|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | |
| HW Access | R | R | R | R | R | R | R | |
| Name | test_res | test_pkt | x_dec | x_inc | minc | mdec | trim | |

The USB IO Control Register 2 (USBIO_CR2) is an internal register used for trimming the USBIO cell and for access to internal test modes. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------|---|
| 7 | test_res | This bit is for testing the nonpass through suspend mode pull up. 0- No effect. 1- Apply resistor to the D+ pin. |
| 6 | test_pkt | This bit enables the device to transmit a packet in response to an internally generated IN packet. 0- No effect. 1- Generate one packet when set. |
| 5 | x_dec | This bit supplies the option to decrease the USB crossover voltage. 0- No effect. 1- Decrement crossover voltage. |
| 4 | x_inc | This bit supplies the option to increase the USB crossover voltage. 0- No effect. 1- Increment crossover voltage. |
| 3 | minc | When set this bit increases the USB edge matching ratio. |
| 2 | mdec | When set this bit decreases the USB edge matching ratio. |
| 1:0 | trim[1:0] | These two bits of trim are for the suspend mode resistor. 00- No effect. 01- Lower idle voltage. 10- Raise idle voltage. 11- Do not use. |

1.3.570 USB_USBIO_CR1

USBIO control 1 Register

Reset: Reset Signals Listed Below

Register : Address

USB_USBIO_CR1: 0x40006012

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|-------|---|---------|-----|-----|
| SW Access:Reset | NA:00 | | R/W:1 | NA:00 | | R/W:0 | R:U | R:U |
| HW Access | NA | | R | NA | | R | W | W |
| Name | | | iomode | | | usbpuen | dpo | dmo |

The USB IO Control Register 1 (USBIO_CR1) is used to manually read or write the D+ and D- pins and to configure internal pull-up resistors on those pins. This register is clocked with AHB (BUS) Clock

| Bits | Name | Description |
|------|---------|--|
| 5 | iomode | This bit allows the D+ and D- pins to be configured for either USB mode or bit banded modes. If this bit is set the DMI and DPI bits are used to drive the D- and D+ pins. 0- USB Mode. Drive Mode has no effect. 1- Drive Mode DMI and DPI determine state of the D+ and D- pins. |
| 2 | usbpuen | This bit controls the connection of the internal 1.5 k pull up resistor on the D+ pin. 0- No effect. 1- Apply internal USB pull-up resistor to D+ pad. |
| 1 | dpo | This read only bit gives the state of the D+ pin. |
| 0 | dmo | This read only bit gives the state of the D- pin. |

Reset Table

| resetsignal | field(s) |
|--|-----------------|
| N/A | dmo, dpo |
| System reset for retention flops [reset_all_retention] | usbpuen, iomode |

1.3.571 USB_DYN_RECONFIG

USB Dynamic reconfiguration register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_DYN_RECONFIG: 0x40006014

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|--------------------------|-------------------|---|---|-------------------|
| SW Access:Reset | NA:000 | | | R:0 | R/W:000 | | | R/W:0 |
| HW Access | NA | | | W | R | | | R |
| Name | | | | dyn_reconfi g_rdy_sts | dyn_reconfig_epno | | | dyn_config_ en |

This register is used for dynamically configuring the data EPs. This register is clocked with AHB Clock

| Bits | Name | Description |
|------|------------------------|--|
| 4 | dyn_reconfig_rdy_sts | This bit indicates the ready status for the dynamic reconfiguration, when set to 1 , indicates the block is ready for reconfiguration . |
| 3:1 | dyn_reconfig_epno[2:0] | These bits indicates the EP number for which reconfiguration is required when dyn_config_en bit is set to 1. |
| 0 | dyn_config_en | This bit is used to enable the dynamic re-configuration for the selected EP. If set to 1 , indicates the reconfiguration required for selected EP. |

1.3.572 USB_SOF0

Start Of Frame Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SOF0: 0x40006018

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | frame_number | | | | | | | |

The USB Start of Frame Registers (SOF0 and SOF1) provide access to the 11-bit SOF frame number. Start of frame packets are sent from the host every one ms. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-------------------|--|
| 7:0 | frame_number[7:0] | It has the lower 8 bits [7:0] of the SOF frame number. |

1.3.573 USB_SOF1

Start Of Frame Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SOF1: 0x40006019

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|--------------|---|---|
| SW Access:Reset | NA:00000 | | | | | R:000 | | |
| HW Access | NA | | | | | R/W | | |
| Name | | | | | | frame_number | | |

The USB Start of Frame Registers (SOF0 and SOF1) provide access to the 11-bit SOF frame number. Start of frame packets are sent from the host every one ms. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-------------------|---|
| 2:0 | frame_number[2:0] | It has the upper 3 bits [10:8] of the SOF frame number. |

1.3.574 USB_SIE_EP2_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP2_CNT0: 0x4000601C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|------------|--------|---|---|----------------|---|---|
| SW Access:Reset | R/W:0 | R/WZC:0 | NA:000 | | | R/W:000 | | |
| HW Access | R/W | W | NA | | | R/W | | |
| Name | data_toggle | data_valid | | | | data_count_msb | | |

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|---------------------|---|
| 7 | data_toggle | This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1 |
| 6 | data_valid | This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits) |
| 2:0 | data_count_msb[2:0] | These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information. |

1.3.575 USB_SIE_EP2_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP2_CNT1: 0x4000601D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_count | | | | | | | |

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater than the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | data_count[7:0] | These bits are the 8 LSb of a 11-bit counter. The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction. |

1.3.576 USB_SIE_EP2_CR0

| | |
|------------------|---|
| Proprname | Non-control endpoint's control Register |
|------------------|---|

0x4000601eDomain reset for non-retention flops [reset_all_nonretention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.577 USB_OSCLK_DR0

Oscillator lock data register 0

Reset: N/A

Register : Address

USB_OSCLK_DR0: 0x40006020

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | W | | | | | | | |
| Name | adder | | | | | | | |

The Oscillator Lock Data Register 0 (OSCLK_DR0) is an internal register that may be used in the testing of the oscillator locking circuit. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|------------|---|
| 7:0 | adder[7:0] | These bits return the lower 8 bits of the oscillator locking circuits adder output. |

1.3.578 USB_OSCLK_DR1

Oscillator lock data register 1

Reset: N/A

Register : Address

USB_OSCLK_DR1: 0x40006021

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R:UUUUUUU | | | | | | |
| HW Access | NA | W | | | | | | |
| Name | | adder | | | | | | |

The Oscillator Lock Data Register 1 (OSCLK_DR1) is an internal register that may be used in the testing of the oscillator locking circuit. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|------------|---|
| 6:0 | adder[6:0] | These bits return the upper 7 bits of the oscillator locking circuits adder output. |

1.3.579 USB_EP0_CR

Endpoint0 control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_EP0_CR: 0x40006028

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---------|----------|-----------|----------|---|---|---|
| SW Access:Reset | R/WC:0 | R/WC:0 | R/WC:0 | R/WC:0 | R/W:0000 | | | |
| HW Access | W | W | W | W | R/W | | | |
| Name | setup_rcvd | in_rcvd | out_rcvd | acked_txn | mode | | | |

The Endpoint Control Register (EP0_CR) is used to configure endpoint 0. Because both firmware and the SIE are allowed to write to the Endpoint 0 Control and Count registers the SIE provides an interlocking mechanism to prevent accidental overwriting of data. When the SIE writes to these registers they are locked and the processor cannot write to them until after reading the EP0_CR register. Writing to this register clears the upper four bits regardless of the value written. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|------------|--|
| 7 | setup_rcvd | When set this bit indicates a valid SETUP packet was received and ACKed. This bit is forced HIGH from the start of the data packet phase of the SETUP transaction until the start of the ACK packet returned by the SIE. The CPU is prevented from clearing this bit during this interval. After this interval the bit will remain set until cleared by firmware. While this bit is set to '1' the CPU cannot write to the EP0_DRx registers. This prevents firmware from overwriting an incoming SETUP transaction before firmware has a chance to read the SETUP data. This bit is cleared by any non-locked writes to the register. Sticky (individual bits) |
| 6 | in_rcvd | When set this bit indicates a valid IN packet has been received. This bit is updated to '1' after the host acknowledges an IN data packet. When clear this bit indicates either no IN has been received or that the host did not acknowledge the IN data by sending ACK handshake. It is cleared by any non-locked writes to the register. Sticky (individual bits) |
| 5 | out_rcvd | When set this bit indicates a valid OUT packet has been received and ACKed. This bit is updated to '1' after the last received packet in an OUT transaction. When clear this bit indicates no OUT received. It is cleared by any non-locked writes to the register. Sticky (individual bits) |
| 4 | acked_txn | This bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with a ACK packet. This bit is cleared by any nonlocked writes to the register. Sticky (individual bits) |
| 3:0 | mode[3:0] | The mode bits control how the USB SIE responds to traffic and how the USB SIE will change the mode of that endpoint as a result of host packets to the endpoint. |

1.3.580 USB_EP0_CNT

Endpoint0 count Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_EP0_CNT: 0x40006029

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|------------|-------|---|------------|---|---|---|
| SW Access:Reset | R/W:0 | R/WZC:0 | NA:00 | | R/W:0000 | | | |
| HW Access | R/W | W | NA | | R/W | | | |
| Name | data_toggle | data_valid | | | byte_count | | | |

The Endpoint 0 Count Register (EP0_CNT) is used to configure endpoint 0. Whenever the count updates from a SETUP or OUT transaction this register locks and can not be written by the CPU. Reading the EP0_CR register unlocks this register. This prevents firmware from overwriting a status update on incoming SETUP or OUT transactions before firmware has a chance to read the data. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------------|---|
| 7 | data_toggle | This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit. For OUT or SETUP transactions the SIE hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1 |
| 6 | data_valid | This bit indicates whether there were errors in OUT or SETUP transactions. It is cleared to '0' if CRC bit stuff or PID errors have occurred. This bit does not update for some endpoint mode settings. This bit may be cleared by writing a zero to it when the register is not locked. 0- Error in data received. 1- No Errors Sticky (individual bits) |
| 3:0 | byte_count[3:0] | These bits indicate the number of data bytes in a transaction. For IN transactions firmware loads the count with the number of bytes to be transmitted to the host from the endpoint FIFO. Valid values are 0 to 8. For OUT or SETUP transactions the count is updated by hardware to the number of data bytes received plus two for the CRC bytes. Valid values are 2 to 10. |

1.3.581 USB_SIE_EP3_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP3_CNT0: 0x4000602C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|------------|--------|---|---|----------------|---|---|
| SW Access:Reset | R/W:0 | R/WZC:0 | NA:000 | | | R/W:000 | | |
| HW Access | R/W | W | NA | | | R/W | | |
| Name | data_toggle | data_valid | | | | data_count_msb | | |

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|---------------------|---|
| 7 | data_toggle | This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1 |
| 6 | data_valid | This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits) |
| 2:0 | data_count_msb[2:0] | These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information. |

1.3.582 USB_SIE_EP3_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP3_CNT1: 0x4000602D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_count | | | | | | | |

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater than the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | data_count[7:0] | These bits are the 8 LSb of a 11-bit counter. The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction. |



0x4000602d

1.3.583 USB_SIE_EP3_CR0

Propname Non-control endpoint's control Register

0x4000602eDomain reset for non-retention flops [reset_all_nonretention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.584 USB_SIE_EP4_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP4_CNT0: 0x4000603C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|------------|--------|---|---|----------------|---|---|
| SW Access:Reset | R/W:0 | R/WZC:0 | NA:000 | | | R/W:000 | | |
| HW Access | R/W | W | NA | | | R/W | | |
| Name | data_toggle | data_valid | | | | data_count_msb | | |

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|---------------------|---|
| 7 | data_toggle | This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1 |
| 6 | data_valid | This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits) |
| 2:0 | data_count_msb[2:0] | These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information. |

1.3.585 USB_SIE_EP4_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP4_CNT1: 0x4000603D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_count | | | | | | | |

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater than the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | data_count[7:0] | These bits are the 8 LSb of a 11-bit counter. The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction. |

1.3.586 USB_SIE_EP4_CR0

| | |
|------------------|---|
| Proprname | Non-control endpoint's control Register |
|------------------|---|

0x4000603eDomain reset for non-retention flops [reset_all_nonretention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.587 USB_SIE_EP5_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP5_CNT0: 0x4000604C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|------------|--------|---|---|----------------|---|---|
| SW Access:Reset | R/W:0 | R/WZC:0 | NA:000 | | | R/W:000 | | |
| HW Access | R/W | W | NA | | | R/W | | |
| Name | data_toggle | data_valid | | | | data_count_msb | | |

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|---------------------|---|
| 7 | data_toggle | This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1 |
| 6 | data_valid | This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits) |
| 2:0 | data_count_msb[2:0] | These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information. |

1.3.588 USB_SIE_EP5_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP5_CNT1: 0x4000604D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_count | | | | | | | |

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater than the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | data_count[7:0] | These bits are the 8 LSb of a 11-bit counter. The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction. |



0x4000604d

1.3.589 USB_SIE_EP5_CR0

Propname Non-control endpoint's control Register

0x4000604eDomain reset for non-retention flops [reset_all_nonretention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.590 USB_SIE_EP6_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP6_CNT0: 0x4000605C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|------------|--------|---|---|----------------|---|---|
| SW Access:Reset | R/W:0 | R/WZC:0 | NA:000 | | | R/W:000 | | |
| HW Access | R/W | W | NA | | | R/W | | |
| Name | data_toggle | data_valid | | | | data_count_msb | | |

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|---------------------|---|
| 7 | data_toggle | This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1 |
| 6 | data_valid | This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits) |
| 2:0 | data_count_msb[2:0] | These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information. |

1.3.591 USB_SIE_EP6_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP6_CNT1: 0x4000605D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_count | | | | | | | |

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater than the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | data_count[7:0] | These bits are the 8 LSb of a 11-bit counter. The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction. |

1.3.592 USB_SIE_EP6_CR0

| | |
|------------------|---|
| Proprname | Non-control endpoint's control Register |
|------------------|---|

0x4000605eDomain reset for non-retention flops [reset_all_nonretention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.593 USB_SIE_EP7_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP7_CNT0: 0x4000606C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|------------|--------|---|---|----------------|---|---|
| SW Access:Reset | R/W:0 | R/WZC:0 | NA:000 | | | R/W:000 | | |
| HW Access | R/W | W | NA | | | R/W | | |
| Name | data_toggle | data_valid | | | | data_count_msb | | |

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|---------------------|---|
| 7 | data_toggle | This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1 |
| 6 | data_valid | This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits) |
| 2:0 | data_count_msb[2:0] | These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information. |

1.3.594 USB_SIE_EP7_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP7_CNT1: 0x4000606D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_count | | | | | | | |

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater than the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | data_count[7:0] | These bits are the 8 LSb of a 11-bit counter. The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction. |



0x4000606d

1.3.595 USB_SIE_EP7_CR0

Propname Non-control endpoint's control Register

0x4000606eDomain reset for non-retention flops [reset_all_nonretention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.596 USB_SIE_EP8_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP8_CNT0: 0x4000607C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|------------|--------|---|---|----------------|---|---|
| SW Access:Reset | R/W:0 | R/WZC:0 | NA:000 | | | R/W:000 | | |
| HW Access | R/W | W | NA | | | R/W | | |
| Name | data_toggle | data_valid | | | | data_count_msb | | |

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|---------------------|---|
| 7 | data_toggle | This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1 |
| 6 | data_valid | This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits) |
| 2:0 | data_count_msb[2:0] | These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information. |

1.3.597 USB_SIE_EP8_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP8_CNT1: 0x4000607D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_count | | | | | | | |

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater than the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | data_count[7:0] | These bits are the 8 LSb of a 11-bit counter. The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction. |

1.3.598 USB_SIE_EP8_CR0

| | |
|------------------|---|
| Proprname | Non-control endpoint's control Register |
|------------------|---|

0x4000607eDomain reset for non-retention flops [reset_all_nonretention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.599 USB_ARB_EP1_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP1_CFG: 0x40006080

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|------------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | reset_ptr | crc_bypass | dma_req | in_data_rdy |

Endpoint Configuration Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---|
| 3 | reset_ptr | Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes. |
| 2 | crc_bypass | Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s |
| 1 | dma_req | Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request |
| 0 | in_data_rdy | Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive. |

1.3.600 USB_ARB_EP1_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP1_INT_EN: 0x40006081

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|------------|--------------|-------------|------------|----------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | err_int_en | buf_under_en | buf_over_en | dma_gnt_en | in_buf_full_en |

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------------|--|
| 4 | err_int_en | Endpoint Error in Transaction Interrupt Enable |
| 3 | buf_under_en | Endpoint Buffer Underflow Enable |
| 2 | buf_over_en | Endpoint Buffer Overflow Enable |
| 1 | dma_gnt_en | Endpoint DMA Grant Enable |
| 0 | in_buf_full_en | IN Endpoint Local Buffer Full Enable |

1.3.601 USB_ARB_EP1_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP1_SR: 0x40006082

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|----------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | buf_under | buf_over | dma_gnt | in_buf_full |

Endpoint Status Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|--|
| 3 | buf_under | Endpoint Buffer Underflow Indication |
| 2 | buf_over | Endpoint Buffer Overflow Indication |
| 1 | dma_gnt | Endpoint DMA Grant Indication |
| 0 | in_buf_full | IN Endpoint Local Buffer Full Indication |

1.3.602 USB_ARB_RW1_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW1_WA: 0x40006084

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | wa | | | | | | | |

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|----------------------|
| 7:0 | wa[7:0] | Write Address for EP |



0x40006085

1.3.603 USB_ARB_RW1_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW1_WA_MSB: 0x40006085

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | wa_msb |

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|----------------------|
| 0 | wa_msb | Write Address for EP |

1.3.604 USB_ARB_RW1_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW1_RA: 0x40006086

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ra | | | | | | | |

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---------------------|
| 7:0 | ra[7:0] | Read Address for EP |

1.3.605 USB_ARB_RW1_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW1_RA_MSB: 0x40006087

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | ra_msb |

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|---------------------|
| 0 | ra_msb | Read Address for EP |

1.3.606 USB_ARB_RW1_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW1_DR: 0x40006088

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dr | | | | | | | |

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---|
| 7:0 | dr[7:0] | Data Register for EP ; This register is linked to the memory, hence reset value is undefined. |

1.3.607 USB_BUF_SIZE

Dedicated Endpoint Buffer Size Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_BUF_SIZE: 0x4000608C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0000 | | | | R/W:0000 | | | |
| HW Access | R | | | | R | | | |
| Name | out_buf | | | | in_buf | | | |

Dedicated buffer size for IN and OUT type Endpoints; Encoded power of 2 value; Eg: 1 => 2 bytes; 2 => 4 bytes; 9 => 512 bytes This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------------|--------------------------------|
| 7:4 | out_buf[3:0] | Buffer size for OUT Endpoints. |
| 3:0 | in_buf[3:0] | Buffer size for IN Endpoints. |

1.3.608 USB_EP_ACTIVE

Endpoint Active Indication Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_EP_ACTIVE: 0x4000608E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | ep8_act | ep7_act | ep6_act | ep5_act | ep4_act | ep3_act | ep2_act | ep1_act |

Endpoint Active Register; Indicates if an Endpoint is active or not; Required to be programmed only in the case of Automatic Memory Management mode of operation. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|--|
| 7 | ep8_act | Endpoint 8 Active Indication. 0: Inactive. 1: Active |
| 6 | ep7_act | Endpoint 7 Active Indication. 0: Inactive. 1: Active |
| 5 | ep6_act | Endpoint 6 Active Indication. 0: Inactive. 1: Active |
| 4 | ep5_act | Endpoint 5 Active Indication. 0: Inactive. 1: Active |
| 3 | ep4_act | Endpoint 4 Active Indication. 0: Inactive. 1: Active |
| 2 | ep3_act | Endpoint 3 Active Indication. 0: Inactive. 1: Active |
| 1 | ep2_act | Endpoint 2 Active Indication. 0: Inactive. 1: Active |
| 0 | ep1_act | Endpoint 1 Active Indication. 0: Inactive. 1: Active |

1.3.609 USB_EP_TYPE

Endpoint Type (IN/OUT) Indication

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_EP_TYPE: 0x4000608F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | ep8_typ | ep7_typ | ep6_typ | ep5_typ | ep4_typ | ep3_typ | ep2_typ | ep1_typ |

Endpoint Type Register; Indicates the Endpoint Type as IN / OUT. Value is valid if EP_ACTIVE bit is set for the corresponding Endpoint. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---|
| 7 | ep8_typ | Endpoint 8 Type Indication. 0: IN. 1: OUT |
| 6 | ep7_typ | Endpoint 7 Type Indication. 0: IN. 1: OUT |
| 5 | ep6_typ | Endpoint 6 Type Indication. 0: IN. 1: OUT |
| 4 | ep5_typ | Endpoint 5 Type Indication. 0: IN. 1: OUT |
| 3 | ep4_typ | Endpoint 4 Type Indication. 0: IN. 1: OUT |
| 2 | ep3_typ | Endpoint 3 Type Indication. 0: IN. 1: OUT |
| 1 | ep2_typ | Endpoint 2 Type Indication. 0: IN. 1: OUT |
| 0 | ep1_typ | Endpoint 1 Type Indication. 0: IN. 1: OUT |

1.3.610 USB_ARB_EP2_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP2_CFG: 0x40006090

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|------------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | reset_ptr | crc_bypass | dma_req | in_data_rdy |

Endpoint Configuration Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---|
| 3 | reset_ptr | Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes. |
| 2 | crc_bypass | Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s |
| 1 | dma_req | Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request |
| 0 | in_data_rdy | Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive. |

1.3.611 USB_ARB_EP2_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP2_INT_EN: 0x40006091

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|------------|--------------|-------------|------------|----------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | err_int_en | buf_under_en | buf_over_en | dma_gnt_en | in_buf_full_en |

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------------|--|
| 4 | err_int_en | Endpoint Error in Transaction Interrupt Enable |
| 3 | buf_under_en | Endpoint Buffer Underflow Enable |
| 2 | buf_over_en | Endpoint Buffer Overflow Enable |
| 1 | dma_gnt_en | Endpoint DMA Grant Enable |
| 0 | in_buf_full_en | IN Endpoint Local Buffer Full Enable |

1.3.612 USB_ARB_EP2_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP2_SR: 0x40006092

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|----------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | buf_under | buf_over | dma_gnt | in_buf_full |

Endpoint Status Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|--|
| 3 | buf_under | Endpoint Buffer Underflow Indication |
| 2 | buf_over | Endpoint Buffer Overflow Indication |
| 1 | dma_gnt | Endpoint DMA Grant Indication |
| 0 | in_buf_full | IN Endpoint Local Buffer Full Indication |

1.3.613 USB_ARB_RW2_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW2_WA: 0x40006094

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | wa | | | | | | | |

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|----------------------|
| 7:0 | wa[7:0] | Write Address for EP |

1.3.614 USB_ARB_RW2_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW2_WA_MSB: 0x40006095

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | wa_msb |

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|----------------------|
| 0 | wa_msb | Write Address for EP |

1.3.615 USB_ARB_RW2_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW2_RA: 0x40006096

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ra | | | | | | | |

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---------------------|
| 7:0 | ra[7:0] | Read Address for EP |

1.3.616 USB_ARB_RW2_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW2_RA_MSB: 0x40006097

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | ra_msb |

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|---------------------|
| 0 | ra_msb | Read Address for EP |

0x40006098

1.3.617 USB_ARB_RW2_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW2_DR: 0x40006098

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dr | | | | | | | |

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---|
| 7:0 | dr[7:0] | Data Register for EP ; This register is linked to the memory, hence reset value is undefined. |

1.3.618 USB_ARB_CFG

Arbiter Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_CFG: 0x4000609C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---------|---|----------|---------|---|---|---|
| SW Access:Reset | R/W:0 | R/W:00 | | R/W:0 | NA:0000 | | | |
| HW Access | R | R | | R | NA | | | |
| Name | cfg_cmp | dma_cfg | | auto_mem | | | | |

Arbiter Configuration Register. For MODE I Operation: This register can be left in its default state. For MODE II and MODE III Operation: This register should be programmed. Cfg_cmp bit set to 0 during configuration of PFSUSB Registers. Cfg_cmp bit set to 1 once configuration is complete. This should then be held at 1 during functional mode. Similarly auto_mem and dma_cfg settings are static and should not be modified during block operation. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------------|--|
| 7 | cfg_cmp | Register Configuration Complete Indication. Posedge is detected on this bit. Hence a 0 to 1 transition is required. 0: Configuration in progress. 1: Configuration complete. |
| 6:5 | dma_cfg[1:0] | DMA Access Configuration. 00: No DMA. 01: Manual DMA. 10: Auto DMA and Manual DMA. 11: Reserved. |
| 4 | auto_mem | Auto / Manual Memory Configuration. 0: Manual Memory Config (CPU). 1: Auto Memory Config |

1.3.619 USB_USB_CLK_EN

USB Block Clock Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_USB_CLK_EN: 0x4000609D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|------------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | csr_clk_en |

USB Block Clock Enable Register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|------------|--|
| 0 | csr_clk_en | Clock Enable for Core Logic clocked by AHB bus clock |

1.3.620 USB_ARB_INT_EN

Arbiter Interrupt Enable

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_INT_EN: 0x4000609E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | ep8_intr_en | ep7_intr_en | ep6_intr_en | ep5_intr_en | ep4_intr_en | ep3_intr_en | ep2_intr_en | ep1_intr_en |

Arbiter Interrupt Enable Register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---|
| 7 | ep8_intr_en | EP8 Interrupt Enable. 0: Do not raise EP8 Interrupt. 1: Raise EP8 Interrupt |
| 6 | ep7_intr_en | EP7 Interrupt Enable. 0: Do not raise EP7 Interrupt. 1: Raise EP7 Interrupt |
| 5 | ep6_intr_en | EP6 Interrupt Enable. 0: Do not raise EP6 Interrupt. 1: Raise EP6 Interrupt |
| 4 | ep5_intr_en | EP5 Interrupt Enable. 0: Do not raise EP5 Interrupt. 1: Raise EP5 Interrupt |
| 3 | ep4_intr_en | EP4 Interrupt Enable. 0: Do not raise EP4 Interrupt. 1: Raise EP4 Interrupt |
| 2 | ep3_intr_en | EP3 Interrupt Enable. 0: Do not raise EP3 Interrupt. 1: Raise EP3 Interrupt |
| 1 | ep2_intr_en | EP2 Interrupt Enable. 0: Do not raise EP2 Interrupt. 1: Raise EP2 Interrupt |
| 0 | ep1_intr_en | EP1 Interrupt Enable. 0: Do not raise EP1 Interrupt. 1: Raise EP1 Interrupt |

1.3.621 USB_ARB_INT_SR

Arbiter Interrupt Status

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_INT_SR: 0x4000609F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|----------|----------|----------|----------|----------|----------|----------|
| SW Access:Reset | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | ep8_intr | ep7_intr | ep6_intr | ep5_intr | ep4_intr | ep3_intr | ep2_intr | ep1_intr |

Arbiter Status Register. This is an Interrupt Status Register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------|---|
| 7 | ep8_intr | EP8 Interrupt Status. 0: EP8 Interrupt not raised. 1: EP8 Interrupt Present |
| 6 | ep7_intr | EP7 Interrupt Status. 0: EP7 Interrupt not raised. 1: EP7 Interrupt Present |
| 5 | ep6_intr | EP6 Interrupt Status. 0: EP6 Interrupt not raised. 1: EP6 Interrupt Present |
| 4 | ep5_intr | EP5 Interrupt Status. 0: EP5 Interrupt not raised. 1: EP5 Interrupt Present |
| 3 | ep4_intr | EP4 Interrupt Status. 0: EP4 Interrupt not raised. 1: EP4 Interrupt Present |
| 2 | ep3_intr | EP3 Interrupt Status. 0: EP3 Interrupt not raised. 1: EP3 Interrupt Present |
| 1 | ep2_intr | EP2 Interrupt Status. 0: EP2 Interrupt not raised. 1: EP2 Interrupt Present |
| 0 | ep1_intr | EP1 Interrupt Status. 0: EP1 Interrupt not raised. 1: EP1 Interrupt Present |

1.3.622 USB_ARB_EP3_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP3_CFG: 0x400060A0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|------------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | reset_ptr | crc_bypass | dma_req | in_data_rdy |

Endpoint Configuration Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---|
| 3 | reset_ptr | Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes. |
| 2 | crc_bypass | Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s |
| 1 | dma_req | Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request |
| 0 | in_data_rdy | Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive. |

1.3.623 USB_ARB_EP3_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP3_INT_EN: 0x400060A1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|------------|--------------|-------------|------------|----------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | err_int_en | buf_under_en | buf_over_en | dma_gnt_en | in_buf_full_en |

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------------|--|
| 4 | err_int_en | Endpoint Error in Transaction Interrupt Enable |
| 3 | buf_under_en | Endpoint Buffer Underflow Enable |
| 2 | buf_over_en | Endpoint Buffer Overflow Enable |
| 1 | dma_gnt_en | Endpoint DMA Grant Enable |
| 0 | in_buf_full_en | IN Endpoint Local Buffer Full Enable |

1.3.624 USB_ARB_EP3_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP3_SR: 0x400060A2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|----------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | buf_under | buf_over | dma_gnt | in_buf_full |

Endpoint Status Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|--|
| 3 | buf_under | Endpoint Buffer Underflow Indication |
| 2 | buf_over | Endpoint Buffer Overflow Indication |
| 1 | dma_gnt | Endpoint DMA Grant Indication |
| 0 | in_buf_full | IN Endpoint Local Buffer Full Indication |

1.3.625 USB_ARB_RW3_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW3_WA: 0x400060A4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | wa | | | | | | | |

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|----------------------|
| 7:0 | wa[7:0] | Write Address for EP |

1.3.626 USB_ARB_RW3_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW3_WA_MSB: 0x400060A5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | wa_msb |

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|----------------------|
| 0 | wa_msb | Write Address for EP |

1.3.627 USB_ARB_RW3_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW3_RA: 0x400060A6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ra | | | | | | | |

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---------------------|
| 7:0 | ra[7:0] | Read Address for EP |

1.3.628 USB_ARB_RW3_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW3_RA_MSB: 0x400060A7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | ra_msb |

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|---------------------|
| 0 | ra_msb | Read Address for EP |

0x400060a8

1.3.629 USB_ARB_RW3_DR Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW3_DR: 0x400060A8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dr | | | | | | | |

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---|
| 7:0 | dr[7:0] | Data Register for EP ; This register is linked to the memory, hence reset value is undefined. |

1.3.630 USB_CWA

Common Area Write Address

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_CWA: 0x400060AC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cwa | | | | | | | |

Write Address Pointer for Common Area; LSB 8 bits of the 9 bit pointer are stored in this register. This register is only valid in Mode3 operation. Although it is R/W register for CPU, all intended updates are performed by the block and CPU can access the value for debug purposes. This register will indicate the Common Area location in memory. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------|-------------------------------|
| 7:0 | cwa[7:0] | Write Address for Common Area |

1.3.631 USB_CWA_MSB

Common Area Write Address

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_CWA_MSB: 0x400060AD

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | cwa_msb |

Write Address Pointer for Common Area; MSB of the 9 bit pointer are stored in this register. This register is only valid in Mode3 operation. Although it is R/W register for CPU, all intended updates are performed by the block and CPU can access the value for debug purposes. This register will indicate the Common Area location in memory. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|-------------------------------|
| 0 | cwa_msb | Write Address for Common Area |

1.3.632 USB_ARB_EP4_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP4_CFG: 0x400060B0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|------------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | reset_ptr | crc_bypass | dma_req | in_data_rdy |

Endpoint Configuration Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---|
| 3 | reset_ptr | Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes. |
| 2 | crc_bypass | Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s |
| 1 | dma_req | Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request |
| 0 | in_data_rdy | Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive. |

1.3.633 USB_ARB_EP4_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP4_INT_EN: 0x400060B1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|------------|--------------|-------------|------------|----------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | err_int_en | buf_under_en | buf_over_en | dma_gnt_en | in_buf_full_en |

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------------|--|
| 4 | err_int_en | Endpoint Error in Transaction Interrupt Enable |
| 3 | buf_under_en | Endpoint Buffer Underflow Enable |
| 2 | buf_over_en | Endpoint Buffer Overflow Enable |
| 1 | dma_gnt_en | Endpoint DMA Grant Enable |
| 0 | in_buf_full_en | IN Endpoint Local Buffer Full Enable |

1.3.634 USB_ARB_EP4_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP4_SR: 0x400060B2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|----------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | buf_under | buf_over | dma_gnt | in_buf_full |

Endpoint Status Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|--|
| 3 | buf_under | Endpoint Buffer Underflow Indication |
| 2 | buf_over | Endpoint Buffer Overflow Indication |
| 1 | dma_gnt | Endpoint DMA Grant Indication |
| 0 | in_buf_full | IN Endpoint Local Buffer Full Indication |

1.3.635 USB_ARB_RW4_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW4_WA: 0x400060B4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | wa | | | | | | | |

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|----------------------|
| 7:0 | wa[7:0] | Write Address for EP |

1.3.636 USB_ARB_RW4_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW4_WA_MSB: 0x400060B5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | wa_msb |

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|----------------------|
| 0 | wa_msb | Write Address for EP |

1.3.637 USB_ARB_RW4_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW4_RA: 0x400060B6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ra | | | | | | | |

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---------------------|
| 7:0 | ra[7:0] | Read Address for EP |

1.3.638 USB_ARB_RW4_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW4_RA_MSB: 0x400060B7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | ra_msb |

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|---------------------|
| 0 | ra_msb | Read Address for EP |

0x400060b8

1.3.639 USB_ARB_RW4_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW4_DR: 0x400060B8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dr | | | | | | | |

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---|
| 7:0 | dr[7:0] | Data Register for EP ; This register is linked to the memory, hence reset value is undefined. |

1.3.640 USB_DMA_THRES

DMA Burst / Threshold Configuration

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_DMA_THRES: 0x400060BC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dma_ths | | | | | | | |

It contains 8 LSB bits of DMA Threshold Register This register is only valid in Mode3 operation. This register should be programmed to the same value as the DMA Burst Count programmed in the corresponding Channel Basic Config Register in PHUB. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | dma_ths[7:0] | 8 Lsb bits of 9 bit DMA Threshold count. |

1.3.641 USB_DMA_THRES_MSB

DMA Burst / Threshold Configuration

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_DMA_THRES_MSB: 0x400060BD

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|-------------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | dma_ths_msb |

It contains the MSB bit of DMA Threshold Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---------------------------------------|
| 0 | dma_ths_msb | Msb bit of 9 bit DMA Threshold count. |

1.3.642 USB_ARB_EP5_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP5_CFG: 0x400060C0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|------------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | reset_ptr | crc_bypass | dma_req | in_data_rdy |

Endpoint Configuration Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---|
| 3 | reset_ptr | Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes. |
| 2 | crc_bypass | Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s |
| 1 | dma_req | Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request |
| 0 | in_data_rdy | Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive. |

1.3.643 USB_ARB_EP5_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP5_INT_EN: 0x400060C1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|------------|--------------|-------------|------------|----------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | err_int_en | buf_under_en | buf_over_en | dma_gnt_en | in_buf_full_en |

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------------|--|
| 4 | err_int_en | Endpoint Error in Transaction Interrupt Enable |
| 3 | buf_under_en | Endpoint Buffer Underflow Enable |
| 2 | buf_over_en | Endpoint Buffer Overflow Enable |
| 1 | dma_gnt_en | Endpoint DMA Grant Enable |
| 0 | in_buf_full_en | IN Endpoint Local Buffer Full Enable |

1.3.644 USB_ARB_EP5_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP5_SR: 0x400060C2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|----------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | buf_under | buf_over | dma_gnt | in_buf_full |

Endpoint Status Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|--|
| 3 | buf_under | Endpoint Buffer Underflow Indication |
| 2 | buf_over | Endpoint Buffer Overflow Indication |
| 1 | dma_gnt | Endpoint DMA Grant Indication |
| 0 | in_buf_full | IN Endpoint Local Buffer Full Indication |

1.3.645 USB_ARB_RW5_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW5_WA: 0x400060C4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | wa | | | | | | | |

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|----------------------|
| 7:0 | wa[7:0] | Write Address for EP |

1.3.646 USB_ARB_RW5_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW5_WA_MSB: 0x400060C5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | wa_msb |

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|----------------------|
| 0 | wa_msb | Write Address for EP |

1.3.647 USB_ARB_RW5_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW5_RA: 0x400060C6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ra | | | | | | | |

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---------------------|
| 7:0 | ra[7:0] | Read Address for EP |

1.3.648 USB_ARB_RW5_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW5_RA_MSB: 0x400060C7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | ra_msb |

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|---------------------|
| 0 | ra_msb | Read Address for EP |

1.3.649 USB_ARB_RW5_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW5_DR: 0x400060C8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dr | | | | | | | |

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---|
| 7:0 | dr[7:0] | Data Register for EP ; This register is linked to the memory, hence reset value is undefined. |

1.3.650 USB_BUS_RST_CNT

Bus Reset Count Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_BUS_RST_CNT: 0x400060CC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-------------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:1010 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | bus_rst_cnt | | | |

Bus Reset Count register ; For USB bus reset length; The value in this register determines the no. of pulses of the low freq. clock which will be counted to determine if an SE0 condition has been held for long enough to declare a USB Bus reset condition. In krypton, 3 pulses of a 32 KHz clock were counted to declare a usb bus reset condition. In leopard, a 100 KHz clock is used. Recommended is to count 10 pulses of this clock to remain equivalent to Krypton. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|------------------|------------------------|
| 3:0 | bus_rst_cnt[3:0] | Bus Reset Count Length |

1.3.651 USB_ARB_EP6_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP6_CFG: 0x400060D0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|------------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | reset_ptr | crc_bypass | dma_req | in_data_rdy |

Endpoint Configuration Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---|
| 3 | reset_ptr | Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes. |
| 2 | crc_bypass | Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s |
| 1 | dma_req | Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request |
| 0 | in_data_rdy | Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive. |

1.3.652 USB_ARB_EP6_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP6_INT_EN: 0x400060D1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|------------|--------------|-------------|------------|----------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | err_int_en | buf_under_en | buf_over_en | dma_gnt_en | in_buf_full_en |

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------------|--|
| 4 | err_int_en | Endpoint Error in Transaction Interrupt Enable |
| 3 | buf_under_en | Endpoint Buffer Underflow Enable |
| 2 | buf_over_en | Endpoint Buffer Overflow Enable |
| 1 | dma_gnt_en | Endpoint DMA Grant Enable |
| 0 | in_buf_full_en | IN Endpoint Local Buffer Full Enable |

1.3.653 USB_ARB_EP6_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP6_SR: 0x400060D2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|----------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | buf_under | buf_over | dma_gnt | in_buf_full |

Endpoint Status Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|--|
| 3 | buf_under | Endpoint Buffer Underflow Indication |
| 2 | buf_over | Endpoint Buffer Overflow Indication |
| 1 | dma_gnt | Endpoint DMA Grant Indication |
| 0 | in_buf_full | IN Endpoint Local Buffer Full Indication |

1.3.654 USB_ARB_RW6_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW6_WA: 0x400060D4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | wa | | | | | | | |

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|----------------------|
| 7:0 | wa[7:0] | Write Address for EP |

0x400060d5

1.3.655 USB_ARB_RW6_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW6_WA_MSB: 0x400060D5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | wa_msb |

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|----------------------|
| 0 | wa_msb | Write Address for EP |

1.3.656 USB_ARB_RW6_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW6_RA: 0x400060D6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ra | | | | | | | |

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---------------------|
| 7:0 | ra[7:0] | Read Address for EP |

0x400060d7

1.3.657 USB_ARB_RW6_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW6_RA_MSB: 0x400060D7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | ra_msb |

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|---------------------|
| 0 | ra_msb | Read Address for EP |

1.3.658 USB_ARB_RW6_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW6_DR: 0x400060D8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dr | | | | | | | |

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---|
| 7:0 | dr[7:0] | Data Register for EP ; This register is linked to the memory, hence reset value is undefined. |

1.3.659 USB_ARB_EP7_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP7_CFG: 0x400060E0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|------------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | reset_ptr | crc_bypass | dma_req | in_data_rdy |

Endpoint Configuration Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---|
| 3 | reset_ptr | Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes. |
| 2 | crc_bypass | Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s |
| 1 | dma_req | Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request |
| 0 | in_data_rdy | Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive. |

1.3.660 USB_ARB_EP7_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP7_INT_EN: 0x400060E1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|------------|--------------|-------------|------------|----------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | err_int_en | buf_under_en | buf_over_en | dma_gnt_en | in_buf_full_en |

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------------|--|
| 4 | err_int_en | Endpoint Error in Transaction Interrupt Enable |
| 3 | buf_under_en | Endpoint Buffer Underflow Enable |
| 2 | buf_over_en | Endpoint Buffer Overflow Enable |
| 1 | dma_gnt_en | Endpoint DMA Grant Enable |
| 0 | in_buf_full_en | IN Endpoint Local Buffer Full Enable |

1.3.661 USB_ARB_EP7_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP7_SR: 0x400060E2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|----------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | buf_under | buf_over | dma_gnt | in_buf_full |

Endpoint Status Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|--|
| 3 | buf_under | Endpoint Buffer Underflow Indication |
| 2 | buf_over | Endpoint Buffer Overflow Indication |
| 1 | dma_gnt | Endpoint DMA Grant Indication |
| 0 | in_buf_full | IN Endpoint Local Buffer Full Indication |

1.3.662 USB_ARB_RW7_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW7_WA: 0x400060E4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | wa | | | | | | | |

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|----------------------|
| 7:0 | wa[7:0] | Write Address for EP |

0x400060e5

1.3.663 USB_ARB_RW7_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW7_WA_MSB: 0x400060E5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | wa_msb |

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|----------------------|
| 0 | wa_msb | Write Address for EP |

1.3.664 USB_ARB_RW7_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW7_RA: 0x400060E6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ra | | | | | | | |

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---------------------|
| 7:0 | ra[7:0] | Read Address for EP |

1.3.665 USB_ARB_RW7_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW7_RA_MSB: 0x400060E7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | ra_msb |

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|---------------------|
| 0 | ra_msb | Read Address for EP |

1.3.666 USB_ARB_RW7_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW7_DR: 0x400060E8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dr | | | | | | | |

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---|
| 7:0 | dr[7:0] | Data Register for EP ; This register is linked to the memory, hence reset value is undefined. |

1.3.667 USB_ARB_EP8_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP8_CFG: 0x400060F0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|------------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | reset_ptr | crc_bypass | dma_req | in_data_rdy |

Endpoint Configuration Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|---|
| 3 | reset_ptr | Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes. |
| 2 | crc_bypass | Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s |
| 1 | dma_req | Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request |
| 0 | in_data_rdy | Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive. |

1.3.668 USB_ARB_EP8_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP8_INT_EN: 0x400060F1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|------------|--------------|-------------|------------|----------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | err_int_en | buf_under_en | buf_over_en | dma_gnt_en | in_buf_full_en |

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|----------------|--|
| 4 | err_int_en | Endpoint Error in Transaction Interrupt Enable |
| 3 | buf_under_en | Endpoint Buffer Underflow Enable |
| 2 | buf_over_en | Endpoint Buffer Overflow Enable |
| 1 | dma_gnt_en | Endpoint DMA Grant Enable |
| 0 | in_buf_full_en | IN Endpoint Local Buffer Full Enable |

1.3.669 USB_ARB_EP8_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP8_SR: 0x400060F2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|----------|---------|-------------|
| SW Access:Reset | NA:0000 | | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | buf_under | buf_over | dma_gnt | in_buf_full |

Endpoint Status Register This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|-------------|--|
| 3 | buf_under | Endpoint Buffer Underflow Indication |
| 2 | buf_over | Endpoint Buffer Overflow Indication |
| 1 | dma_gnt | Endpoint DMA Grant Indication |
| 0 | in_buf_full | IN Endpoint Local Buffer Full Indication |

1.3.670 USB_ARB_RW8_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW8_WA: 0x400060F4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | wa | | | | | | | |

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|----------------------|
| 7:0 | wa[7:0] | Write Address for EP |

0x400060f5

1.3.671 USB_ARB_RW8_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW8_WA_MSB: 0x400060F5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | wa_msb |

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|----------------------|
| 0 | wa_msb | Write Address for EP |

1.3.672 USB_ARB_RW8_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW8_RA: 0x400060F6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ra | | | | | | | |

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---------------------|
| 7:0 | ra[7:0] | Read Address for EP |

0x400060f7

1.3.673 USB_ARB_RW8_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW8_RA_MSB: 0x400060F7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | ra_msb |

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|--------|---------------------|
| 0 | ra_msb | Read Address for EP |

1.3.674 USB_ARB_RW8_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW8_DR: 0x400060F8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dr | | | | | | | |

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

| Bits | Name | Description |
|------|---------|---|
| 7:0 | dr[7:0] | Data Register for EP ; This register is linked to the memory, hence reset value is undefined. |

@0x40006100 + [0..511 * 0x1]

1.3.675 USB_MEM_DATA[0..511] DATA

Reset: N/A

Register : Address

USB_MEM_DATA: 0x40006100-0x400062FF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

The memory for the PFSUSB block is 256x16 S8 SRAM. Any access to address space 0x100 - 0x2FF puts the block into memory test mode and offers direct read/write access to the 512 memory byte locations.

| Bits | Name | Description |
|------|-----------|------------------|
| 7:0 | data[7:0] | (no description) |

1.3.676 B[0..3]_UDB00_A0

UDB00_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_A0: 0x40006400

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.677 B[0..3]_UDB01_A0

UDB01_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_A0: 0x40006401

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.678 B[0..3]_UDB02_A0

UDB02_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_A0: 0x40006402

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.679 B[0..3]_UDB03_A0

UDB03_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_A0: 0x40006403

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.680 B[0..3]_UDB04_A0

UDB04_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_A0: 0x40006404

B1_UDB04_A0: 0x40006504

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.681 B[0..3]_UDB05_A0

UDB05_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_A0: 0x40006405

B1_UDB05_A0: 0x40006505

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.682 B[0..3]_UDB06_A0

UDB06_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_A0: 0x40006406

B1_UDB06_A0: 0x40006506

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.683 B[0..3]_UDB07_A0

UDB07_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_A0: 0x40006407

B1_UDB07_A0: 0x40006507

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.684 B[0..3]_UDB08_A0

UDB08_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_A0: 0x40006408

B1_UDB08_A0: 0x40006508

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.685 B[0..3]_UDB09_A0

UDB09_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_A0: 0x40006409

B1_UDB09_A0: 0x40006509

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.686 B[0..3]_UDB10_A0

UDB10_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_A0: 0x4000640A

B1_UDB10_A0: 0x4000650A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.687 B[0..3]_UDB11_A0

UDB11_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_A0: 0x4000640B

B1_UDB11_A0: 0x4000650B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.688 B[0..3]_UDB12_A0

UDB12_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_A0: 0x4000640C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.689 B[0..3]_UDB13_A0

UDB13_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_A0: 0x4000640D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.690 B[0..3]_UDB14_A0

UDB14_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_A0: 0x4000640E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.691 B[0..3]_UDB15_A0

UDB15_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_A0: 0x4000640F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.692 B[0..3]_UDB00_A1

UDB00_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_A1: 0x40006410

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.693 B[0..3]_UDB01_A1

UDB01_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_A1: 0x40006411

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.694 B[0..3]_UDB02_A1

UDB02_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_A1: 0x40006412

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.695 B[0..3]_UDB03_A1

UDB03_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_A1: 0x40006413

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.696 B[0..3]_UDB04_A1

UDB04_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_A1: 0x40006414

B1_UDB04_A1: 0x40006514

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.697 B[0..3]_UDB05_A1

UDB05_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_A1: 0x40006415

B1_UDB05_A1: 0x40006515

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.698 B[0..3]_UDB06_A1

UDB06_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_A1: 0x40006416

B1_UDB06_A1: 0x40006516

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.699 B[0..3]_UDB07_A1

UDB07_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_A1: 0x40006417

B1_UDB07_A1: 0x40006517

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.700 B[0..3]_UDB08_A1

UDB08_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_A1: 0x40006418

B1_UDB08_A1: 0x40006518

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.701 B[0..3]_UDB09_A1

UDB09_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_A1: 0x40006419

B1_UDB09_A1: 0x40006519

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.702 B[0..3]_UDB10_A1

UDB10_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_A1: 0x4000641A

B1_UDB10_A1: 0x4000651A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.703 B[0..3]_UDB11_A1

UDB11_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_A1: 0x4000641B

B1_UDB11_A1: 0x4000651B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.704 B[0..3]_UDB12_A1

UDB12_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_A1: 0x4000641C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.705 B[0..3]_UDB13_A1

UDB13_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_A1: 0x4000641D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.706 B[0..3]_UDB14_A1

UDB14_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_A1: 0x4000641E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |



@0x40006400 + [0..3 * 0x100] + 0x1f

1.3.707 B[0..3]_UDB15_A1 UDB15_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_A1: 0x4000641F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | A1[7:0] | Generic field for 8 bit working registers |

1.3.708 B[0..3]_UDB00_D0

UDB00_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_D0: 0x40006420

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.709 B[0..3]_UDB01_D0

UDB01_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_D0: 0x40006421

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.710 B[0..3]_UDB02_D0

UDB02_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_D0: 0x40006422

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.711 B[0..3]_UDB03_D0

UDB03_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_D0: 0x40006423

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.712 B[0..3]_UDB04_D0

UDB04_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_D0: 0x40006424

B1_UDB04_D0: 0x40006524

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.713 B[0..3]_UDB05_D0

UDB05_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_D0: 0x40006425

B1_UDB05_D0: 0x40006525

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.714 B[0..3]_UDB06_D0

UDB06_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_D0: 0x40006426

B1_UDB06_D0: 0x40006526

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.715 B[0..3]_UDB07_D0

UDB07_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_D0: 0x40006427

B1_UDB07_D0: 0x40006527

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.716 B[0..3]_UDB08_D0

UDB08_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_D0: 0x40006428

B1_UDB08_D0: 0x40006528

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.717 B[0..3]_UDB09_D0

UDB09_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_D0: 0x40006429

B1_UDB09_D0: 0x40006529

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.718 B[0..3]_UDB10_D0

UDB10_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_D0: 0x4000642A

B1_UDB10_D0: 0x4000652A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.719 B[0..3]_UDB11_D0

UDB11_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_D0: 0x4000642B

B1_UDB11_D0: 0x4000652B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.720 B[0..3]_UDB12_D0

UDB12_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_D0: 0x4000642C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.721 B[0..3]_UDB13_D0

UDB13_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_D0: 0x4000642D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.722 B[0..3]_UDB14_D0

UDB14_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_D0: 0x4000642E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.723 B[0..3]_UDB15_D0

UDB15_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_D0: 0x4000642F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

Data 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.724 B[0..3]_UDB00_D1

UDB00_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_D1: 0x40006430

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.725 B[0..3]_UDB01_D1

UDB01_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_D1: 0x40006431

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.726 B[0..3]_UDB02_D1

UDB02_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_D1: 0x40006432

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.727 B[0..3]_UDB03_D1

UDB03_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_D1: 0x40006433

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.728 B[0..3]_UDB04_D1

UDB04_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_D1: 0x40006434

B1_UDB04_D1: 0x40006534

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.729 B[0..3]_UDB05_D1

UDB05_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_D1: 0x40006435

B1_UDB05_D1: 0x40006535

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.730 B[0..3]_UDB06_D1

UDB06_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_D1: 0x40006436

B1_UDB06_D1: 0x40006536

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.731 B[0..3]_UDB07_D1

UDB07_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_D1: 0x40006437

B1_UDB07_D1: 0x40006537

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.732 B[0..3]_UDB08_D1

UDB08_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_D1: 0x40006438

B1_UDB08_D1: 0x40006538

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.733 B[0..3]_UDB09_D1

UDB09_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_D1: 0x40006439

B1_UDB09_D1: 0x40006539

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.734 B[0..3]_UDB10_D1

UDB10_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_D1: 0x4000643A

B1_UDB10_D1: 0x4000653A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.735 B[0..3]_UDB11_D1

UDB11_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_D1: 0x4000643B

B1_UDB11_D1: 0x4000653B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.736 B[0..3]_UDB12_D1

UDB12_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_D1: 0x4000643C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.737 B[0..3]_UDB13_D1

UDB13_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_D1: 0x4000643D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.738 B[0..3]_UDB14_D1

UDB14_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_D1: 0x4000643E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.739 B[0..3]_UDB15_D1

UDB15_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_D1: 0x4000643F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | D1[7:0] | Generic field for 8 bit working registers |

1.3.740 B[0..3]_UDB00_F0

UDB00_F0

Reset: N/A

Register : Address

B0_UDB00_F0: 0x40006440

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.741 B[0..3]_UDB01_F0

UDB01_F0

Reset: N/A

Register : Address

B0_UDB01_F0: 0x40006441

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.742 B[0..3]_UDB02_F0

UDB02_F0

Reset: N/A

Register : Address

B0_UDB02_F0: 0x40006442

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.743 B[0..3]_UDB03_F0

UDB03_F0

Reset: N/A

Register : Address

B0_UDB03_F0: 0x40006443

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.744 B[0..3]_UDB04_F0

UDB04_F0

Reset: N/A

Register : Address

B0_UDB04_F0: 0x40006444

B1_UDB04_F0: 0x40006544

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.745 B[0..3]_UDB05_F0

UDB05_F0

Reset: N/A

Register : Address

B0_UDB05_F0: 0x40006445

B1_UDB05_F0: 0x40006545

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.746 B[0..3]_UDB06_F0

UDB06_F0

Reset: N/A

Register : Address

B0_UDB06_F0: 0x40006446

B1_UDB06_F0: 0x40006546

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.747 B[0..3]_UDB07_F0

UDB07_F0

Reset: N/A

Register : Address

B0_UDB07_F0: 0x40006447

B1_UDB07_F0: 0x40006547

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.748 B[0..3]_UDB08_F0

UDB08_F0

Reset: N/A

Register : Address

B0_UDB08_F0: 0x40006448

B1_UDB08_F0: 0x40006548

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.749 B[0..3]_UDB09_F0

UDB09_F0

Reset: N/A

Register : Address

B0_UDB09_F0: 0x40006449

B1_UDB09_F0: 0x40006549

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.750 B[0..3]_UDB10_F0

UDB10_F0

Reset: N/A

Register : Address

B0_UDB10_F0: 0x4000644A

B1_UDB10_F0: 0x4000654A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

@0x40006400 + [0..3 * 0x100] + 0x4b

1.3.751 B[0..3]_UDB11_F0

UDB11_F0

Reset: N/A

Register : Address

B0_UDB11_F0: 0x4000644B

B1_UDB11_F0: 0x4000654B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.752 B[0..3]_UDB12_F0

UDB12_F0

Reset: N/A

Register : Address

B0_UDB12_F0: 0x4000644C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.753 B[0..3]_UDB13_F0

UDB13_F0

Reset: N/A

Register : Address

B0_UDB13_F0: 0x4000644D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.754 B[0..3]_UDB14_F0

UDB14_F0

Reset: N/A

Register : Address

B0_UDB14_F0: 0x4000644E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.755 B[0..3]_UDB15_F0

UDB15_F0

Reset: N/A

Register : Address

B0_UDB15_F0: 0x4000644F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.756 B[0..3]_UDB00_F1

UDB00_F1

Reset: N/A

Register : Address

B0_UDB00_F1: 0x40006450

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.757 B[0..3]_UDB01_F1

UDB01_F1

Reset: N/A

Register : Address

B0_UDB01_F1: 0x40006451

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.758 B[0..3]_UDB02_F1

UDB02_F1

Reset: N/A

Register : Address

B0_UDB02_F1: 0x40006452

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.759 B[0..3]_UDB03_F1

UDB03_F1

Reset: N/A

Register : Address

B0_UDB03_F1: 0x40006453

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.760 B[0..3]_UDB04_F1

UDB04_F1

Reset: N/A

Register : Address

B0_UDB04_F1: 0x40006454

B1_UDB04_F1: 0x40006554

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

@0x40006400 + [0..3 * 0x100] + 0x55

1.3.761 B[0..3]_UDB05_F1

UDB05_F1

Reset: N/A

Register : Address

B0_UDB05_F1: 0x40006455

B1_UDB05_F1: 0x40006555

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.762 B[0..3]_UDB06_F1

UDB06_F1

Reset: N/A

Register : Address

B0_UDB06_F1: 0x40006456

B1_UDB06_F1: 0x40006556

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.763 B[0..3]_UDB07_F1

UDB07_F1

Reset: N/A

Register : Address

B0_UDB07_F1: 0x40006457

B1_UDB07_F1: 0x40006557

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.764 B[0..3]_UDB08_F1

UDB08_F1

Reset: N/A

Register : Address

B0_UDB08_F1: 0x40006458

B1_UDB08_F1: 0x40006558

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.765 B[0..3]_UDB09_F1

UDB09_F1

Reset: N/A

Register : Address

B0_UDB09_F1: 0x40006459

B1_UDB09_F1: 0x40006559

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.766 B[0..3]_UDB10_F1

UDB10_F1

Reset: N/A

Register : Address

B0_UDB10_F1: 0x4000645A

B1_UDB10_F1: 0x4000655A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.767 B[0..3]_UDB11_F1

UDB11_F1

Reset: N/A

Register : Address

B0_UDB11_F1: 0x4000645B

B1_UDB11_F1: 0x4000655B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.768 B[0..3]_UDB12_F1

UDB12_F1

Reset: N/A

Register : Address

B0_UDB12_F1: 0x4000645C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.769 B[0..3]_UDB13_F1

UDB13_F1

Reset: N/A

Register : Address

B0_UDB13_F1: 0x4000645D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.770 B[0..3]_UDB14_F1

UDB14_F1

Reset: N/A

Register : Address

B0_UDB14_F1: 0x4000645E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.771 B[0..3]_UDB15_F1

UDB15_F1

Reset: N/A

Register : Address

B0_UDB15_F1: 0x4000645F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|---------|---|
| 7:0 | F1[7:0] | Generic field for 8 bit working registers |

1.3.772 B[0..3]_UDB00_ST

UDB00_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_ST: 0x40006460

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.773 B[0..3]_UDB01_ST

UDB01_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_ST: 0x40006461

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.774 B[0..3]_UDB02_ST

UDB02_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_ST: 0x40006462

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.775 B[0..3]_UDB03_ST

UDB03_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_ST: 0x40006463

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.776 B[0..3]_UDB04_ST

UDB04_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_ST: 0x40006464

B1_UDB04_ST: 0x40006564

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.777 B[0..3]_UDB05_ST

UDB05_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_ST: 0x40006465

B1_UDB05_ST: 0x40006565

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.778 B[0..3]_UDB06_ST

UDB06_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_ST: 0x40006466

B1_UDB06_ST: 0x40006566

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.779 B[0..3]_UDB07_ST UDB07_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_ST: 0x40006467

B1_UDB07_ST: 0x40006567

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.780 B[0..3]_UDB08_ST

UDB08_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_ST: 0x40006468

B1_UDB08_ST: 0x40006568

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.781 B[0..3]_UDB09_ST UDB09_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_ST: 0x40006469

B1_UDB09_ST: 0x40006569

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.782 B[0..3]_UDB10_ST

UDB10_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_ST: 0x4000646A

B1_UDB10_ST: 0x4000656A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.783 B[0..3]_UDB11_ST UDB11_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_ST: 0x4000646B

B1_UDB11_ST: 0x4000656B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.784 B[0..3]_UDB12_ST

UDB12_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_ST: 0x4000646C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.785 B[0..3]_UDB13_ST UDB13_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_ST: 0x4000646D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.786 B[0..3]_UDB14_ST

UDB14_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_ST: 0x4000646E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.787 B[0..3]_UDB15_ST UDB15_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_ST: 0x4000646F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

Status Register

| Bits | Name | Description |
|------|---------|-----------------|
| 7:0 | ST[7:0] | Status register |

1.3.788 B[0..3]_UDB00_CTL

UDB00_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_CTL: 0x40006470

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.789 B[0..3]_UDB01_CTL

UDB01_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_CTL: 0x40006471

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.790 B[0..3]_UDB02_CTL

UDB02_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_CTL: 0x40006472

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.791 B[0..3]_UDB03_CTL

UDB03_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_CTL: 0x40006473

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.792 B[0..3]_UDB04_CTL

UDB04_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_CTL: 0x40006474

B1_UDB04_CTL: 0x40006574

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.793 B[0..3]_UDB05_CTL

UDB05_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_CTL: 0x40006475

B1_UDB05_CTL: 0x40006575

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.794 B[0..3]_UDB06_CTL

UDB06_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_CTL: 0x40006476

B1_UDB06_CTL: 0x40006576

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.795 B[0..3]_UDB07_CTL

UDB07_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_CTL: 0x40006477

B1_UDB07_CTL: 0x40006577

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.796 B[0..3]_UDB08_CTL

UDB08_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_CTL: 0x40006478

B1_UDB08_CTL: 0x40006578

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.797 B[0..3]_UDB09_CTL

UDB09_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_CTL: 0x40006479

B1_UDB09_CTL: 0x40006579

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.798 B[0..3]_UDB10_CTL

UDB10_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_CTL: 0x4000647A

B1_UDB10_CTL: 0x4000657A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.799 B[0..3]_UDB11_CTL

UDB11_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_CTL: 0x4000647B

B1_UDB11_CTL: 0x4000657B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.800 B[0..3]_UDB12_CTL

UDB12_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_CTL: 0x4000647C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.801 B[0..3]_UDB13_CTL

UDB13_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_CTL: 0x4000647D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.802 B[0..3]_UDB14_CTL

UDB14_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_CTL: 0x4000647E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.803 B[0..3]_UDB15_CTL

UDB15_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_CTL: 0x4000647F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

Control Register

| Bits | Name | Description |
|------|----------|------------------|
| 7:0 | CTL[7:0] | Control register |

1.3.804 B[0..3]_UDB00_MSK

UDB00_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_MSK: 0x40006480

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.805 B[0..3]_UDB01_MSK

UDB01_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_MSK: 0x40006481

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.806 B[0..3]_UDB02_MSK

UDB02_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_MSK: 0x40006482

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.807 B[0..3]_UDB03_MSK

UDB03_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_MSK: 0x40006483

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.808 B[0..3]_UDB04_MSK

UDB04_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_MSK: 0x40006484

B1_UDB04_MSK: 0x40006584

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.809 B[0..3]_UDB05_MSK

UDB05_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_MSK: 0x40006485

B1_UDB05_MSK: 0x40006585

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.810 B[0..3]_UDB06_MSK

UDB06_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_MSK: 0x40006486

B1_UDB06_MSK: 0x40006586

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.811 B[0..3]_UDB07_MSK

UDB07_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_MSK: 0x40006487

B1_UDB07_MSK: 0x40006587

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.812 B[0..3]_UDB08_MSK

UDB08_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_MSK: 0x40006488

B1_UDB08_MSK: 0x40006588

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.813 B[0..3]_UDB09_MSK

UDB09_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_MSK: 0x40006489

B1_UDB09_MSK: 0x40006589

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.814 B[0..3]_UDB10_MSK

UDB10_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_MSK: 0x4000648A

B1_UDB10_MSK: 0x4000658A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.815 B[0..3]_UDB11_MSK

UDB11_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_MSK: 0x4000648B

B1_UDB11_MSK: 0x4000658B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.816 B[0..3]_UDB12_MSK

UDB12_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_MSK: 0x4000648C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.817 B[0..3]_UDB13_MSK

UDB13_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_MSK: 0x4000648D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.818 B[0..3]_UDB14_MSK

UDB14_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_MSK: 0x4000648E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.819 B[0..3]_UDB15_MSK

UDB15_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_MSK: 0x4000648F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|----------|---|
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

1.3.820 B[0..3]_UDB00_ACTL

UDB00_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_ACTL: 0x40006490

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-544. |
| 4 | INT_EN | (no description) See Table 1-547. |
| 3 | FIFO1_LVL | FIFO level See Table 1-546. |
| 2 | FIFO0_LVL | FIFO level See Table 1-546. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-545. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-545. |

Table 1-544. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-545. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-546. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-547. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.820 B[0..3]_UDB00_ACTL (continued)

Table 1-547. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.821 B[0..3]_UDB01_ACTL

UDB01_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_ACTL: 0x40006491

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-548. |
| 4 | INT_EN | (no description) See Table 1-551. |
| 3 | FIFO1_LVL | FIFO level See Table 1-550. |
| 2 | FIFO0_LVL | FIFO level See Table 1-550. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-549. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-549. |

Table 1-548. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-549. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-550. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-551. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.821 B[0..3]_UDB01_ACTL (continued)

Table 1-551. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.822 B[0..3]_UDB02_ACTL

UDB02_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_ACTL: 0x40006492

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-552. |
| 4 | INT_EN | (no description) See Table 1-555. |
| 3 | FIFO1_LVL | FIFO level See Table 1-554. |
| 2 | FIFO0_LVL | FIFO level See Table 1-554. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-553. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-553. |

Table 1-552. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-553. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-554. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-555. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.822 B[0..3]_UDB02_ACTL (continued)

Table 1-555. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.823 B[0..3]_UDB03_ACTL

UDB03_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_ACTL: 0x40006493

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-556. |
| 4 | INT_EN | (no description) See Table 1-559. |
| 3 | FIFO1_LVL | FIFO level See Table 1-558. |
| 2 | FIFO0_LVL | FIFO level See Table 1-558. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-557. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-557. |

Table 1-556. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-557. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-558. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-559. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.823 B[0..3]_UDB03_ACTL (continued)

Table 1-559. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.824 B[0..3]_UDB04_ACTL

UDB04_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_ACTL: 0x40006494

B1_UDB04_ACTL: 0x40006594

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-560. |
| 4 | INT_EN | (no description) See Table 1-563. |
| 3 | FIFO1_LVL | FIFO level See Table 1-562. |
| 2 | FIFO0_LVL | FIFO level See Table 1-562. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-561. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-561. |

Table 1-560. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-561. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-562. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-563. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.824 B[0..3]_UDB04_ACTL (continued)

Table 1-563. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.825 B[0..3]_UDB05_ACTL

UDB05_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_ACTL: 0x40006495

B1_UDB05_ACTL: 0x40006595

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-564. |
| 4 | INT_EN | (no description) See Table 1-567. |
| 3 | FIFO1_LVL | FIFO level See Table 1-566. |
| 2 | FIFO0_LVL | FIFO level See Table 1-566. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-565. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-565. |

Table 1-564. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-565. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-566. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-567. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.825 B[0..3]_UDB05_ACTL (continued)

Table 1-567. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.826 B[0..3]_UDB06_ACTL

UDB06_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_ACTL: 0x40006496

B1_UDB06_ACTL: 0x40006596

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-568. |
| 4 | INT_EN | (no description) See Table 1-571. |
| 3 | FIFO1_LVL | FIFO level See Table 1-570. |
| 2 | FIFO0_LVL | FIFO level See Table 1-570. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-569. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-569. |

Table 1-568. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-569. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-570. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-571. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.826 B[0..3]_UDB06_ACTL (continued)

Table 1-571. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.827 B[0..3]_UDB07_ACTL

UDB07_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_ACTL: 0x40006497

B1_UDB07_ACTL: 0x40006597

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-572. |
| 4 | INT_EN | (no description) See Table 1-575. |
| 3 | FIFO1_LVL | FIFO level See Table 1-574. |
| 2 | FIFO0_LVL | FIFO level See Table 1-574. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-573. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-573. |

Table 1-572. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-573. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-574. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-575. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.827 B[0..3]_UDB07_ACTL (continued)

Table 1-575. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.828 B[0..3]_UDB08_ACTL

UDB08_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_ACTL: 0x40006498

B1_UDB08_ACTL: 0x40006598

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-576. |
| 4 | INT_EN | (no description) See Table 1-579. |
| 3 | FIFO1_LVL | FIFO level See Table 1-578. |
| 2 | FIFO0_LVL | FIFO level See Table 1-578. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-577. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-577. |

Table 1-576. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-577. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-578. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-579. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.828 B[0..3]_UDB08_ACTL (continued)

Table 1-579. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.829 B[0..3]_UDB09_ACTL

UDB09_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_ACTL: 0x40006499

B1_UDB09_ACTL: 0x40006599

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-580. |
| 4 | INT_EN | (no description) See Table 1-583. |
| 3 | FIFO1_LVL | FIFO level See Table 1-582. |
| 2 | FIFO0_LVL | FIFO level See Table 1-582. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-581. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-581. |

Table 1-580. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-581. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-582. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-583. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.829 B[0..3]_UDB09_ACTL (continued)

Table 1-583. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.830 B[0..3]_UDB10_ACTL

UDB10_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_ACTL: 0x4000649A

B1_UDB10_ACTL: 0x4000659A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-584. |
| 4 | INT_EN | (no description) See Table 1-587. |
| 3 | FIFO1_LVL | FIFO level See Table 1-586. |
| 2 | FIFO0_LVL | FIFO level See Table 1-586. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-585. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-585. |

Table 1-584. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-585. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-586. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-587. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.830 B[0..3]_UDB10_ACTL (continued)

Table 1-587. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.831 B[0..3]_UDB11_ACTL

UDB11_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_ACTL: 0x4000649B

B1_UDB11_ACTL: 0x4000659B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-588. |
| 4 | INT_EN | (no description) See Table 1-591. |
| 3 | FIFO1_LVL | FIFO level See Table 1-590. |
| 2 | FIFO0_LVL | FIFO level See Table 1-590. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-589. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-589. |

Table 1-588. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-589. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-590. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-591. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.831 B[0..3]_UDB11_ACTL (continued)

Table 1-591. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.832 B[0..3]_UDB12_ACTL

UDB12_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_ACTL: 0x4000649C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|---------------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-592. |
| 4 | INT_EN | (no description) See Table 1-595. |
| 3 | FIFO1_LVL | FIFO level See Table 1-594. |
| 2 | FIFO0_LVL | FIFO level See Table 1-594. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-593. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-593. |

Table 1-592. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-593. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-594. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-595. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.832 B[0..3]_UDB12_ACTL (continued)

Table 1-595. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.833 B[0..3]_UDB13_ACTL

UDB13_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_ACTL: 0x4000649D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-596. |
| 4 | INT_EN | (no description) See Table 1-599. |
| 3 | FIFO1_LVL | FIFO level See Table 1-598. |
| 2 | FIFO0_LVL | FIFO level See Table 1-598. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-597. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-597. |

Table 1-596. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-597. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-598. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-599. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.833 B[0..3]_UDB13_ACTL (continued)

Table 1-599. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.834 B[0..3]_UDB14_ACTL

UDB14_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_ACTL: 0x4000649E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-600. |
| 4 | INT_EN | (no description) See Table 1-603. |
| 3 | FIFO1_LVL | FIFO level See Table 1-602. |
| 2 | FIFO0_LVL | FIFO level See Table 1-602. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-601. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-601. |

Table 1-600. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-601. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-602. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-603. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.834 B[0..3]_UDB14_ACTL (continued)

Table 1-603. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.835 B[0..3]_UDB15_ACTL

UDB15_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_ACTL: 0x4000649F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 5 | CNT_START | FIFO0 clear See Table 1-604. |
| 4 | INT_EN | (no description) See Table 1-607. |
| 3 | FIFO1_LVL | FIFO level See Table 1-606. |
| 2 | FIFO0_LVL | FIFO level See Table 1-606. |
| 1 | FIFO1_CLR | FIFO clear See Table 1-605. |
| 0 | FIFO0_CLR | FIFO clear See Table 1-605. |

Table 1-604. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-605. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-606. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-607. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.835 B[0..3]_UDB15_ACTL (continued)

Table 1-607. Bit field encoding: E_INT_EN

| | | |
|------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.836 B[0..3]_UDB00_MC

UDB00_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_MC: 0x400064A0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.837 B[0..3]_UDB01_MC

UDB01_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_MC: 0x400064A1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.838 B[0..3]_UDB02_MC

UDB02_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_MC: 0x400064A2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.839 B[0..3]_UDB03_MC

UDB03_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_MC: 0x400064A3

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.840 B[0..3]_UDB04_MC

UDB04_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_MC: 0x400064A4

B1_UDB04_MC: 0x400065A4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.841 B[0..3]_UDB05_MC

UDB05_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_MC: 0x400064A5

B1_UDB05_MC: 0x400065A5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.842 B[0..3]_UDB06_MC

UDB06_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_MC: 0x400064A6

B1_UDB06_MC: 0x400065A6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.843 B[0..3]_UDB07_MC

UDB07_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_MC: 0x400064A7

B1_UDB07_MC: 0x400065A7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.844 B[0..3]_UDB08_MC

UDB08_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_MC: 0x400064A8

B1_UDB08_MC: 0x400065A8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.845 B[0..3]_UDB09_MC

UDB09_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_MC: 0x400064A9

B1_UDB09_MC: 0x400065A9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.846 B[0..3]_UDB10_MC

UDB10_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_MC: 0x400064AA

B1_UDB10_MC: 0x400065AA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.847 B[0..3]_UDB11_MC

UDB11_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_MC: 0x400064AB

B1_UDB11_MC: 0x400065AB

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.848 B[0..3]_UDB12_MC

UDB12_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_MC: 0x400064AC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.849 B[0..3]_UDB13_MC

UDB13_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_MC: 0x400064AD

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.850 B[0..3]_UDB14_MC

UDB14_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_MC: 0x400064AE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.851 B[0..3]_UDB15_MC

UDB15_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_MC: 0x400064AF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC | | | | PLD0_MC | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|--------------|----------------|
| 7:4 | PLD1_MC[3:0] | Read Macrocell |
| 3:0 | PLD0_MC[3:0] | Read Macrocell |

1.3.852 B[0..3]_UDB00_01_A0

UDB00_01_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_A0: 0x40006800

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.853 B[0..3]_UDB01_02_A0

UDB01_02_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_A0: 0x40006802

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.854 B[0..3]_UDB02_03_A0

UDB02_03_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_A0: 0x40006804

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.855 B[0..3]_UDB03_04_A0

UDB03_04_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_A0: 0x40006806

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.856 B[0..3]_UDB04_05_A0

UDB04_05_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_A0: 0x40006808

B1_UDB04_05_A0: 0x40006A08

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.857 B[0..3]_UDB05_06_A0

UDB05_06_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_A0: 0x4000680A

B1_UDB05_06_A0: 0x40006A0A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.858 B[0..3]_UDB06_07_A0

UDB06_07_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_A0: 0x4000680C

B1_UDB06_07_A0: 0x40006A0C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.859 B[0..3]_UDB07_08_A0

UDB07_08_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_A0: 0x4000680E

B1_UDB07_08_A0: 0x40006A0E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.860 B[0..3]_UDB08_09_A0

UDB08_09_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_A0: 0x40006810

B1_UDB08_09_A0: 0x40006A10

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.861 B[0..3]_UDB09_10_A0

UDB09_10_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_A0: 0x40006812

B1_UDB09_10_A0: 0x40006A12

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.862 B[0..3]_UDB10_11_A0

UDB10_11_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_A0: 0x40006814

B1_UDB10_11_A0: 0x40006A14

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.863 B[0..3]_UDB11_12_A0

UDB11_12_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_A0: 0x40006816

B1_UDB11_12_A0: 0x40006A16

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.864 B[0..3]_UDB12_13_A0

UDB12_13_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_A0: 0x40006818

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.865 B[0..3]_UDB13_14_A0

UDB13_14_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_A0: 0x4000681A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.866 B[0..3]_UDB14_15_A0

UDB14_15_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_A0: 0x4000681C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0_MS | | | | | | | |

Accumulator 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0_LS[7:0] | Generic field for 8 bit working registers |

1.3.867 B[0..3]_UDB00_01_A1

UDB00_01_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_A1: 0x40006820

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.868 B[0..3]_UDB01_02_A1

UDB01_02_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_A1: 0x40006822

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.869 B[0..3]_UDB02_03_A1

UDB02_03_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_A1: 0x40006824

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.870 B[0..3]_UDB03_04_A1

UDB03_04_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_A1: 0x40006826

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.871 B[0..3]_UDB04_05_A1

UDB04_05_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_A1: 0x40006828

B1_UDB04_05_A1: 0x40006A28

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.872 B[0..3]_UDB05_06_A1

UDB05_06_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_A1: 0x4000682A

B1_UDB05_06_A1: 0x40006A2A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.873 B[0..3]_UDB06_07_A1

UDB06_07_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_A1: 0x4000682C

B1_UDB06_07_A1: 0x40006A2C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.874 B[0..3]_UDB07_08_A1

UDB07_08_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_A1: 0x4000682E

B1_UDB07_08_A1: 0x40006A2E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.875 B[0..3]_UDB08_09_A1

UDB08_09_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_A1: 0x40006830

B1_UDB08_09_A1: 0x40006A30

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.876 B[0..3]_UDB09_10_A1

UDB09_10_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_A1: 0x40006832

B1_UDB09_10_A1: 0x40006A32

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.877 B[0..3]_UDB10_11_A1

UDB10_11_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_A1: 0x40006834

B1_UDB10_11_A1: 0x40006A34

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.878 B[0..3]_UDB11_12_A1

UDB11_12_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_A1: 0x40006836

B1_UDB11_12_A1: 0x40006A36

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.879 B[0..3]_UDB12_13_A1

UDB12_13_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_A1: 0x40006838

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.880 B[0..3]_UDB13_14_A1

UDB13_14_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_A1: 0x4000683A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.881 B[0..3]_UDB14_15_A1

UDB14_15_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_A1: 0x4000683C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1_MS | | | | | | | |

Accumulator 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | A1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | A1_LS[7:0] | Generic field for 8 bit working registers |

1.3.882 B[0..3]_UDB00_01_D0

UDB00_01_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_01_D0: 0x40006840

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.883 B[0..3]_UDB01_02_D0

UDB01_02_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_02_D0: 0x40006842

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.884 B[0..3]_UDB02_03_D0

UDB02_03_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_03_D0: 0x40006844

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.885 B[0..3]_UDB03_04_D0

UDB03_04_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_04_D0: 0x40006846

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.886 B[0..3]_UDB04_05_D0

UDB04_05_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_05_D0: 0x40006848

B1_UDB04_05_D0: 0x40006A48

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.887 B[0..3]_UDB05_06_D0

UDB05_06_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_06_D0: 0x4000684A

B1_UDB05_06_D0: 0x40006A4A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.888 B[0..3]_UDB06_07_D0

UDB06_07_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_07_D0: 0x4000684C

B1_UDB06_07_D0: 0x40006A4C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.889 B[0..3]_UDB07_08_D0

UDB07_08_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_08_D0: 0x4000684E

B1_UDB07_08_D0: 0x40006A4E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.890 B[0..3]_UDB08_09_D0

UDB08_09_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_09_D0: 0x40006850

B1_UDB08_09_D0: 0x40006A50

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.891 B[0..3]_UDB09_10_D0

UDB09_10_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_10_D0: 0x40006852

B1_UDB09_10_D0: 0x40006A52

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.892 B[0..3]_UDB10_11_D0

UDB10_11_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_11_D0: 0x40006854

B1_UDB10_11_D0: 0x40006A54

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.893 B[0..3]_UDB11_12_D0

UDB11_12_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_12_D0: 0x40006856

B1_UDB11_12_D0: 0x40006A56

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.894 B[0..3]_UDB12_13_D0

UDB12_13_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_13_D0: 0x40006858

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.895 B[0..3]_UDB13_14_D0

UDB13_14_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_14_D0: 0x4000685A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.896 B[0..3]_UDB14_15_D0

UDB14_15_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_15_D0: 0x4000685C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0_MS | | | | | | | |

Data 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0_LS[7:0] | Generic field for 8 bit working registers |

1.3.897 B[0..3]_UDB00_01_D1

UDB00_01_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_01_D1: 0x40006860

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.898 B[0..3]_UDB01_02_D1

UDB01_02_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_02_D1: 0x40006862

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.899 B[0..3]_UDB02_03_D1

UDB02_03_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_03_D1: 0x40006864

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.900 B[0..3]_UDB03_04_D1

UDB03_04_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_04_D1: 0x40006866

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.901 B[0..3]_UDB04_05_D1

UDB04_05_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_05_D1: 0x40006868

B1_UDB04_05_D1: 0x40006A68

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.902 B[0..3]_UDB05_06_D1

UDB05_06_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_06_D1: 0x4000686A

B1_UDB05_06_D1: 0x40006A6A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.903 B[0..3]_UDB06_07_D1

UDB06_07_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_07_D1: 0x4000686C

B1_UDB06_07_D1: 0x40006A6C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.904 B[0..3]_UDB07_08_D1

UDB07_08_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_08_D1: 0x4000686E

B1_UDB07_08_D1: 0x40006A6E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.905 B[0..3]_UDB08_09_D1

UDB08_09_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_09_D1: 0x40006870

B1_UDB08_09_D1: 0x40006A70

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.906 B[0..3]_UDB09_10_D1

UDB09_10_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_10_D1: 0x40006872

B1_UDB09_10_D1: 0x40006A72

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.907 B[0..3]_UDB10_11_D1

UDB10_11_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_11_D1: 0x40006874

B1_UDB10_11_D1: 0x40006A74

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.908 B[0..3]_UDB11_12_D1

UDB11_12_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_12_D1: 0x40006876

B1_UDB11_12_D1: 0x40006A76

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.909 B[0..3]_UDB12_13_D1

UDB12_13_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_13_D1: 0x40006878

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.910 B[0..3]_UDB13_14_D1

UDB13_14_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_14_D1: 0x4000687A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.911 B[0..3]_UDB14_15_D1

UDB14_15_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_15_D1: 0x4000687C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1_MS | | | | | | | |

Data 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | D1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | D1_LS[7:0] | Generic field for 8 bit working registers |

1.3.912 B[0..3]_UDB00_01_F0

UDB00_01_F0

Reset: N/A

Register : Address

B0_UDB00_01_F0: 0x40006880

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.913 B[0..3]_UDB01_02_F0

UDB01_02_F0

Reset: N/A

Register : Address

B0_UDB01_02_F0: 0x40006882

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.914 B[0..3]_UDB02_03_F0

UDB02_03_F0

Reset: N/A

Register : Address

B0_UDB02_03_F0: 0x40006884

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.915 B[0..3]_UDB03_04_F0

UDB03_04_F0

Reset: N/A

Register : Address

B0_UDB03_04_F0: 0x40006886

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.916 B[0..3]_UDB04_05_F0

UDB04_05_F0

Reset: N/A

Register : Address

B0_UDB04_05_F0: 0x40006888

B1_UDB04_05_F0: 0x40006A88

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.917 B[0..3]_UDB05_06_F0

UDB05_06_F0

Reset: N/A

Register : Address

B0_UDB05_06_F0: 0x4000688A

B1_UDB05_06_F0: 0x40006A8A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.918 B[0..3]_UDB06_07_F0

UDB06_07_F0

Reset: N/A

Register : Address

B0_UDB06_07_F0: 0x4000688C

B1_UDB06_07_F0: 0x40006A8C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.919 B[0..3]_UDB07_08_F0

UDB07_08_F0

Reset: N/A

Register : Address

B0_UDB07_08_F0: 0x4000688E

B1_UDB07_08_F0: 0x40006A8E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.920 B[0..3]_UDB08_09_F0

UDB08_09_F0

Reset: N/A

Register : Address

B0_UDB08_09_F0: 0x40006890

B1_UDB08_09_F0: 0x40006A90

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.921 B[0..3]_UDB09_10_F0

UDB09_10_F0

Reset: N/A

Register : Address

B0_UDB09_10_F0: 0x40006892

B1_UDB09_10_F0: 0x40006A92

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.922 B[0..3]_UDB10_11_F0

UDB10_11_F0

Reset: N/A

Register : Address

B0_UDB10_11_F0: 0x40006894

B1_UDB10_11_F0: 0x40006A94

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.923 B[0..3]_UDB11_12_F0

UDB11_12_F0

Reset: N/A

Register : Address

B0_UDB11_12_F0: 0x40006896

B1_UDB11_12_F0: 0x40006A96

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.924 B[0..3]_UDB12_13_F0

UDB12_13_F0

Reset: N/A

Register : Address

B0_UDB12_13_F0: 0x40006898

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.925 B[0..3]_UDB13_14_F0

UDB13_14_F0

Reset: N/A

Register : Address

B0_UDB13_14_F0: 0x4000689A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.926 B[0..3]_UDB14_15_F0

UDB14_15_F0

Reset: N/A

Register : Address

B0_UDB14_15_F0: 0x4000689C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0_MS | | | | | | | |

FIFO 0

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F0_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0_LS[7:0] | Generic field for 8 bit working registers |

1.3.927 B[0..3]_UDB00_01_F1

UDB00_01_F1

Reset: N/A

Register : Address

B0_UDB00_01_F1: 0x400068A0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.928 B[0..3]_UDB01_02_F1

UDB01_02_F1

Reset: N/A

Register : Address

B0_UDB01_02_F1: 0x400068A2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.929 B[0..3]_UDB02_03_F1

UDB02_03_F1

Reset: N/A

Register : Address

B0_UDB02_03_F1: 0x400068A4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.930 B[0..3]_UDB03_04_F1

UDB03_04_F1

Reset: N/A

Register : Address

B0_UDB03_04_F1: 0x400068A6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.931 B[0..3]_UDB04_05_F1

UDB04_05_F1

Reset: N/A

Register : Address

B0_UDB04_05_F1: 0x400068A8

B1_UDB04_05_F1: 0x40006AA8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.932 B[0..3]_UDB05_06_F1

UDB05_06_F1

Reset: N/A

Register : Address

B0_UDB05_06_F1: 0x400068AA

B1_UDB05_06_F1: 0x40006AAA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.933 B[0..3]_UDB06_07_F1

UDB06_07_F1

Reset: N/A

Register : Address

B0_UDB06_07_F1: 0x400068AC

B1_UDB06_07_F1: 0x40006AAC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.934 B[0..3]_UDB07_08_F1

UDB07_08_F1

Reset: N/A

Register : Address

B0_UDB07_08_F1: 0x400068AE

B1_UDB07_08_F1: 0x40006AAE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.935 B[0..3]_UDB08_09_F1

UDB08_09_F1

Reset: N/A

Register : Address

B0_UDB08_09_F1: 0x400068B0

B1_UDB08_09_F1: 0x40006AB0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.936 B[0..3]_UDB09_10_F1

UDB09_10_F1

Reset: N/A

Register : Address

B0_UDB09_10_F1: 0x400068B2

B1_UDB09_10_F1: 0x40006AB2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.937 B[0..3]_UDB10_11_F1

UDB10_11_F1

Reset: N/A

Register : Address

B0_UDB10_11_F1: 0x400068B4

B1_UDB10_11_F1: 0x40006AB4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.938 B[0..3]_UDB11_12_F1

UDB11_12_F1

Reset: N/A

Register : Address

B0_UDB11_12_F1: 0x400068B6

B1_UDB11_12_F1: 0x40006AB6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.939 B[0..3]_UDB12_13_F1

UDB12_13_F1

Reset: N/A

Register : Address

B0_UDB12_13_F1: 0x400068B8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.940 B[0..3]_UDB13_14_F1

UDB13_14_F1

Reset: N/A

Register : Address

B0_UDB13_14_F1: 0x400068BA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.941 B[0..3]_UDB14_15_F1

UDB14_15_F1

Reset: N/A

Register : Address

B0_UDB14_15_F1: 0x400068BC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1_MS | | | | | | | |

FIFO 1

| Bits | Name | Description |
|------|------------|---|
| 15:8 | F1_MS[7:0] | Generic field for 8 bit working registers |
| 7:0 | F1_LS[7:0] | Generic field for 8 bit working registers |

1.3.942 B[0..3]_UDB00_01_ST

UDB00_01_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_ST: 0x400068C0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.943 B[0..3]_UDB01_02_ST

UDB01_02_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_ST: 0x400068C2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.944 B[0..3]_UDB02_03_ST

UDB02_03_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_ST: 0x400068C4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.945 B[0..3]_UDB03_04_ST

UDB03_04_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_ST: 0x400068C6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.946 B[0..3]_UDB04_05_ST

UDB04_05_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_ST: 0x400068C8

B1_UDB04_05_ST: 0x40006AC8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.947 B[0..3]_UDB05_06_ST

UDB05_06_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_ST: 0x400068CA

B1_UDB05_06_ST: 0x40006ACA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.948 B[0..3]_UDB06_07_ST

UDB06_07_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_ST: 0x400068CC

B1_UDB06_07_ST: 0x40006ACC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.949 B[0..3]_UDB07_08_ST

UDB07_08_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_ST: 0x400068CE

B1_UDB07_08_ST: 0x40006ACE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.950 B[0..3]_UDB08_09_ST

UDB08_09_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_ST: 0x400068D0

B1_UDB08_09_ST: 0x40006AD0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.951 B[0..3]_UDB09_10_ST

UDB09_10_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_ST: 0x400068D2

B1_UDB09_10_ST: 0x40006AD2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.952 B[0..3]_UDB10_11_ST

UDB10_11_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_ST: 0x400068D4

B1_UDB10_11_ST: 0x40006AD4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.953 B[0..3]_UDB11_12_ST

UDB11_12_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_ST: 0x400068D6

B1_UDB11_12_ST: 0x40006AD6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.954 B[0..3]_UDB12_13_ST

UDB12_13_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_ST: 0x400068D8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.955 B[0..3]_UDB13_14_ST

UDB13_14_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_ST: 0x400068DA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.956 B[0..3]_UDB14_15_ST

UDB14_15_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_ST: 0x400068DC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST_MS | | | | | | | |

Status Register

| Bits | Name | Description |
|------|------------|-----------------|
| 15:8 | ST_MS[7:0] | Status register |
| 7:0 | ST_LS[7:0] | Status register |

1.3.957 B[0..3]_UDB00_01_CTL

UDB00_01_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_CTL: 0x400068E0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.958 B[0..3]_UDB01_02_CTL

UDB01_02_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_CTL: 0x400068E2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.959 B[0..3]_UDB02_03_CTL

UDB02_03_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_CTL: 0x400068E4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.960 B[0..3]_UDB03_04_CTL

UDB03_04_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_CTL: 0x400068E6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.961 B[0..3]_UDB04_05_CTL

UDB04_05_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_CTL: 0x400068E8

B1_UDB04_05_CTL: 0x40006AE8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.962 B[0..3]_UDB05_06_CTL

UDB05_06_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_CTL: 0x400068EA

B1_UDB05_06_CTL: 0x40006AEA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.963 B[0..3]_UDB06_07_CTL

UDB06_07_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_CTL: 0x400068EC

B1_UDB06_07_CTL: 0x40006AEC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.964 B[0..3]_UDB07_08_CTL

UDB07_08_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_CTL: 0x400068EE

B1_UDB07_08_CTL: 0x40006AEE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.965 B[0..3]_UDB08_09_CTL

UDB08_09_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_CTL: 0x400068F0

B1_UDB08_09_CTL: 0x40006AF0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.966 B[0..3]_UDB09_10_CTL

UDB09_10_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_CTL: 0x400068F2

B1_UDB09_10_CTL: 0x40006AF2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.967 B[0..3]_UDB10_11_CTL

UDB10_11_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_CTL: 0x400068F4

B1_UDB10_11_CTL: 0x40006AF4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.968 B[0..3]_UDB11_12_CTL

UDB11_12_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_CTL: 0x400068F6

B1_UDB11_12_CTL: 0x40006AF6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.969 B[0..3]_UDB12_13_CTL

UDB12_13_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_CTL: 0x400068F8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.970 B[0..3]_UDB13_14_CTL

UDB13_14_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_CTL: 0x400068FA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.971 B[0..3]_UDB14_15_CTL

UDB14_15_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_CTL: 0x400068FC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_LS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MS | | | | | | | |

Control Register

| Bits | Name | Description |
|------|-------------|------------------|
| 15:8 | CTL_MS[7:0] | Control register |
| 7:0 | CTL_LS[7:0] | Control register |

1.3.972 B[0..3]_UDB00_01_MSK

UDB00_01_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_01_MSK: 0x40006900

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.973 B[0..3]_UDB01_02_MSK

UDB01_02_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_02_MSK: 0x40006902

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.974 B[0..3]_UDB02_03_MSK

UDB02_03_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_03_MSK: 0x40006904

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.975 B[0..3]_UDB03_04_MSK

UDB03_04_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_04_MSK: 0x40006906

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.976 B[0..3]_UDB04_05_MSK

UDB04_05_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_05_MSK: 0x40006908

B1_UDB04_05_MSK: 0x40006B08

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.977 B[0..3]_UDB05_06_MSK

UDB05_06_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_06_MSK: 0x4000690A

B1_UDB05_06_MSK: 0x40006B0A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.978 B[0..3]_UDB06_07_MSK

UDB06_07_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_07_MSK: 0x4000690C

B1_UDB06_07_MSK: 0x40006B0C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.979 B[0..3]_UDB07_08_MSK

UDB07_08_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_08_MSK: 0x4000690E

B1_UDB07_08_MSK: 0x40006B0E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.980 B[0..3]_UDB08_09_MSK

UDB08_09_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_09_MSK: 0x40006910

B1_UDB08_09_MSK: 0x40006B10

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.981 B[0..3]_UDB09_10_MSK

UDB09_10_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_10_MSK: 0x40006912

B1_UDB09_10_MSK: 0x40006B12

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.982 B[0..3]_UDB10_11_MSK

UDB10_11_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_11_MSK: 0x40006914

B1_UDB10_11_MSK: 0x40006B14

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.983 B[0..3]_UDB11_12_MSK

UDB11_12_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_12_MSK: 0x40006916

B1_UDB11_12_MSK: 0x40006B16

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.984 B[0..3]_UDB12_13_MSK

UDB12_13_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_13_MSK: 0x40006918

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.985 B[0..3]_UDB13_14_MSK

UDB13_14_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_14_MSK: 0x4000691A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.986 B[0..3]_UDB14_15_MSK

UDB14_15_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_15_MSK: 0x4000691C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_LS | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------------|----|----|----|----|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK_MS | | | | | | |

Interrupt Mask

| Bits | Name | Description |
|------|-------------|---|
| 14:8 | MSK_MS[6:0] | Generic field for 7 bit working registers |
| 6:0 | MSK_LS[6:0] | Generic field for 7 bit working registers |

1.3.987 B[0..3]_UDB00_01_ACTL

UDB00_01_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_01_ACTL: 0x40006920

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-608. |
| 12 | INT_EN_MS | (no description) See Table 1-611. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-610. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-610. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-609. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-609. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-608. |
| 4 | INT_EN_LS | (no description) See Table 1-611. |
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-610. |

1.3.987 B[0..3]_UDB00_01_ACTL (continued)

| | | |
|---|--------------|--|
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-610. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-609. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-609. |

Table 1-608. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-609. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-610. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-611. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.988 B[0..3]_UDB01_02_ACTL

UDB01_02_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_02_ACTL: 0x40006922

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-612. |
| 12 | INT_EN_MS | (no description) See Table 1-615. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-614. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-614. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-613. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-613. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-612. |
| 4 | INT_EN_LS | (no description) See Table 1-615. |
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-614. |

1.3.988 B[0..3]_UDB01_02_ACTL (continued)

| | | |
|---|--------------|--|
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-614. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-613. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-613. |

Table 1-612. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-613. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-614. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-615. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.989 B[0..3]_UDB02_03_ACTL

UDB02_03_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_03_ACTL: 0x40006924

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-616. |
| 12 | INT_EN_MS | (no description) See Table 1-619. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-618. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-618. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-617. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-617. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-616. |
| 4 | INT_EN_LS | (no description) See Table 1-619. |
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-618. |

1.3.989 B[0..3]_UDB02_03_ACTL (continued)

| | | |
|---|--------------|--|
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-618. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-617. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-617. |

Table 1-616. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-617. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-618. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-619. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.990 B[0..3]_UDB03_04_ACTL

UDB03_04_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_04_ACTL: 0x40006926

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-620. |
| 12 | INT_EN_MS | (no description) See Table 1-623. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-622. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-622. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-621. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-621. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-620. |
| 4 | INT_EN_LS | (no description) See Table 1-623. |
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-622. |

1.3.990 B[0..3]_UDB03_04_ACTL (continued)

| | | |
|---|--------------|--|
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-622. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-621. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-621. |

Table 1-620. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-621. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-622. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-623. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.991 B[0..3]_UDB04_05_ACTL

UDB04_05_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_05_ACTL: 0x40006928

B1_UDB04_05_ACTL: 0x40006B28

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-624. |
| 12 | INT_EN_MS | (no description) See Table 1-627. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-626. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-626. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-625. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-625. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-624. |
| 4 | INT_EN_LS | (no description) See Table 1-627. |

1.3.991 B[0..3]_UDB04_05_ACTL (continued)

| | | |
|---|--------------|--|
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-626. |
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-626. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-625. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-625. |

Table 1-624. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-625. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-626. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-627. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.992 B[0..3]_UDB05_06_ACTL

UDB05_06_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_06_ACTL: 0x4000692A

B1_UDB05_06_ACTL: 0x40006B2A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-628. |
| 12 | INT_EN_MS | (no description) See Table 1-631. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-630. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-630. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-629. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-629. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-628. |
| 4 | INT_EN_LS | (no description) See Table 1-631. |

1.3.992 B[0..3]_UDB05_06_ACTL (continued)

| | | |
|---|--------------|--|
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-630. |
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-630. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-629. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-629. |

Table 1-628. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-629. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-630. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-631. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.993 B[0..3]_UDB06_07_ACTL

UDB06_07_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_07_ACTL: 0x4000692C

B1_UDB06_07_ACTL: 0x40006B2C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-632. |
| 12 | INT_EN_MS | (no description) See Table 1-635. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-634. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-634. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-633. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-633. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-632. |
| 4 | INT_EN_LS | (no description) See Table 1-635. |

1.3.993 B[0..3]_UDB06_07_ACTL (continued)

| | | |
|---|--------------|--|
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-634. |
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-634. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-633. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-633. |

Table 1-632. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-633. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-634. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-635. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.994 B[0..3]_UDB07_08_ACTL

UDB07_08_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_08_ACTL: 0x4000692E

B1_UDB07_08_ACTL: 0x40006B2E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-636. |
| 12 | INT_EN_MS | (no description) See Table 1-639. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-638. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-638. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-637. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-637. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-636. |
| 4 | INT_EN_LS | (no description) See Table 1-639. |

1.3.994 B[0..3]_UDB07_08_ACTL (continued)

| | | |
|---|--------------|--|
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-638. |
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-638. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-637. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-637. |

Table 1-636. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-637. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-638. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-639. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.995 B[0..3]_UDB08_09_ACTL

UDB08_09_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_09_ACTL: 0x40006930

B1_UDB08_09_ACTL: 0x40006B30

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-640. |
| 12 | INT_EN_MS | (no description) See Table 1-643. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-642. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-642. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-641. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-641. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-640. |
| 4 | INT_EN_LS | (no description) See Table 1-643. |

1.3.995 B[0..3]_UDB08_09_ACTL (continued)

| | | |
|---|--------------|--|
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-642. |
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-642. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-641. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-641. |

Table 1-640. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-641. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-642. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-643. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.996 B[0..3]_UDB09_10_ACTL

UDB09_10_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_10_ACTL: 0x40006932

B1_UDB09_10_ACTL: 0x40006B32

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-644. |
| 12 | INT_EN_MS | (no description) See Table 1-647. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-646. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-646. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-645. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-645. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-644. |
| 4 | INT_EN_LS | (no description) See Table 1-647. |

1.3.996 B[0..3]_UDB09_10_ACTL (continued)

| | | |
|---|--------------|--|
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-646. |
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-646. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-645. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-645. |

Table 1-644. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-645. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-646. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-647. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.997 B[0..3]_UDB10_11_ACTL

UDB10_11_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_11_ACTL: 0x40006934

B1_UDB10_11_ACTL: 0x40006B34

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-648. |
| 12 | INT_EN_MS | (no description) See Table 1-651. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-650. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-650. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-649. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-649. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-648. |
| 4 | INT_EN_LS | (no description) See Table 1-651. |

1.3.997 B[0..3]_UDB10_11_ACTL (continued)

| | | |
|---|--------------|--|
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-650. |
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-650. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-649. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-649. |

Table 1-648. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-649. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-650. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-651. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.998 B[0..3]_UDB11_12_ACTL

UDB11_12_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_12_ACTL: 0x40006936

B1_UDB11_12_ACTL: 0x40006B36

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-652. |
| 12 | INT_EN_MS | (no description) See Table 1-655. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-654. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-654. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-653. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-653. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-652. |
| 4 | INT_EN_LS | (no description) See Table 1-655. |

1.3.998 B[0..3]_UDB11_12_ACTL (continued)

| | | |
|---|--------------|--|
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-654. |
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-654. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-653. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-653. |

Table 1-652. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-653. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-654. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-655. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.999 B[0..3]_UDB12_13_ACTL

UDB12_13_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_13_ACTL: 0x40006938

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-656. |
| 12 | INT_EN_MS | (no description) See Table 1-659. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-658. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-658. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-657. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-657. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-656. |
| 4 | INT_EN_LS | (no description) See Table 1-659. |
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-658. |

1.3.999 B[0..3]_UDB12_13_ACTL (continued)

| | | |
|---|--------------|--|
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-658. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-657. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-657. |

Table 1-656. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-657. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-658. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-659. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1000 B[0..3]_UDB13_14_ACTL

UDB13_14_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_14_ACTL: 0x4000693A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-660. |
| 12 | INT_EN_MS | (no description) See Table 1-663. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-662. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-662. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-661. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-661. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-660. |
| 4 | INT_EN_LS | (no description) See Table 1-663. |
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-662. |

1.3.1000 B[0..3]_UDB13_14_ACTL (continued)

| | | |
|---|--------------|--|
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-662. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-661. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-661. |

Table 1-660. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-661. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-662. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-663. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1001 B[0..3]_UDB14_15_ACTL

UDB14_15_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_15_ACTL: 0x4000693C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------------|-----------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_LS | INT_EN_LS | FIFO1_LVL _LS | FIFO0_LVL _LS | FIFO1_CLR _LS | FIFO0_CLR _LS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------------|---------------|------------------|------------------|------------------|------------------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_STAR T_MS | INT_EN_M S | FIFO1_LVL _MS | FIFO0_LVL _MS | FIFO1_CLR _MS | FIFO0_CLR _MS |

Auxiliary Control

| Bits | Name | Description |
|------|--------------|--|
| 13 | CNT_START_MS | FIFO0 clear See Table 1-664. |
| 12 | INT_EN_MS | (no description) See Table 1-667. |
| 11 | FIFO1_LVL_MS | FIFO level See Table 1-666. |
| 10 | FIFO0_LVL_MS | FIFO level See Table 1-666. |
| 9 | FIFO1_CLR_MS | FIFO clear See Table 1-665. |
| 8 | FIFO0_CLR_MS | FIFO clear See Table 1-665. |
| 5 | CNT_START_LS | FIFO0 clear See Table 1-664. |
| 4 | INT_EN_LS | (no description) See Table 1-667. |
| 3 | FIFO1_LVL_LS | FIFO level See Table 1-666. |

1.3.1001 B[0..3]_UDB14_15_ACTL (continued)

| | | |
|---|--------------|--|
| 2 | FIFO0_LVL_LS | FIFO level See Table 1-666. |
| 1 | FIFO1_CLR_LS | FIFO clear See Table 1-665. |
| 0 | FIFO0_CLR_LS | FIFO clear See Table 1-665. |

Table 1-664. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-665. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-666. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-667. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1002 B[0..3]_UDB00_01_MC

UDB00_01_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_MC: 0x40006940

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1003 B[0..3]_UDB01_02_MC

UDB01_02_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_MC: 0x40006942

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1004 B[0..3]_UDB02_03_MC

UDB02_03_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_MC: 0x40006944

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1005 B[0..3]_UDB03_04_MC

UDB03_04_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_MC: 0x40006946

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1006 B[0..3]_UDB04_05_MC

UDB04_05_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_MC: 0x40006948

B1_UDB04_05_MC: 0x40006B48

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1007 B[0..3]_UDB05_06_MC

UDB05_06_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_MC: 0x4000694A

B1_UDB05_06_MC: 0x40006B4A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1008 B[0..3]_UDB06_07_MC

UDB06_07_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_MC: 0x4000694C

B1_UDB06_07_MC: 0x40006B4C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1009 B[0..3]_UDB07_08_MC

UDB07_08_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_MC: 0x4000694E

B1_UDB07_08_MC: 0x40006B4E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1010 B[0..3]_UDB08_09_MC

UDB08_09_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_MC: 0x40006950

B1_UDB08_09_MC: 0x40006B50

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1011 B[0..3]_UDB09_10_MC

UDB09_10_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_MC: 0x40006952

B1_UDB09_10_MC: 0x40006B52

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1012 B[0..3]_UDB10_11_MC

UDB10_11_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_MC: 0x40006954

B1_UDB10_11_MC: 0x40006B54

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1013 B[0..3]_UDB11_12_MC

UDB11_12_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_MC: 0x40006956

B1_UDB11_12_MC: 0x40006B56

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1014 B[0..3]_UDB12_13_MC

UDB12_13_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_MC: 0x40006958

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1015 B[0..3]_UDB13_14_MC

UDB13_14_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_MC: 0x4000695A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1016 B[0..3]_UDB14_15_MC

UDB14_15_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_MC: 0x4000695C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|------------|----|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_MS | | | | PLD0_MC_MS | | | |

PLD Macrocell reading

| Bits | Name | Description |
|-------|-----------------|----------------|
| 15:12 | PLD1_MC_MS[3:0] | Read Macrocell |
| 11:8 | PLD0_MC_MS[3:0] | Read Macrocell |
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1017 B[0..3]_UDB00_A0_A1

UDB00_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_A0_A1: 0x40006800

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1018 B[0..3]_UDB01_A0_A1

UDB01_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_A0_A1: 0x40006802

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1019 B[0..3]_UDB02_A0_A1

UDB02_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_A0_A1: 0x40006804

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1020 B[0..3]_UDB03_A0_A1

UDB03_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_A0_A1: 0x40006806

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1021 B[0..3]_UDB04_A0_A1

UDB04_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_A0_A1: 0x40006808

B1_UDB04_A0_A1: 0x40006A08

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1022 B[0..3]_UDB05_A0_A1

UDB05_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_A0_A1: 0x4000680A

B1_UDB05_A0_A1: 0x40006A0A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1023 B[0..3]_UDB06_A0_A1

UDB06_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_A0_A1: 0x4000680C

B1_UDB06_A0_A1: 0x40006A0C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1024 B[0..3]_UDB07_A0_A1

UDB07_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_A0_A1: 0x4000680E

B1_UDB07_A0_A1: 0x40006A0E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1025 B[0..3]_UDB08_A0_A1

UDB08_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_A0_A1: 0x40006810

B1_UDB08_A0_A1: 0x40006A10

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1026 B[0..3]_UDB09_A0_A1

UDB09_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_A0_A1: 0x40006812

B1_UDB09_A0_A1: 0x40006A12

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1027 B[0..3]_UDB10_A0_A1

UDB10_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_A0_A1: 0x40006814

B1_UDB10_A0_A1: 0x40006A14

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1028 B[0..3]_UDB11_A0_A1

UDB11_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_A0_A1: 0x40006816

B1_UDB11_A0_A1: 0x40006A16

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1029 B[0..3]_UDB12_A0_A1

UDB12_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_A0_A1: 0x40006818

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1030 B[0..3]_UDB13_A0_A1

UDB13_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_A0_A1: 0x4000681A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1031 B[0..3]_UDB14_A0_A1

UDB14_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_A0_A1: 0x4000681C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1032 B[0..3]_UDB15_A0_A1

UDB15_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_A0_A1: 0x4000681E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | A1 | | | | | | | |

Accumulator 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | A1[7:0] | Generic field for 8 bit working registers |
| 7:0 | A0[7:0] | Generic field for 8 bit working registers |

1.3.1033 B[0..3]_UDB00_D0_D1

UDB00_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_D0_D1: 0x40006840

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1034 B[0..3]_UDB01_D0_D1

UDB01_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_D0_D1: 0x40006842

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1035 B[0..3]_UDB02_D0_D1

UDB02_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_D0_D1: 0x40006844

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1036 B[0..3]_UDB03_D0_D1

UDB03_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_D0_D1: 0x40006846

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1037 B[0..3]_UDB04_D0_D1

UDB04_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_D0_D1: 0x40006848

B1_UDB04_D0_D1: 0x40006A48

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1038 B[0..3]_UDB05_D0_D1

UDB05_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_D0_D1: 0x4000684A

B1_UDB05_D0_D1: 0x40006A4A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1039 B[0..3]_UDB06_D0_D1

UDB06_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_D0_D1: 0x4000684C

B1_UDB06_D0_D1: 0x40006A4C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1040 B[0..3]_UDB07_D0_D1

UDB07_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_D0_D1: 0x4000684E

B1_UDB07_D0_D1: 0x40006A4E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1041 B[0..3]_UDB08_D0_D1

UDB08_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_D0_D1: 0x40006850

B1_UDB08_D0_D1: 0x40006A50

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1042 B[0..3]_UDB09_D0_D1

UDB09_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_D0_D1: 0x40006852

B1_UDB09_D0_D1: 0x40006A52

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1043 B[0..3]_UDB10_D0_D1

UDB10_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_D0_D1: 0x40006854

B1_UDB10_D0_D1: 0x40006A54

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1044 B[0..3]_UDB11_D0_D1

UDB11_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_D0_D1: 0x40006856

B1_UDB11_D0_D1: 0x40006A56

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1045 B[0..3]_UDB12_D0_D1

UDB12_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_D0_D1: 0x40006858

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1046 B[0..3]_UDB13_D0_D1

UDB13_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_D0_D1: 0x4000685A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1047 B[0..3]_UDB14_D0_D1

UDB14_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_D0_D1: 0x4000685C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1048 B[0..3]_UDB15_D0_D1

UDB15_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_D0_D1: 0x4000685E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | D1 | | | | | | | |

Data 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | D1[7:0] | Generic field for 8 bit working registers |
| 7:0 | D0[7:0] | Generic field for 8 bit working registers |

1.3.1049 B[0..3]_UDB00_F0_F1

UDB00_F0_F1

Reset: N/A

Register : Address

B0_UDB00_F0_F1: 0x40006880

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1050 B[0..3]_UDB01_F0_F1

UDB01_F0_F1

Reset: N/A

Register : Address

B0_UDB01_F0_F1: 0x40006882

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1051 B[0..3]_UDB02_F0_F1

UDB02_F0_F1

Reset: N/A

Register : Address

B0_UDB02_F0_F1: 0x40006884

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1052 B[0..3]_UDB03_F0_F1

UDB03_F0_F1

Reset: N/A

Register : Address

B0_UDB03_F0_F1: 0x40006886

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1053 B[0..3]_UDB04_F0_F1

UDB04_F0_F1

Reset: N/A

Register : Address

B0_UDB04_F0_F1: 0x40006888

B1_UDB04_F0_F1: 0x40006A88

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1054 B[0..3]_UDB05_F0_F1

UDB05_F0_F1

Reset: N/A

Register : Address

B0_UDB05_F0_F1: 0x4000688A

B1_UDB05_F0_F1: 0x40006A8A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1055 B[0..3]_UDB06_F0_F1

UDB06_F0_F1

Reset: N/A

Register : Address

B0_UDB06_F0_F1: 0x4000688C

B1_UDB06_F0_F1: 0x40006A8C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1056 B[0..3]_UDB07_F0_F1

UDB07_F0_F1

Reset: N/A

Register : Address

B0_UDB07_F0_F1: 0x4000688E

B1_UDB07_F0_F1: 0x40006A8E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1057 B[0..3]_UDB08_F0_F1

UDB08_F0_F1

Reset: N/A

Register : Address

B0_UDB08_F0_F1: 0x40006890

B1_UDB08_F0_F1: 0x40006A90

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1058 B[0..3]_UDB09_F0_F1

UDB09_F0_F1

Reset: N/A

Register : Address

B0_UDB09_F0_F1: 0x40006892

B1_UDB09_F0_F1: 0x40006A92

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1059 B[0..3]_UDB10_F0_F1

UDB10_F0_F1

Reset: N/A

Register : Address

B0_UDB10_F0_F1: 0x40006894

B1_UDB10_F0_F1: 0x40006A94

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1060 B[0..3]_UDB11_F0_F1

UDB11_F0_F1

Reset: N/A

Register : Address

B0_UDB11_F0_F1: 0x40006896

B1_UDB11_F0_F1: 0x40006A96

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1061 B[0..3]_UDB12_F0_F1

UDB12_F0_F1

Reset: N/A

Register : Address

B0_UDB12_F0_F1: 0x40006898

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1062 B[0..3]_UDB13_F0_F1

UDB13_F0_F1

Reset: N/A

Register : Address

B0_UDB13_F0_F1: 0x4000689A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1063 B[0..3]_UDB14_F0_F1

UDB14_F0_F1

Reset: N/A

Register : Address

B0_UDB14_F0_F1: 0x4000689C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1064 B[0..3]_UDB15_F0_F1

UDB15_F0_F1

Reset: N/A

Register : Address

B0_UDB15_F0_F1: 0x4000689E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | F1 | | | | | | | |

FIFO 0 and 1

| Bits | Name | Description |
|------|---------|---|
| 15:8 | F1[7:0] | Generic field for 8 bit working registers |
| 7:0 | F0[7:0] | Generic field for 8 bit working registers |

1.3.1065 B[0..3]_UDB00_ST_CTL

UDB00_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_ST_CTL: 0x400068C0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1066 B[0..3]_UDB01_ST_CTL

UDB01_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_ST_CTL: 0x400068C2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1067 B[0..3]_UDB02_ST_CTL

UDB02_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_ST_CTL: 0x400068C4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1068 B[0..3]_UDB03_ST_CTL

UDB03_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_ST_CTL: 0x400068C6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1069 B[0..3]_UDB04_ST_CTL

UDB04_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_ST_CTL: 0x400068C8

B1_UDB04_ST_CTL: 0x40006AC8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1070 B[0..3]_UDB05_ST_CTL

UDB05_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_ST_CTL: 0x400068CA

B1_UDB05_ST_CTL: 0x40006ACA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1071 B[0..3]_UDB06_ST_CTL

UDB06_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_ST_CTL: 0x400068CC

B1_UDB06_ST_CTL: 0x40006ACC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1072 B[0..3]_UDB07_ST_CTL

UDB07_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_ST_CTL: 0x400068CE

B1_UDB07_ST_CTL: 0x40006ACE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1073 B[0..3]_UDB08_ST_CTL

UDB08_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_ST_CTL: 0x400068D0

B1_UDB08_ST_CTL: 0x40006AD0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1074 B[0..3]_UDB09_ST_CTL

UDB09_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_ST_CTL: 0x400068D2

B1_UDB09_ST_CTL: 0x40006AD2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1075 B[0..3]_UDB10_ST_CTL

UDB10_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_ST_CTL: 0x400068D4

B1_UDB10_ST_CTL: 0x40006AD4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1076 B[0..3]_UDB11_ST_CTL

UDB11_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_ST_CTL: 0x400068D6

B1_UDB11_ST_CTL: 0x40006AD6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1077 B[0..3]_UDB12_ST_CTL

UDB12_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_ST_CTL: 0x400068D8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1078 B[0..3]_UDB13_ST_CTL

UDB13_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_ST_CTL: 0x400068DA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1079 B[0..3]_UDB14_ST_CTL

UDB14_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_ST_CTL: 0x400068DC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1080 B[0..3]_UDB15_ST_CTL

UDB15_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_ST_CTL: 0x400068DE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | ST | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL | | | | | | | |

My Status and Control Register

| Bits | Name | Description |
|------|----------|---------------------|
| 15:8 | CTL[7:0] | My Control register |
| 7:0 | ST[7:0] | My Status register |

1.3.1081 B[0..3]_UDB00_MSK_ACTL

UDB00_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_MSK_ACTL: 0x40006900

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | MSK | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-668. |
| 12 | INT_EN | (no description) See Table 1-671. |
| 11 | FIFO1_LVL | FIFO level See Table 1-670. |
| 10 | FIFO0_LVL | FIFO level See Table 1-670. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-669. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-669. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-668. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-669. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

1.3.1081 B[0..3]_UDB00_MSK_ACTL (continued)

Table 1-670. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-671. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1082 B[0..3]_UDB01_MSK_ACTL

UDB01_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_MSK_ACTL: 0x40006902

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | MSK | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-672. |
| 12 | INT_EN | (no description) See Table 1-675. |
| 11 | FIFO1_LVL | FIFO level See Table 1-674. |
| 10 | FIFO0_LVL | FIFO level See Table 1-674. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-673. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-673. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-672. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-673. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

1.3.1082 B[0..3]_UDB01_MSK_ACTL (continued)

Table 1-674. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-675. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1083 B[0..3]_UDB02_MSK_ACTL

UDB02_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_MSK_ACTL: 0x40006904

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | MSK | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-676. |
| 12 | INT_EN | (no description) See Table 1-679. |
| 11 | FIFO1_LVL | FIFO level See Table 1-678. |
| 10 | FIFO0_LVL | FIFO level See Table 1-678. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-677. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-677. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-676. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-677. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

@0x40006800 + [0..3 * 0x200] + 0x104

1.3.1083 B[0..3]_UDB02_MSK_ACTL (continued)

Table 1-678. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-679. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1084 B[0..3]_UDB03_MSK_ACTL

UDB03_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_MSK_ACTL: 0x40006906

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | MSK | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-680. |
| 12 | INT_EN | (no description) See Table 1-683. |
| 11 | FIFO1_LVL | FIFO level See Table 1-682. |
| 10 | FIFO0_LVL | FIFO level See Table 1-682. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-681. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-681. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-680. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-681. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

1.3.1084 B[0..3]_UDB03_MSK_ACTL (continued)

Table 1-682. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-683. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1085 B[0..3]_UDB04_MSK_ACTL

UDB04_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_MSK_ACTL: 0x40006908

B1_UDB04_MSK_ACTL: 0x40006B08

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-684. |
| 12 | INT_EN | (no description) See Table 1-687. |
| 11 | FIFO1_LVL | FIFO level See Table 1-686. |
| 10 | FIFO0_LVL | FIFO level See Table 1-686. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-685. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-685. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-684. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-685. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1085 B[0..3]_UDB04_MSK_ACTL (continued)

Table 1-685. Bit field encoding: E_FIFO_CLR

| | | |
|------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-686. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-687. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1086 B[0..3]_UDB05_MSK_ACTL

UDB05_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_MSK_ACTL: 0x4000690A

B1_UDB05_MSK_ACTL: 0x40006B0A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-688. |
| 12 | INT_EN | (no description) See Table 1-691. |
| 11 | FIFO1_LVL | FIFO level See Table 1-690. |
| 10 | FIFO0_LVL | FIFO level See Table 1-690. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-689. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-689. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-688. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-689. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1086 B[0..3]_UDB05_MSK_ACTL (continued)

Table 1-689. Bit field encoding: E_FIFO_CLR

| | | |
|------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-690. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-691. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1087 B[0..3]_UDB06_MSK_ACTL

UDB06_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_MSK_ACTL: 0x4000690C

B1_UDB06_MSK_ACTL: 0x40006B0C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-692. |
| 12 | INT_EN | (no description) See Table 1-695. |
| 11 | FIFO1_LVL | FIFO level See Table 1-694. |
| 10 | FIFO0_LVL | FIFO level See Table 1-694. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-693. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-693. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-692. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-693. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1087 B[0..3]_UDB06_MSK_ACTL (continued)

Table 1-693. Bit field encoding: E_FIFO_CLR

| | | |
|------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-694. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-695. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1088 B[0..3]_UDB07_MSK_ACTL

UDB07_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_MSK_ACTL: 0x4000690E

B1_UDB07_MSK_ACTL: 0x40006B0E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-696. |
| 12 | INT_EN | (no description) See Table 1-699. |
| 11 | FIFO1_LVL | FIFO level See Table 1-698. |
| 10 | FIFO0_LVL | FIFO level See Table 1-698. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-697. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-697. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-696. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-697. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1088 B[0..3]_UDB07_MSK_ACTL (continued)

Table 1-697. Bit field encoding: E_FIFO_CLR

| | | |
|------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-698. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-699. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1089 B[0..3]_UDB08_MSK_ACTL

UDB08_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_MSK_ACTL: 0x40006910

B1_UDB08_MSK_ACTL: 0x40006B10

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-700. |
| 12 | INT_EN | (no description) See Table 1-703. |
| 11 | FIFO1_LVL | FIFO level See Table 1-702. |
| 10 | FIFO0_LVL | FIFO level See Table 1-702. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-701. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-701. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-700. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-701. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1089 B[0..3]_UDB08_MSK_ACTL (continued)

Table 1-701. Bit field encoding: E_FIFO_CLR

| | | |
|------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-702. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-703. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1090 B[0..3]_UDB09_MSK_ACTL

UDB09_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_MSK_ACTL: 0x40006912

B1_UDB09_MSK_ACTL: 0x40006B12

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-704. |
| 12 | INT_EN | (no description) See Table 1-707. |
| 11 | FIFO1_LVL | FIFO level See Table 1-706. |
| 10 | FIFO0_LVL | FIFO level See Table 1-706. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-705. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-705. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-704. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-705. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1090 B[0..3]_UDB09_MSK_ACTL (continued)

Table 1-705. Bit field encoding: E_FIFO_CLR

| | | |
|------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-706. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-707. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1091 B[0..3]_UDB10_MSK_ACTL

UDB10_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_MSK_ACTL: 0x40006914

B1_UDB10_MSK_ACTL: 0x40006B14

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-708. |
| 12 | INT_EN | (no description) See Table 1-711. |
| 11 | FIFO1_LVL | FIFO level See Table 1-710. |
| 10 | FIFO0_LVL | FIFO level See Table 1-710. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-709. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-709. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-708. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-709. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

@0x40006800 + [0..3 * 0x200] + 0x114

1.3.1091 B[0..3]_UDB10_MSK_ACTL (continued)

Table 1-709. Bit field encoding: E_FIFO_CLR

| | | |
|------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-710. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-711. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1092 B[0..3]_UDB11_MSK_ACTL

UDB11_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_MSK_ACTL: 0x40006916

B1_UDB11_MSK_ACTL: 0x40006B16

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | MSK | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-712. |
| 12 | INT_EN | (no description) See Table 1-715. |
| 11 | FIFO1_LVL | FIFO level See Table 1-714. |
| 10 | FIFO0_LVL | FIFO level See Table 1-714. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-713. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-713. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-712. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-713. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1092 B[0..3]_UDB11_MSK_ACTL (continued)

Table 1-713. Bit field encoding: E_FIFO_CLR

| | | |
|------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

Table 1-714. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-715. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1093 B[0..3]_UDB12_MSK_ACTL

UDB12_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_MSK_ACTL: 0x40006918

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | MSK | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-716. |
| 12 | INT_EN | (no description) See Table 1-719. |
| 11 | FIFO1_LVL | FIFO level See Table 1-718. |
| 10 | FIFO0_LVL | FIFO level See Table 1-718. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-717. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-717. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-716. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-717. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

1.3.1093 B[0..3]_UDB12_MSK_ACTL (continued)

Table 1-718. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-719. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1094 B[0..3]_UDB13_MSK_ACTL

UDB13_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_MSK_ACTL: 0x4000691A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | MSK | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-720. |
| 12 | INT_EN | (no description) See Table 1-723. |
| 11 | FIFO1_LVL | FIFO level See Table 1-722. |
| 10 | FIFO0_LVL | FIFO level See Table 1-722. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-721. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-721. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-720. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-721. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

@0x40006800 + [0..3 * 0x200] + 0x11a

1.3.1094 B[0..3]_UDB13_MSK_ACTL (continued)

Table 1-722. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-723. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1095 B[0..3]_UDB14_MSK_ACTL

UDB14_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_MSK_ACTL: 0x4000691C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | MSK | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-724. |
| 12 | INT_EN | (no description) See Table 1-727. |
| 11 | FIFO1_LVL | FIFO level See Table 1-726. |
| 10 | FIFO0_LVL | FIFO level See Table 1-726. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-725. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-725. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-724. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-725. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

1.3.1095 B[0..3]_UDB14_MSK_ACTL (continued)

Table 1-726. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-727. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1096 B[0..3]_UDB15_MSK_ACTL

UDB15_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_MSK_ACTL: 0x4000691E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | MSK | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|-----------|--------|-----------|-----------|-----------|-----------|
| SW Access:Reset | NA:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | | CNT_START | INT_EN | FIFO1_LVL | FIFO0_LVL | FIFO1_CLR | FIFO0_CLR |

Interrupt Mask and Auxiliary Control

| Bits | Name | Description |
|------|-----------|--|
| 13 | CNT_START | FIFO0 clear See Table 1-728. |
| 12 | INT_EN | (no description) See Table 1-731. |
| 11 | FIFO1_LVL | FIFO level See Table 1-730. |
| 10 | FIFO0_LVL | FIFO level See Table 1-730. |
| 9 | FIFO1_CLR | FIFO clear See Table 1-729. |
| 8 | FIFO0_CLR | FIFO clear See Table 1-729. |
| 6:0 | MSK[6:0] | Generic field for 7 bit working registers |

Table 1-728. Bit field encoding: E_CNT_START

| Value | Name | Description |
|-------|--------------|-----------------|
| 1'b0 | E_CNT_START0 | Disable counter |
| 1'b1 | E_CNT_START1 | Enable counter |

Table 1-729. Bit field encoding: E_FIFO_CLR

| Value | Name | Description |
|-------|--------------|-----------------------|
| 1'b0 | E_FIFO_CLR_0 | Normal FIFO operation |
| 1'b1 | E_FIFO_CLR_1 | Clear FIFO state |

1.3.1096 B[0..3]_UDB15_MSK_ACTL (continued)

Table 1-730. Bit field encoding: E_FIFO_LVL

| Value | Name | Description |
|-------|--------------|--|
| 1'b0 | E_FIFO_LVL_0 | FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty |
| 1'b1 | E_FIFO_LVL_1 | FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full |

Table 1-731. Bit field encoding: E_INT_EN

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | E_INT_EN0 | Interrupt disabled |
| 1'b1 | E_INT_EN1 | Interrupt enabled |

1.3.1097 B[0..3]_UDB00_MC_00

UDB00_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_MC_00: 0x40006940

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1098 B[0..3]_UDB01_MC_00

UDB01_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_MC_00: 0x40006942

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1099 B[0..3]_UDB02_MC_00

UDB02_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_MC_00: 0x40006944

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1100 B[0..3]_UDB03_MC_00

UDB03_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_MC_00: 0x40006946

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1101 B[0..3]_UDB04_MC_00

UDB04_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_MC_00: 0x40006948

B1_UDB04_MC_00: 0x40006B48

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1102 B[0..3]_UDB05_MC_00

UDB05_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_MC_00: 0x4000694A

B1_UDB05_MC_00: 0x40006B4A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1103 B[0..3]_UDB06_MC_00

UDB06_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_MC_00: 0x4000694C

B1_UDB06_MC_00: 0x40006B4C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1104 B[0..3]_UDB07_MC_00

UDB07_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_MC_00: 0x4000694E

B1_UDB07_MC_00: 0x40006B4E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1105 B[0..3]_UDB08_MC_00

UDB08_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_MC_00: 0x40006950

B1_UDB08_MC_00: 0x40006B50

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1106 B[0..3]_UDB09_MC_00

UDB09_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_MC_00: 0x40006952

B1_UDB09_MC_00: 0x40006B52

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1107 B[0..3]_UDB10_MC_00

UDB10_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_MC_00: 0x40006954

B1_UDB10_MC_00: 0x40006B54

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1108 B[0..3]_UDB11_MC_00

UDB11_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_MC_00: 0x40006956

B1_UDB11_MC_00: 0x40006B56

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1109 B[0..3]_UDB12_MC_00

UDB12_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_MC_00: 0x40006958

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1110 B[0..3]_UDB13_MC_00

UDB13_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_MC_00: 0x4000695A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1111 B[0..3]_UDB14_MC_00

UDB14_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_MC_00: 0x4000695C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1112 B[0..3]_UDB15_MC_00

UDB15_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_MC_00: 0x4000695E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|------------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PLD1_MC_LS | | | | PLD0_MC_LS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PLD Macrocell reading

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:4 | PLD1_MC_LS[3:0] | Read Macrocell |
| 3:0 | PLD0_MC_LS[3:0] | Read Macrocell |

1.3.1113 PHUB_CFG

PHUB Configuration

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PHUB_CFG: 0x40007000

| | | | | | | | | |
|-----------------|--------------|-------------|-----------|-----------|-----------|-------------|-----------|------------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:1111111 | | | | | | | R/W:0 |
| HW Access | R | | | | | | | R |
| Name | spk_cpu_pri | | | | | | | cpu_clkdif |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:UUUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:0 | R/W:0000000 | | | | | | |
| HW Access | R | R | | | | | | |
| Name | simple_pri | pri_int_en | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:UUU | | | R:1 | R/W:1 | R/W:111 | | |
| HW Access | NA | | | R/W | R | R | | |
| Name | | | | dmac_idle | dmac_en | bus_timeout | | |

This is the general configuration register for the PHUB

| Bits | Name | Description |
|-------|------------------|---|
| 28 | dmac_idle | Indicates whether the DMAC is currently IDLE or not |
| 27 | dmac_en | Global DMAC enable |
| 26:24 | bus_timeout[2:0] | Specifies the number of wait states (!HREADY responses by an accessed peripheral) PHUB will allow before timing out the AHB transaction. On a bus timeout PHUB will act as if it received a positive HREADY from the peripheral then move onto the next natural transaction as it would normally. The BUS_TIMEOUT bit of the ERR register will be set upon detecting the timeout. See Table 1-732. |
| 23 | simple_pri | 0: Grant allocation fairness algorithm enabled 1: Grant allocation fairness algorithm disabled; simple priority utilized |
| 22:16 | pri_int_en[6:0] | 0: Priority can not interrupt lower priority channels 1: Priority can interrupt lower priority channels Bits 22:16 correspond to priorities 6:0. Priority 7 is the lowest priority and thus can not interrupt yet lower priorities and therefore there is no bit for it. |

1.3.1113 PHUB_CFG (continued)

| | | |
|-----|------------------|--|
| 7:1 | spk_cpu_pri[6:0] | 0: DMA priority spoke 1: CPU priority spoke Bits 15:1 correspond to spokes 15:1 respectively. SPK0 is not accessible by the CPU and thus no bit exists for it. The number of valid SPKxx_CPU_PRI bits is determined by the cfg_num_of_spk[4:0] input to PHUB; non-configured bits are hardwired to 0. |
| 0 | cpu_clkdif | 0: CPU_CLOCK_EN assumed tied to 1; Performance Mode 1: CPU_CLOCK_EN assumed to modulate; Mixed Frequency Mode |

Table 1-732. Bit field encoding: BUS_TIMEOUT_ENUM

| Value | Name | Description |
|--------|-----------|-------------------------------|
| 3'b000 | Timeout_0 | Disable bus timeout detection |
| 3'b001 | Timeout_1 | 8 wait states |
| 3'b010 | Timeout_2 | 16 wait states |
| 3'b011 | Timeout_3 | 32 wait states |
| 3'b100 | Timeout_4 | 64 wait states |
| 3'b101 | Timeout_5 | 128 wait states |
| 3'b110 | Timeout_6 | 256 wait states |
| 3'b111 | Timeout_7 | 511 wait states (default) |

1.3.1114 PHUB_ERR

PHUB Error Detection

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

PHUB_ERR: 0x40007004

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------------|-----------|-------------|------|
| SW Access:Reset | NA:UUUU | | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | NA:U |
| HW Access | NA | | | | R/W | R/W | R/W | NA |
| Name | | | | | periph_err | unpop_acc | bus_timeout | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

PHUB detects the following errors: 1. Bus Timeout 2. Unpopulated address access 3. Peripheral AHB ERROR response If the error was detected as a result of a CPU access then PHUB will send an AHB ERROR response to the CPU. If the error was detected as a result of either a CPU or DMA access then PHUB will set the corresponding bit in the following ERR register.

| Bits | Name | Description |
|------|-------------|---|
| 3 | periph_err | Set to 1 when a peripheral responds to a bus transaction with an AHB ERROR response. Cleared by writing a 1. |
| 2 | unpop_acc | Set to 1 when an access is attempted to an address that does not decode to any spoke HSEL. Cleared by writing a 1. |
| 1 | bus_timeout | Set to 1 when a bus timeout occurs. Cleared by writing a 1. Timeout values are determined by the BUS_TIMEOUT field in the PHUBCFG register. |

1.3.1115 PHUB_ERR_ADR

PHUB Error Address

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

PHUB_ERR_ADR: 0x40007008

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | err_adr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | err_adr | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | err_adr | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | err_adr | | | | | | | |

Contains the address that caused an error to trigger

| Bits | Name | Description |
|------|---------------|--|
| 31:0 | err_adr[31:0] | Contains the value of the address that caused the error (limited to the BUS_TIMEOUT, UNPOP_ACC and PERIPH_ERR errors). If there are a succession of errors that occur before the CPU is able to clear the ERR register to all zeros, ERR_ADR will latch the address of the first error only. |

1.3.1116 PHUB_CH[0..23]_BASIC_CFG

Channel Basic Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PHUB_CH0_BASIC_CFG: 0x40007010

PHUB_CH1_BASIC_CFG: 0x40007020

PHUB_CH2_BASIC_CFG: 0x40007030

PHUB_CH3_BASIC_CFG: 0x40007040

PHUB_CH4_BASIC_CFG: 0x40007050

PHUB_CH5_BASIC_CFG: 0x40007060

PHUB_CH6_BASIC_CFG: 0x40007070

PHUB_CH7_BASIC_CFG: 0x40007080

PHUB_CH8_BASIC_CFG: 0x40007090

PHUB_CH9_BASIC_CFG: 0x400070A0

PHUB_CH10_BASIC_CFG: 0x400070B0

PHUB_CH11_BASIC_CFG: 0x400070C0

PHUB_CH12_BASIC_CFG: 0x400070D0

PHUB_CH13_BASIC_CFG: 0x400070E0

PHUB_CH14_BASIC_CFG: 0x400070F0

PHUB_CH15_BASIC_CFG: 0x40007100

PHUB_CH16_BASIC_CFG: 0x40007110

PHUB_CH17_BASIC_CFG: 0x40007120

PHUB_CH18_BASIC_CFG: 0x40007130

PHUB_CH19_BASIC_CFG: 0x40007140

PHUB_CH20_BASIC_CFG: 0x40007150

PHUB_CH21_BASIC_CFG: 0x40007160

PHUB_CH22_BASIC_CFG: 0x40007170

PHUB_CH23_BASIC_CFG: 0x40007180

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|----------|-------|---------|---|---|-------|
| SW Access:Reset | NA:UU | | R/W:0 | R/W:0 | R/W:000 | | | R/W:0 |
| HW Access | NA | | R | R | R | | | R |
| Name | | | work_sep | rr_en | pri | | | en |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

1.3.1116 PHUB_CH[0..23]_BASIC_CFG (continued)

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Each channel will have the following basic configuration stored in gates inside PHUB.

| Bits | Name | Description |
|------|----------|--|
| 5 | work_sep | <p>If a TD requires multiple bursts DMAC must remember where it left off between bursts while allowing interleaving other channels' bus access. It can either store the intermediate TD states on top of the current CHn_ORIG_TD0/1 of the TD chain, OR it can store it separately in a working area called CHn_SEP_TD0/1. The latter allows the original TD chain to be preserved.</p> <p>0: Store the intermediate and final TD states on top of the original TD chain. Intermediate state storage allows the CPU to gauge progress of a particular TD. Final state storage allows the CPU to 'walk the chain' later and see what the final completion state of each TD was.</p> <p>1: Store the intermediate TD states separately in CHn_SEP_TD0/1 to preserve the original TD chain. Intermediate state storage allows the CPU to gauge progress of a particular TD. Note the final state of each TD is not stored anywhere in this case. CHn_SEP_TD0/1 is stored in TDMEM and the address is:</p> <p>{00, CH_NUM[5:0], 000}</p> <p>In other words the slot in TDMEM that equals the channel number becomes reserved for DMAC's private use. Instead of processing the original TDs in place, DMAC will copy the original TDs to this separate working area and process them there. Because of this the separate working area is considered reserved and no real TDs should be stored there.</p> |
| 4 | rr_en | <p>Round-Robin enable</p> <p>RR_EN is only valid if the cfg_ch_recent_cnt_size[2:0] input to PHUB is not zero; otherwise RR_EN is hardwired to zero.</p> |
| 3:1 | pri[2:0] | Channel priority; see DMA Arbiter section for description of channel priorities |
| 0 | en | <p>0: Channel is disabled from accepting requests. This is the default state of the channel and allows the channel to be fully configured before enabling. This can also be used to stall a chain.</p> <p>If TD_ACTIVE=0 then clearing this bit will prevent any further DMA requests from being accepted by the channel until ENABLE is set again.</p> <p>If TD_ACTIVE=1 then DMAC will allow the current burst to finish naturally. Then when DMAC returns to the IDLE state it will prevent any further DMA requests from being accepted by the channel until ENABLE is set again.</p> <p>If a TD chain finishes due to NEXT_TD_PTR=0xFE then the ENABLE bit will be cleared automatically (this is not the case if the TD chain finishes due to NEXT_TD_PTR=0xFF).</p> <p>1: channel is enabled and will accept DMA requests for it</p> |

1.3.1117 PHUB_CH[0..23]_ACTION

Channel Action

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|------------------------------|------------------------------|
| PHUB_CH0_ACTION: 0x40007014 | PHUB_CH1_ACTION: 0x40007024 |
| PHUB_CH2_ACTION: 0x40007034 | PHUB_CH3_ACTION: 0x40007044 |
| PHUB_CH4_ACTION: 0x40007054 | PHUB_CH5_ACTION: 0x40007064 |
| PHUB_CH6_ACTION: 0x40007074 | PHUB_CH7_ACTION: 0x40007084 |
| PHUB_CH8_ACTION: 0x40007094 | PHUB_CH9_ACTION: 0x400070A4 |
| PHUB_CH10_ACTION: 0x400070B4 | PHUB_CH11_ACTION: 0x400070C4 |
| PHUB_CH12_ACTION: 0x400070D4 | PHUB_CH13_ACTION: 0x400070E4 |
| PHUB_CH14_ACTION: 0x400070F4 | PHUB_CH15_ACTION: 0x40007104 |
| PHUB_CH16_ACTION: 0x40007114 | PHUB_CH17_ACTION: 0x40007124 |
| PHUB_CH18_ACTION: 0x40007134 | PHUB_CH19_ACTION: 0x40007144 |
| PHUB_CH20_ACTION: 0x40007154 | PHUB_CH21_ACTION: 0x40007164 |
| PHUB_CH22_ACTION: 0x40007174 | PHUB_CH23_ACTION: 0x40007184 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|--------------------|-------------|-----------|
| SW Access:Reset | NA:UUUUU | | | | | R/WOSET:0 | R/WOSET:0 | R/WOSET:0 |
| HW Access | NA | | | | | R/W | R/W | R/W |
| Name | | | | | | cpu_term_c hain | cpu_term_td | cpu_req |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Each channel will have the following action register associated with it:

| Bits | Name | Description |
|------|------|-------------|
|------|------|-------------|

1.3.1117 PHUB_CH[0..23]_ACTION (continued)

| | | |
|---|----------------|---|
| 2 | cpu_term_chain | <p>Setting this bit causes the TD chain to terminate and the channel's ENABLE and CHAIN_ACTIVE bits to clear.</p> <p>If TD_ACTIVE=0 setting this bit will effectively create a request for the channel. When the request wins the DMAC will do some housekeeping associated with terminating a chain which includes clearing the channel's ENABLE, CHAIN_ACTIVE and CPU_TERM_CHAIN bits.</p> <p>If TD_ACTIVE=1 then DMAC will terminate the current burst as soon as any outstanding AHB requests are completed. The channel's ENABLE, CHAIN_ACTIVE and CPU_TERM_CHAIN bits will be cleared when the DMAC returns to the IDLE state.</p> |
| 1 | cpu_term_td | <p>Setting this bit causes the current TD to terminate regardless of the status of the XFRCNT associated with the TD.</p> <p>If TD_ACTIVE=0 the CPU_TERM_TD bit will just wait in the background. When the channel is eventually requested and serviced by DMAC the data burst will be preempted and the TD will complete just as if XFRCNT had expired. When the DMAC FSM returns to the IDLE state it will clear the CPU_TERM_TD bit.</p> <p>If TD_ACTIVE=1 then DMAC will terminate the current burst as soon as any outstanding AHB requests are completed. The TD will then complete just as if XFRCNT had expired. When the DMAC FSM returns to the IDLE state it will clear the CPU_TERM_TD bit.</p> |
| 0 | cpu_req | <p>Setting this bit creates a direct DMA request for the channel.</p> <p>If TD_ACTIVE=0 CPU_REQ will remain set until the request wins arbitration and is accepted by DMAC. This bit is cleared upon triggering the DMAC FSM from the IDLE state.</p> <p>If TD_ACTIVE=1 CPU_REQ will remain set and will apply to the next burst for the channel. The bit will essentially be ignored by DMAC and will be left alone so that it can trigger the next burst for the channel.</p> |

1.3.1118 PHUB_CH[0..23]_BASIC_STATUS

Channel Basic Status Register

Reset: Reset Signals Listed Below

Register : Address

PHUB_CH0_BASIC_STATUS: 0x40007018
 PHUB_CH1_BASIC_STATUS: 0x40007028
 PHUB_CH2_BASIC_STATUS: 0x40007038
 PHUB_CH3_BASIC_STATUS: 0x40007048
 PHUB_CH4_BASIC_STATUS: 0x40007058
 PHUB_CH5_BASIC_STATUS: 0x40007068
 PHUB_CH6_BASIC_STATUS: 0x40007078
 PHUB_CH7_BASIC_STATUS: 0x40007088
 PHUB_CH8_BASIC_STATUS: 0x40007098
 PHUB_CH9_BASIC_STATUS: 0x400070A8
 PHUB_CH10_BASIC_STATUS: 0x400070B8
 PHUB_CH11_BASIC_STATUS: 0x400070C8
 PHUB_CH12_BASIC_STATUS: 0x400070D8
 PHUB_CH13_BASIC_STATUS: 0x400070E8
 PHUB_CH14_BASIC_STATUS: 0x400070F8
 PHUB_CH15_BASIC_STATUS: 0x40007108
 PHUB_CH16_BASIC_STATUS: 0x40007118
 PHUB_CH17_BASIC_STATUS: 0x40007128
 PHUB_CH18_BASIC_STATUS: 0x40007138
 PHUB_CH19_BASIC_STATUS: 0x40007148
 PHUB_CH20_BASIC_STATUS: 0x40007158
 PHUB_CH21_BASIC_STATUS: 0x40007168
 PHUB_CH22_BASIC_STATUS: 0x40007178
 PHUB_CH23_BASIC_STATUS: 0x40007188

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|-------------|----|----|------|-------|-----------|--------------|
| SW Access:Reset | R:1111 | | | | NA:U | R/W:0 | R:0 | R:0 |
| HW Access | R/W | | | | NA | R/W | R/W | R/W |
| Name | rr_cnt | | | | | drq | td_active | chain_active |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:U | R/W:UUUUUUU | | | | | | |
| HW Access | NA | R/W | | | | | | |

1.3.1118 PHUB_CH[0..23]_BASIC_STATUS (continued)

| Name | td_ptr | | | | | | | |
|-----------------|-------------|----|----|----|----|----|----|----|
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:UUUUUUUU | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Each channel will have the following status information stored in gates inside PHUB

| Bits | Name | Description |
|------|--------------|---|
| 14:8 | td_ptr[6:0] | <p>Address pointer to the current CHn_ORIG_TD0/1 in the chain. The CPU initializes this to the location of the first TD in the chain before enabling the channel. DMAC updates TD_PTR with NEXT_TD when it completes the current TD. This gives status to the CPU of how far along the chain is and where it is.</p> <p>The CHn_ORIG_TD0/1 chain is stored in TDMEM and DMAC accesses the current TD at: {TD_PTR[7:0], 000}</p> <p>The number of valid TD_PTR bits is determined by the cfg_ch_td_ptr_size[3:0] input to PHUB; non-configured bits are hardwired to 0. br] TD_PTR resets to the same value as the channel number.</p> |
| 7:4 | rr_cnt[3:0] | <p>Current state of the channel's Round-Robin counter. The lower the value the more recently the channel has won a DMA grant with zero meaning it won the last grant.</p> <p>0: RR_CNT will be frozen on the terminal count (all ones) and therefore it will look as if the channel has never received a DMA grant which will give it an advantage over channels that do support Round-Robin. Put another way, when RR_EN=0 the channel is not subject to Round-Robin rules.</p> <p>1: RR_CNT will reset each time the channel wins a DMA grant. It will increment each time any other channel wins a DMA grant. It will stop incrementing when it hits the terminal count (all ones).</p> <p>The number of valid RR_CNT bits is determined by the cfg_ch_recent_cnt_size[2:0] input to PHUB; non-configured bits are hardwired to 0.</p> |
| 2 | drq | <p>0: hardware DRQ bit is not set</p> <p>1: hardware DRQ bit is set and is awaiting service by DMAC; will be cleared by DMAC when serviced or by SW by writing a 1</p> |
| 1 | td_active | <p>0: channel is not currently being serviced by DMAC</p> <p>1: channel is currently being serviced by DMAC</p> |
| 0 | chain_active | <p>0: TD chain is inactive; either no DMA requests have triggered a new chain or the previous chain has completed.</p> <p>1: TD chain has been triggered by a DMA request</p> |

1.3.1118 PHUB_CH[0..23]_BASIC_STATUS (continued)

Reset Table

| resetsignal | field(s) |
|--|---|
| N/A | td_ptr[6:0] |
| System reset for retention flops [reset_all_retention] | chain_active, td_active, drq, rr_cnt[3:0] |

1.3.1119 PHUB_CFGMEM[0..23]_CFG0

PHUB Channel Configuration Register 0

Reset: N/A

Register : Address

PHUB_CFGMEM0_CFG0: 0x40007600

PHUB_CFGMEM1_CFG0: 0x40007608

PHUB_CFGMEM2_CFG0: 0x40007610

PHUB_CFGMEM3_CFG0: 0x40007618

PHUB_CFGMEM4_CFG0: 0x40007620

PHUB_CFGMEM5_CFG0: 0x40007628

PHUB_CFGMEM6_CFG0: 0x40007630

PHUB_CFGMEM7_CFG0: 0x40007638

PHUB_CFGMEM8_CFG0: 0x40007640

PHUB_CFGMEM9_CFG0: 0x40007648

PHUB_CFGMEM10_CFG0: 0x40007650

PHUB_CFGMEM11_CFG0: 0x40007658

PHUB_CFGMEM12_CFG0: 0x40007660

PHUB_CFGMEM13_CFG0: 0x40007668

PHUB_CFGMEM14_CFG0: 0x40007670

PHUB_CFGMEM15_CFG0: 0x40007678

PHUB_CFGMEM16_CFG0: 0x40007680

PHUB_CFGMEM17_CFG0: 0x40007688

PHUB_CFGMEM18_CFG0: 0x40007690

PHUB_CFGMEM19_CFG0: 0x40007698

PHUB_CFGMEM20_CFG0: 0x400076A0

PHUB_CFGMEM21_CFG0: 0x400076A8

PHUB_CFGMEM22_CFG0: 0x400076B0

PHUB_CFGMEM23_CFG0: 0x400076B8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|-------------|---|---|---|---|---|---|
| SW Access:Reset | R/W:U | R/W:UUUUUUU | | | | | | |
| HW Access | R | R | | | | | | |
| Name | req_per_burst | burstcnt | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|----------|----|----|----|----------|----|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |

1.3.1119 PHUB_CFGMEM[0..23]_CFG0 (continued)

| | | | | | | | | |
|-----------------|-------------------|-----------|-----------|--------------------------|--------------|-----------|-----------|-----------|
| Name | termout1_sel | | | | termout0_sel | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:UUU | | | R/W:U | R/W:UUUU | | | |
| HW Access | NA | | | R | R | | | |
| Name | | | | wait_udb_fl ag_settle | termin_sel | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUU | | | | | | | NA:U |
| HW Access | R | | | | | | | NA |
| Name | burstcount_remain | | | | | | | |

Each channel will have some configuration information stored in RAM, and this configuration information is called CHn_CFG0/1. CHn_CFG0/1 are stored in CFGMEM at {CH_NUM[5:0], 000}. CHn_CFG0/1 are described in detail below.

| Bits | Name | Description |
|-------|------------------------|---|
| 31:25 | burstcount_remain[6:0] | These bits are reserved for use by the DMAC in storing the intermediate state of BURSTCNT in the event that the channel is interrupted mid-burst by a higher priority channel. These bits need to be preserved by SW only if the channel is active and interrupt-able. Otherwise SW can overwrite these bits without concern, for instance when initially setting up the configuration for the channel. |
| 20 | wait_udb_flag_settle | UDB FIFO flags may be used directly as a DRQ to the DMAC. However, these flags can take multiple cycles to settle. Setting this bit instructs the DMAC to wait an extra cycle after finishing a DMA for this channel before considering a new DRQ. Otherwise a DRQ may be interpreted prematurely. |
| 19:16 | termin_sel[3:0] | Selects 1 of the 16 TERMIN[15:0] inputs to PHUB for use in terminating a TD. Any active high strobe on the TERMIN signal will be positive edge detected and will cause the TD to terminate if TERMIN_EN is set in the TD. The TD will complete just as if XFRCNT expired. |
| 15:12 | termout1_sel[3:0] | Selects 1 of the 16 TERMOUT1[15:0] outputs from PHUB to be toggled upon completion of the current TD if TERMOUT1_EN is set in the TD. Because the frequency of the receiving logic for the TERMOUT1 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT1 signal and interpret either as the completion of the current TD. |
| 11:8 | termout0_sel[3:0] | Selects 1 of the 16 TERMOUT0[15:0] outputs from PHUB to be toggled upon completion of the current TD if TERMOUT0_EN is set in the TD. Because the frequency of the receiving logic for the TERMOUT0 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT0 signal and interpret either as the completion of the current TD. |
| 7 | req_per_burst | 0: A DMA request is required to activate each TD in the chain. If the TD requires multiple bursts to complete then all subsequent bursts after the first burst will be automatically requested and carried out. DMAC will set the AUTO_BURST_WHOLE_TD request after completing each burst except the last. 1: A DMA request is required to activate each TD in the chain. If the TD requires multiple bursts to complete then all subsequent bursts after the first burst must also be individually requested. |

1.3.1119 PHUB_CFGMEM[0..23]_CFG0 (continued)

| | | |
|-----|---------------|--|
| 6:0 | burstcnt[6:0] | <p>The data block moved by a TD can be broken up into small bursts. BURSTCNT[6:0] specifies the length of the small burst from 1 to 127 bytes. If BURSTCNT=0 this means do not break the data block into small bursts and instead burst the whole XFRCNT in one burst.</p> <p>The number of valid BURSTCNT bits is determined by the <code>cfg_burstcnt_size[2:0]</code> input to PHUB; non-configured bits are ignored by the DMAC.</p> |
|-----|---------------|--|

1.3.1120 PHUB_CFGMEM[0..23]_CFG1

PHUB Channel Configuration Register 1

Reset: N/A

Register : Address

PHUB_CFGMEM0_CFG1: 0x40007604
 PHUB_CFGMEM1_CFG1: 0x4000760C
 PHUB_CFGMEM2_CFG1: 0x40007614
 PHUB_CFGMEM3_CFG1: 0x4000761C
 PHUB_CFGMEM4_CFG1: 0x40007624
 PHUB_CFGMEM5_CFG1: 0x4000762C
 PHUB_CFGMEM6_CFG1: 0x40007634
 PHUB_CFGMEM7_CFG1: 0x4000763C
 PHUB_CFGMEM8_CFG1: 0x40007644
 PHUB_CFGMEM9_CFG1: 0x4000764C
 PHUB_CFGMEM10_CFG1: 0x40007654
 PHUB_CFGMEM11_CFG1: 0x4000765C
 PHUB_CFGMEM12_CFG1: 0x40007664
 PHUB_CFGMEM13_CFG1: 0x4000766C
 PHUB_CFGMEM14_CFG1: 0x40007674
 PHUB_CFGMEM15_CFG1: 0x4000767C
 PHUB_CFGMEM16_CFG1: 0x40007684
 PHUB_CFGMEM17_CFG1: 0x4000768C
 PHUB_CFGMEM18_CFG1: 0x40007694
 PHUB_CFGMEM19_CFG1: 0x4000769C
 PHUB_CFGMEM20_CFG1: 0x400076A4
 PHUB_CFGMEM21_CFG1: 0x400076AC
 PHUB_CFGMEM22_CFG1: 0x400076B4
 PHUB_CFGMEM23_CFG1: 0x400076BC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | src_base_adr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | src_base_adr | | | | | | | |

@0x40007600 + [0..23 * 0x8] + 0x4

1.3.1120 PHUB_CFGMEM[0..23]_CFG1 (continued)

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dst_base_adr | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | dst_base_adr | | | | | | | |

Each channel will have some configuration information stored in RAM, and this configuration information is called CHn_CFG0/1. CHn_CFG0/1 are stored in CFGMEM at {CH_NUM[5:0], 000}. Chn_CFG0/1 are described in detail below.

| Bits | Name | Description |
|-------|--------------------|--|
| 31:16 | dst_base_adr[15:0] | Base address used for the destination address. Concatenates with DST_ADR[15:0] from the TD to form the full address. |
| 15:0 | src_base_adr[15:0] | Base address used for the source address. Concatenates with SRC_ADR[15:0] from the TD to form the full source address. |

1.3.1121 PHUB_TDMEM[0..127]_ORIG_TD0

PHUB Original Transaction Descriptor 0

Reset: N/A

Register : Address

PHUB_TDMEM0_ORIG_TD0: 0x40007800
PHUB_TDMEM1_ORIG_TD0: 0x40007808
PHUB_TDMEM2_ORIG_TD0: 0x40007810
PHUB_TDMEM3_ORIG_TD0: 0x40007818
PHUB_TDMEM4_ORIG_TD0: 0x40007820
PHUB_TDMEM5_ORIG_TD0: 0x40007828
PHUB_TDMEM6_ORIG_TD0: 0x40007830
PHUB_TDMEM7_ORIG_TD0: 0x40007838
PHUB_TDMEM8_ORIG_TD0: 0x40007840
PHUB_TDMEM9_ORIG_TD0: 0x40007848
PHUB_TDMEM10_ORIG_TD0: 0x40007850
PHUB_TDMEM11_ORIG_TD0: 0x40007858
PHUB_TDMEM12_ORIG_TD0: 0x40007860
PHUB_TDMEM13_ORIG_TD0: 0x40007868
PHUB_TDMEM14_ORIG_TD0: 0x40007870
PHUB_TDMEM15_ORIG_TD0: 0x40007878
PHUB_TDMEM16_ORIG_TD0: 0x40007880
PHUB_TDMEM17_ORIG_TD0: 0x40007888
PHUB_TDMEM18_ORIG_TD0: 0x40007890
PHUB_TDMEM19_ORIG_TD0: 0x40007898
PHUB_TDMEM20_ORIG_TD0: 0x400078A0
PHUB_TDMEM21_ORIG_TD0: 0x400078A8
PHUB_TDMEM22_ORIG_TD0: 0x400078B0
PHUB_TDMEM23_ORIG_TD0: 0x400078B8
PHUB_TDMEM24_ORIG_TD0: 0x400078C0
PHUB_TDMEM25_ORIG_TD0: 0x400078C8
PHUB_TDMEM26_ORIG_TD0: 0x400078D0
PHUB_TDMEM27_ORIG_TD0: 0x400078D8
PHUB_TDMEM28_ORIG_TD0: 0x400078E0
PHUB_TDMEM29_ORIG_TD0: 0x400078E8
PHUB_TDMEM30_ORIG_TD0: 0x400078F0
PHUB_TDMEM31_ORIG_TD0: 0x400078F8

1.3.1121 PHUB_TDMEM[0..127]_ORIG_TDO (continued)

Register : Address

PHUB_TDMEM32_ORIG_TDO: 0x40007900

PHUB_TDMEM33_ORIG_TDO: 0x40007908

PHUB_TDMEM34_ORIG_TDO: 0x40007910

PHUB_TDMEM35_ORIG_TDO: 0x40007918

PHUB_TDMEM36_ORIG_TDO: 0x40007920

PHUB_TDMEM37_ORIG_TDO: 0x40007928

PHUB_TDMEM38_ORIG_TDO: 0x40007930

PHUB_TDMEM39_ORIG_TDO: 0x40007938

PHUB_TDMEM40_ORIG_TDO: 0x40007940

PHUB_TDMEM41_ORIG_TDO: 0x40007948

PHUB_TDMEM42_ORIG_TDO: 0x40007950

PHUB_TDMEM43_ORIG_TDO: 0x40007958

PHUB_TDMEM44_ORIG_TDO: 0x40007960

PHUB_TDMEM45_ORIG_TDO: 0x40007968

PHUB_TDMEM46_ORIG_TDO: 0x40007970

PHUB_TDMEM47_ORIG_TDO: 0x40007978

PHUB_TDMEM48_ORIG_TDO: 0x40007980

PHUB_TDMEM49_ORIG_TDO: 0x40007988

PHUB_TDMEM50_ORIG_TDO: 0x40007990

PHUB_TDMEM51_ORIG_TDO: 0x40007998

PHUB_TDMEM52_ORIG_TDO: 0x400079A0

PHUB_TDMEM53_ORIG_TDO: 0x400079A8

PHUB_TDMEM54_ORIG_TDO: 0x400079B0

PHUB_TDMEM55_ORIG_TDO: 0x400079B8

PHUB_TDMEM56_ORIG_TDO: 0x400079C0

PHUB_TDMEM57_ORIG_TDO: 0x400079C8

PHUB_TDMEM58_ORIG_TDO: 0x400079D0

PHUB_TDMEM59_ORIG_TDO: 0x400079D8

PHUB_TDMEM60_ORIG_TDO: 0x400079E0

PHUB_TDMEM61_ORIG_TDO: 0x400079E8

PHUB_TDMEM62_ORIG_TDO: 0x400079F0

PHUB_TDMEM63_ORIG_TDO: 0x400079F8

PHUB_TDMEM64_ORIG_TDO: 0x40007A00

PHUB_TDMEM65_ORIG_TDO: 0x40007A08

PHUB_TDMEM66_ORIG_TDO: 0x40007A10

PHUB_TDMEM67_ORIG_TDO: 0x40007A18

1.3.1121 PHUB_TDMEM[0..127]_ORIG_TD0 (continued)

Register : Address

PHUB_TDMEM68_ORIG_TD0: 0x40007A20
PHUB_TDMEM69_ORIG_TD0: 0x40007A28
PHUB_TDMEM70_ORIG_TD0: 0x40007A30
PHUB_TDMEM71_ORIG_TD0: 0x40007A38
PHUB_TDMEM72_ORIG_TD0: 0x40007A40
PHUB_TDMEM73_ORIG_TD0: 0x40007A48
PHUB_TDMEM74_ORIG_TD0: 0x40007A50
PHUB_TDMEM75_ORIG_TD0: 0x40007A58
PHUB_TDMEM76_ORIG_TD0: 0x40007A60
PHUB_TDMEM77_ORIG_TD0: 0x40007A68
PHUB_TDMEM78_ORIG_TD0: 0x40007A70
PHUB_TDMEM79_ORIG_TD0: 0x40007A78
PHUB_TDMEM80_ORIG_TD0: 0x40007A80
PHUB_TDMEM81_ORIG_TD0: 0x40007A88
PHUB_TDMEM82_ORIG_TD0: 0x40007A90
PHUB_TDMEM83_ORIG_TD0: 0x40007A98
PHUB_TDMEM84_ORIG_TD0: 0x40007AA0
PHUB_TDMEM85_ORIG_TD0: 0x40007AA8
PHUB_TDMEM86_ORIG_TD0: 0x40007AB0
PHUB_TDMEM87_ORIG_TD0: 0x40007AB8
PHUB_TDMEM88_ORIG_TD0: 0x40007AC0
PHUB_TDMEM89_ORIG_TD0: 0x40007AC8
PHUB_TDMEM90_ORIG_TD0: 0x40007AD0
PHUB_TDMEM91_ORIG_TD0: 0x40007AD8
PHUB_TDMEM92_ORIG_TD0: 0x40007AE0
PHUB_TDMEM93_ORIG_TD0: 0x40007AE8
PHUB_TDMEM94_ORIG_TD0: 0x40007AF0
PHUB_TDMEM95_ORIG_TD0: 0x40007AF8
PHUB_TDMEM96_ORIG_TD0: 0x40007B00
PHUB_TDMEM97_ORIG_TD0: 0x40007B08
PHUB_TDMEM98_ORIG_TD0: 0x40007B10
PHUB_TDMEM99_ORIG_TD0: 0x40007B18
PHUB_TDMEM100_ORIG_TD0: 0x40007B20
PHUB_TDMEM101_ORIG_TD0: 0x40007B28
PHUB_TDMEM102_ORIG_TD0: 0x40007B30
PHUB_TDMEM103_ORIG_TD0: 0x40007B38

1.3.1121 PHUB_TDMEM[0..127]_ORIG_TD0 (continued)

Register : Address

PHUB_TDMEM104_ORIG_TD0: 0x40007B40

PHUB_TDMEM105_ORIG_TD0: 0x40007B48

PHUB_TDMEM106_ORIG_TD0: 0x40007B50

PHUB_TDMEM107_ORIG_TD0: 0x40007B58

PHUB_TDMEM108_ORIG_TD0: 0x40007B60

PHUB_TDMEM109_ORIG_TD0: 0x40007B68

PHUB_TDMEM110_ORIG_TD0: 0x40007B70

PHUB_TDMEM111_ORIG_TD0: 0x40007B78

PHUB_TDMEM112_ORIG_TD0: 0x40007B80

PHUB_TDMEM113_ORIG_TD0: 0x40007B88

PHUB_TDMEM114_ORIG_TD0: 0x40007B90

PHUB_TDMEM115_ORIG_TD0: 0x40007B98

PHUB_TDMEM116_ORIG_TD0: 0x40007BA0

PHUB_TDMEM117_ORIG_TD0: 0x40007BA8

PHUB_TDMEM118_ORIG_TD0: 0x40007BB0

PHUB_TDMEM119_ORIG_TD0: 0x40007BB8

PHUB_TDMEM120_ORIG_TD0: 0x40007BC0

PHUB_TDMEM121_ORIG_TD0: 0x40007BC8

PHUB_TDMEM122_ORIG_TD0: 0x40007BD0

PHUB_TDMEM123_ORIG_TD0: 0x40007BD8

PHUB_TDMEM124_ORIG_TD0: 0x40007BE0

PHUB_TDMEM125_ORIG_TD0: 0x40007BE8

PHUB_TDMEM126_ORIG_TD0: 0x40007BF0

PHUB_TDMEM127_ORIG_TD0: 0x40007BF8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | xfrcnt | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|---------|----|----|----|----------|----|---|---|
| SW Access:Reset | NA:UUUU | | | | R/W:UUUU | | | |
| HW Access | NA | | | | R/W | | | |
| Name | | | | | xfrcnt | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |

1.3.1121 PHUB_TDMEM[0..127]_ORIG_TD0 (continued)

| | | | | | | | | |
|-----------------|-------------|-----------|----------------|-----------|-------------|-------------|-------------|-------------|
| HW Access | R | | | | | | | |
| Name | next_td_ptr | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | R | R | R | R | R | R | R |
| Name | swap_en | swap_size | auto_exec_next | termin_en | termout1_en | termout0_en | inc_dst_adr | inc_src_adr |

Each channel will have a TD chain (as short as one TD in length) that provides instructions to the DMAC for carrying out a DMA sequence for the channel. This is described in greater detail in the 'TD Chains' section to follow. The TD chain is comprised of one or more CHn_ORIG_TD0/1 TDs. DMAC accesses the CHn_ORIG_TD0/1 chain from TDMEM and the address in TDMEM of the current TD in the chain is {TD_PTR[7:0], 000}. TD_PTR for the first TD in a chain is initialized by the CPU. As the chain progresses through TDs the TD_PTR will be automatically updated by DMAC to reflect the current TD being accessed in the chain. CHn_ORIG_TD0/1 are described in detail below.

| Bits | Name | Description |
|------|----------------|--|
| 31 | swap_en | 0: Do not perform endian swap 1: Perform endian swap. BURSTCNT and XFRcnt must be an integer multiple of SWAP_SIZE. |
| 30 | swap_size | Only valid if SWAP_EN=1. 0: Swap size = 2 bytes, meaning every 2 bytes are endian swapped during the DMA transfer. 1: Swap size = 4 bytes, meaning every 4 bytes are endian swapped during the DMA transfer. |
| 29 | auto_exec_next | 0: The next TD in the chain requires a CPU_REQ or peripheral request in order to trigger 1: The next TD in the chain will trigger automatically when the current TD completes. The DMAC will create an AUTO_EXEC_NEXT_TD request for the channel when it completes the current TD. |
| 28 | termin_en | 0: Do not terminate this TD based on a TERMIN signal. 1: Terminate this TD if a positive edge on the TERMIN signal selected by TERMIN_SEL is detected. Any ongoing burst will terminate as soon as any outstanding AHB requests have been completed. The TD will then complete just as if XFRcnt expired. TBD: describe when TERMIN signal can activate, when it gets considered (TD_ACTIVE 0/1) and when it gets cleared. |
| 27 | termout1_en | 0: Do not toggle a TERMOUT1 signal when this TD completes 1: When this TD completes the TERMOUT1 signal selected by TERMOUT1_SEL will toggle. Because the frequency of the receiving logic for the TERMOUT1 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT1 signal and interpret either as the completion of the current TD. |
| 26 | termout0_en | 0: Do not toggle a TERMOUT0 signal when the TD completes 1: When this TD completes the TERMOUT0 signal selected by TERMOUT0_SEL will toggle. Because the frequency of the receiving logic for the TERMOUT0 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT0 signal and interpret either as the completion of the current TD. |

1.3.1121 PHUB_TDMEM[0..127]_ORIG_TD0 (continued)

| | | |
|-------|------------------|--|
| 25 | inc_dst_adr | <p>0: Freeze DST_ADR throughout the burst</p> <p>1: Increment DST_ADR according to the size of each data transaction in the burst</p> |
| 24 | inc_src_adr | <p>0: Freeze SRC_ADR throughout the burst</p> <p>1: Increment SRC_ADR according to the size of each data transaction in the burst</p> |
| 23:16 | next_td_ptr[7:0] | <p>Specifies the next TD to be executed in the chain when this TD completes. When this TD completes the value of NEXT_TD_PTR is copied into the TD_PTR status register to allow the CPU to see where in the chain the channel is.</p> <p>If NEXT_TD_PTR=0xFE or 0xFF then this is the last TD in the chain. When the last TD in a chain completes DMAC will clear CHAIN_ACTIVE and if NEXT_TD_PTR=0xFE then ENABLE will clear as well.</p> |
| 11:0 | xfrcnt[11:0] | <p>Transfer count in bytes from 1 to 4KB-1, or indefinite transfer count if set to 0.</p> <p>1. Setting XFRCNT to 0:</p> <p>This means transfer count is not used to terminate the TD. An indefinite amount of data can be transferred in this mode. The TD must be terminated either by TERMIN, CPU_TERM_TD or CPU_TERM_CHAIN.</p> <p>Data movement is broken into bursts according to BURSTCNT. Note in the special case where both XFRCNT and BURSTCNT are 0 data will be transferred indefinitely and without interruption.</p> <p>2. Setting XFRCNT to non-0:</p> <p>This means the XFRCNT is used to determine how much data will be transferred (1 to 4KB-1).</p> <p>If BURSTCNT=0 then DMAC will transfer the entire XFRCNT worth of data in one burst.</p> <p>If BURSTCNT is not 0 and BURSTCNT represents a value that is greater than or equal to XFRCNT then DMAC will transfer the entire XFRCNT worth of data in one burst.</p> <p>If BURSTCNT is not 0 and BURSTCNT represents a value that is less than XFRCNT then DMAC will break the data movement into multiple bursts as dictated by BURSTCNT. See the description for the REQ_PER_BURST bit for how subsequent bursts are triggered.</p> <p>At any point the TD can terminate before exhausting the XFRCNT due to TERMIN, CPU_TERM_TD or CPU_TERM_CHAIN.</p> <p>When DMAC updates the TD (whether it's the CHn_ORIG_TD0/1 or CHn_SEP_TD0/1) at the end of a burst it will update the XFRCNT to reflect the newly decremented value based on the number of bytes that were transferred in the burst.</p> <p>The number of valid XFRCNT bits is determined by the cfg_xfrcnt_size[4:0] input to PHUB; non-configured bits are ignored by the DMAC.</p> |

1.3.1122 PHUB_TDMEM[0..127]_ORIG_TD1

PHUB Original Transaction Descriptor 0

Reset: N/A

Register : Address

PHUB_TDMEM0_ORIG_TD1: 0x40007804
PHUB_TDMEM1_ORIG_TD1: 0x4000780C
PHUB_TDMEM2_ORIG_TD1: 0x40007814
PHUB_TDMEM3_ORIG_TD1: 0x4000781C
PHUB_TDMEM4_ORIG_TD1: 0x40007824
PHUB_TDMEM5_ORIG_TD1: 0x4000782C
PHUB_TDMEM6_ORIG_TD1: 0x40007834
PHUB_TDMEM7_ORIG_TD1: 0x4000783C
PHUB_TDMEM8_ORIG_TD1: 0x40007844
PHUB_TDMEM9_ORIG_TD1: 0x4000784C
PHUB_TDMEM10_ORIG_TD1: 0x40007854
PHUB_TDMEM11_ORIG_TD1: 0x4000785C
PHUB_TDMEM12_ORIG_TD1: 0x40007864
PHUB_TDMEM13_ORIG_TD1: 0x4000786C
PHUB_TDMEM14_ORIG_TD1: 0x40007874
PHUB_TDMEM15_ORIG_TD1: 0x4000787C
PHUB_TDMEM16_ORIG_TD1: 0x40007884
PHUB_TDMEM17_ORIG_TD1: 0x4000788C
PHUB_TDMEM18_ORIG_TD1: 0x40007894
PHUB_TDMEM19_ORIG_TD1: 0x4000789C
PHUB_TDMEM20_ORIG_TD1: 0x400078A4
PHUB_TDMEM21_ORIG_TD1: 0x400078AC
PHUB_TDMEM22_ORIG_TD1: 0x400078B4
PHUB_TDMEM23_ORIG_TD1: 0x400078BC
PHUB_TDMEM24_ORIG_TD1: 0x400078C4
PHUB_TDMEM25_ORIG_TD1: 0x400078CC
PHUB_TDMEM26_ORIG_TD1: 0x400078D4
PHUB_TDMEM27_ORIG_TD1: 0x400078DC
PHUB_TDMEM28_ORIG_TD1: 0x400078E4
PHUB_TDMEM29_ORIG_TD1: 0x400078EC
PHUB_TDMEM30_ORIG_TD1: 0x400078F4
PHUB_TDMEM31_ORIG_TD1: 0x400078FC

1.3.1122 PHUB_TDMEM[0..127]_ORIG_TD1 (continued)

Register : Address

PHUB_TDMEM32_ORIG_TD1: 0x40007904
PHUB_TDMEM33_ORIG_TD1: 0x4000790C
PHUB_TDMEM34_ORIG_TD1: 0x40007914
PHUB_TDMEM35_ORIG_TD1: 0x4000791C
PHUB_TDMEM36_ORIG_TD1: 0x40007924
PHUB_TDMEM37_ORIG_TD1: 0x4000792C
PHUB_TDMEM38_ORIG_TD1: 0x40007934
PHUB_TDMEM39_ORIG_TD1: 0x4000793C
PHUB_TDMEM40_ORIG_TD1: 0x40007944
PHUB_TDMEM41_ORIG_TD1: 0x4000794C
PHUB_TDMEM42_ORIG_TD1: 0x40007954
PHUB_TDMEM43_ORIG_TD1: 0x4000795C
PHUB_TDMEM44_ORIG_TD1: 0x40007964
PHUB_TDMEM45_ORIG_TD1: 0x4000796C
PHUB_TDMEM46_ORIG_TD1: 0x40007974
PHUB_TDMEM47_ORIG_TD1: 0x4000797C
PHUB_TDMEM48_ORIG_TD1: 0x40007984
PHUB_TDMEM49_ORIG_TD1: 0x4000798C
PHUB_TDMEM50_ORIG_TD1: 0x40007994
PHUB_TDMEM51_ORIG_TD1: 0x4000799C
PHUB_TDMEM52_ORIG_TD1: 0x400079A4
PHUB_TDMEM53_ORIG_TD1: 0x400079AC
PHUB_TDMEM54_ORIG_TD1: 0x400079B4
PHUB_TDMEM55_ORIG_TD1: 0x400079BC
PHUB_TDMEM56_ORIG_TD1: 0x400079C4
PHUB_TDMEM57_ORIG_TD1: 0x400079CC
PHUB_TDMEM58_ORIG_TD1: 0x400079D4
PHUB_TDMEM59_ORIG_TD1: 0x400079DC
PHUB_TDMEM60_ORIG_TD1: 0x400079E4
PHUB_TDMEM61_ORIG_TD1: 0x400079EC
PHUB_TDMEM62_ORIG_TD1: 0x400079F4
PHUB_TDMEM63_ORIG_TD1: 0x400079FC
PHUB_TDMEM64_ORIG_TD1: 0x40007A04
PHUB_TDMEM65_ORIG_TD1: 0x40007A0C
PHUB_TDMEM66_ORIG_TD1: 0x40007A14
PHUB_TDMEM67_ORIG_TD1: 0x40007A1C

1.3.1122 PHUB_TDMEM[0..127]_ORIG_TD1 (continued)

Register : Address

PHUB_TDMEM68_ORIG_TD1: 0x40007A24
PHUB_TDMEM69_ORIG_TD1: 0x40007A2C
PHUB_TDMEM70_ORIG_TD1: 0x40007A34
PHUB_TDMEM71_ORIG_TD1: 0x40007A3C
PHUB_TDMEM72_ORIG_TD1: 0x40007A44
PHUB_TDMEM73_ORIG_TD1: 0x40007A4C
PHUB_TDMEM74_ORIG_TD1: 0x40007A54
PHUB_TDMEM75_ORIG_TD1: 0x40007A5C
PHUB_TDMEM76_ORIG_TD1: 0x40007A64
PHUB_TDMEM77_ORIG_TD1: 0x40007A6C
PHUB_TDMEM78_ORIG_TD1: 0x40007A74
PHUB_TDMEM79_ORIG_TD1: 0x40007A7C
PHUB_TDMEM80_ORIG_TD1: 0x40007A84
PHUB_TDMEM81_ORIG_TD1: 0x40007A8C
PHUB_TDMEM82_ORIG_TD1: 0x40007A94
PHUB_TDMEM83_ORIG_TD1: 0x40007A9C
PHUB_TDMEM84_ORIG_TD1: 0x40007AA4
PHUB_TDMEM85_ORIG_TD1: 0x40007AAC
PHUB_TDMEM86_ORIG_TD1: 0x40007AB4
PHUB_TDMEM87_ORIG_TD1: 0x40007ABC
PHUB_TDMEM88_ORIG_TD1: 0x40007AC4
PHUB_TDMEM89_ORIG_TD1: 0x40007ACC
PHUB_TDMEM90_ORIG_TD1: 0x40007AD4
PHUB_TDMEM91_ORIG_TD1: 0x40007ADC
PHUB_TDMEM92_ORIG_TD1: 0x40007AE4
PHUB_TDMEM93_ORIG_TD1: 0x40007AEC
PHUB_TDMEM94_ORIG_TD1: 0x40007AF4
PHUB_TDMEM95_ORIG_TD1: 0x40007AFC
PHUB_TDMEM96_ORIG_TD1: 0x40007B04
PHUB_TDMEM97_ORIG_TD1: 0x40007B0C
PHUB_TDMEM98_ORIG_TD1: 0x40007B14
PHUB_TDMEM99_ORIG_TD1: 0x40007B1C
PHUB_TDMEM100_ORIG_TD1: 0x40007B24
PHUB_TDMEM101_ORIG_TD1: 0x40007B2C
PHUB_TDMEM102_ORIG_TD1: 0x40007B34
PHUB_TDMEM103_ORIG_TD1: 0x40007B3C

1.3.1122 PHUB_TDMEM[0..127]_ORIG_TD1 (continued)

Register : Address

PHUB_TDMEM104_ORIG_TD1: 0x40007B44

PHUB_TDMEM105_ORIG_TD1: 0x40007B4C

PHUB_TDMEM106_ORIG_TD1: 0x40007B54

PHUB_TDMEM107_ORIG_TD1: 0x40007B5C

PHUB_TDMEM108_ORIG_TD1: 0x40007B64

PHUB_TDMEM109_ORIG_TD1: 0x40007B6C

PHUB_TDMEM110_ORIG_TD1: 0x40007B74

PHUB_TDMEM111_ORIG_TD1: 0x40007B7C

PHUB_TDMEM112_ORIG_TD1: 0x40007B84

PHUB_TDMEM113_ORIG_TD1: 0x40007B8C

PHUB_TDMEM114_ORIG_TD1: 0x40007B94

PHUB_TDMEM115_ORIG_TD1: 0x40007B9C

PHUB_TDMEM116_ORIG_TD1: 0x40007BA4

PHUB_TDMEM117_ORIG_TD1: 0x40007BAC

PHUB_TDMEM118_ORIG_TD1: 0x40007BB4

PHUB_TDMEM119_ORIG_TD1: 0x40007BBC

PHUB_TDMEM120_ORIG_TD1: 0x40007BC4

PHUB_TDMEM121_ORIG_TD1: 0x40007BCC

PHUB_TDMEM122_ORIG_TD1: 0x40007BD4

PHUB_TDMEM123_ORIG_TD1: 0x40007BDC

PHUB_TDMEM124_ORIG_TD1: 0x40007BE4

PHUB_TDMEM125_ORIG_TD1: 0x40007BEC

PHUB_TDMEM126_ORIG_TD1: 0x40007BF4

PHUB_TDMEM127_ORIG_TD1: 0x40007BFC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | src_adr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | src_adr | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |

1.3.1122 PHUB_TDMEM[0..127]_ORIG_TD1 (continued)

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| HW Access | R/W | | | | | | | |
| Name | dst_adr | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dst_adr | | | | | | | |

Each channel will have a TD chain (as short as one TD in length) that provides instructions to the DMAC for carrying out a DMA sequence for the channel. This is described in greater detail in the 'TD Chains' section to follow. The TD chain is comprised of one or more CHn_ORIG_TD0/1 TDs. DMAC accesses the CHn_ORIG_TD0/1 chain from TDMEM and the address in TDMEM of the current TD in the chain is {TD_PTR[7:0], 000}. TD_PTR for the first TD in a chain is initialized by the CPU. As the chain progresses through TDs the TD_PTR will be automatically updated by DMAC to reflect the current TD being accessed in the chain. CHn_ORIG_TD0/1 are described in detail below.

| Bits | Name | Description |
|-------|---------------|--|
| 31:16 | dst_adr[15:0] | <p>Specifies the lower portion of the full destination address by concatenating with DST_BASE_ADR from CHn_CFG1.</p> <p>Can be incremented or not depending on the setting of INC_DST_ADR. Only DST_ADR will increment; DST_BASE_ADR will remain static. Therefore, separate TDs should be used to cross 64KB address boundaries.</p> <p>If INC_DST_ADR=1 then when DMAC updates the TD (whether it's the CHn_ORIG_TD0/1 or CHn_SEP_TD0/1) at the end of a burst it will update DST_ADR to reflect the newly incremented value based on the number of bytes that were transferred to the destination during the burst.</p> |
| 15:0 | src_adr[15:0] | <p>Specifies the lower portion of the full source address by concatenating with SRC_BASE_ADR from CHn_CFG1.</p> <p>Can be incremented or not depending on the setting of INC_SRC_ADR. Only SRC_ADR will increment; SRC_BASE_ADR will remain static. Therefore, separate TDs should be used to cross 64KB address boundaries.</p> <p>If INC_SRC_ADR=1 then when DMAC updates the TD (whether it's the CHn_ORIG_TD0/1 or CHn_SEP_TD0/1) at the end of a burst it will update SRC_ADR to reflect the newly incremented value based on the number of bytes that were transferred from the source during the burst.</p> |

1.3.1123 EE_DATA[0..2047]

EEPROM Memory

Reset: N/A

Register : Address

EE_DATA: 0x40008000-0x400087FF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|------------------|
| 7:0 | data[7:0] | (no description) |

1.3.1124 CAN[0..0]_CSR_INT_SR

INT_SR

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_INT_SR: 0x4000A000

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---------|-----------|---------|----------|----------|-------|---|
| SW Access:Reset | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | NA:00 | |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | NA | |
| Name | form_err | ack_err | stuff_err | bit_err | ovr_load | arb_loss | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------|----|----|---------|---------|-------------|---------|---------|
| SW Access:Reset | NA:000 | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | R/W | R/W | R/W | R/W | R/W |
| Name | | | | rx_msg | tx_msg | rx_msg_loss | bus_off | crc_err |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The interrupt status register stores internal interrupt events. Once a bit is set it remains set until it is cleared by writing a '1' to it. The interrupt enable register has no effect on the interrupt status register. A pending interrupt occurs when the flag is set to '1'. To acknowledge an interrupt, set the flag to '1'

| Bits | Name | Description |
|------|-------------|-----------------------|
| 12 | rx_msg | Msg Recieved |
| 11 | tx_msg | Tx msg Sent |
| 10 | rx_msg_loss | Rx msg loss Interrupt |
| 9 | bus_off | Bus Off State |
| 8 | crc_err | CRC Error Interrupt |
| 7 | form_err | Form Error Interrupt |
| 6 | ack_err | Ack Error Interrupt |
| 5 | stuff_err | Stuff Error Interrupt |
| 4 | bit_err | Bit Error Interrupt |



0x4000a000

1.3.1124 CAN[0..0]_CSR_INT_SR (continued)

| | | |
|---|----------|--------------------|
| 3 | ovr_load | Overload Interrupt |
| 2 | arb_loss | Arbitration Loss |

1.3.1125 CAN[0..0]_CSR_INT_EN

INT_EN

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_INT_EN: 0x4000A004

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---------|-----------|---------|----------|----------|------|---------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | NA | R |
| Name | form_err | ack_err | stuff_err | bit_err | ovr_load | arb_loss | | int_ebl |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------|----|----|--------|--------|-----------------|---------|---------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | rx_msg | tx_msg | rx_msg_los s | bus_off | crc_err |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

A particular interrupt source is enabled by setting its respective flag to 1

| Bits | Name | Description |
|------|-------------|-----------------------------------|
| 12 | rx_msg | Msg Recived |
| 11 | tx_msg | Tx Msg sent Interrupt |
| 10 | rx_msg_loss | Rx Msg Loss Interrupt Enable |
| 9 | bus_off | Busoff State Interrupt Enable |
| 8 | crc_err | CRC Error Interrupt Enable |
| 7 | form_err | Form Error Interrupt Enable |
| 6 | ack_err | Ack Error Interrupt Enable |
| 5 | stuff_err | Stuff Error Interrupt Enable |
| 4 | bit_err | Bit Error Interrupt Enable |
| 3 | ovr_load | Overload Interrupt Enable |
| 2 | arb_loss | Arbitration Loss Interrupt Enable |



0x4000a004

1.3.1125 CAN[0..0]_CSR_INT_EN (continued)

| | | |
|---|---------|------------------------------|
| 0 | int_ebl | Global Interrupt enable Flag |
|---|---------|------------------------------|

1.3.1126 CAN[0..0]_CSR_BUF_SR

BUF_SR

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_BUF_SR: 0x4000A008

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| SW Access:Reset | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | rx_msg7 | rx_msg6 | rx_msg5 | rx_msg4 | rx_msg3 | rx_msg2 | rx_msg1 | rx_msg0 |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|----------|----------|----------|----------|----------|----------|---------|---------|
| SW Access:Reset | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | rx_msg15 | rx_msg14 | rx_msg13 | rx_msg12 | rx_msg11 | rx_msg10 | rx_msg9 | rx_msg8 |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| SW Access:Reset | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 | R:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | tx_msg7 | tx_msg6 | tx_msg5 | tx_msg4 | tx_msg3 | tx_msg2 | tx_msg1 | tx_msg0 |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

These status indicators bundle the respective flags from all RxMessage and TxMessage buffers. Note All flags are read only. To acknowledge a MsgAv flag, the CPU must write to the respective RxMessage buffer.

| Bits | Name | Description |
|------|----------|----------------------------|
| 23 | tx_msg7 | Tx req Pending for Tx Msg7 |
| 22 | tx_msg6 | Tx req Pending for Tx Msg6 |
| 21 | tx_msg5 | Tx req Pending for Tx Msg5 |
| 20 | tx_msg4 | Tx req Pending for Tx Msg4 |
| 19 | tx_msg3 | Tx req Pending for Tx Msg3 |
| 18 | tx_msg2 | Tx req Pending for Tx Msg2 |
| 17 | tx_msg1 | Tx req Pending for Tx Msg1 |
| 16 | tx_msg0 | Tx req Pending for Tx Msg0 |
| 15 | rx_msg15 | Rx Msg15 Available |
| 14 | rx_msg14 | Rx Msg14 Available |
| 13 | rx_msg13 | Rx Msg13 Available |

1.3.1126 CAN[0..0]_CSR_BUF_SR (continued)

| | | |
|----|----------|--------------------|
| 12 | rx_msg12 | Rx Msg12 Available |
| 11 | rx_msg11 | Rx Msg11 Available |
| 10 | rx_msg10 | Rx Msg10 Available |
| 9 | rx_msg9 | Rx Msg9 Available |
| 8 | rx_msg8 | Rx Msg8 Available |
| 7 | rx_msg7 | Rx Msg7 Available |
| 6 | rx_msg6 | Rx Msg6 Available |
| 5 | rx_msg5 | Rx Msg5 Available |
| 4 | rx_msg4 | Rx Msg4 Available |
| 3 | rx_msg3 | Rx Msg3 Available |
| 2 | rx_msg2 | Rx Msg2 Available |
| 1 | rx_msg1 | Rx Msg1 Available |
| 0 | rx_msg0 | Rx Msg0 Available |

1.3.1127 CAN[0..0]_CSR_ERR_SR

ERR_SR

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_ERR_SR: 0x4000A00C

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | tx_err_cnt | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | rx_err_cnt | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:0000 | | | | R:0 | R:0 | R:00 | |
| HW Access | NA | | | | R/W | R/W | R/W | |
| Name | | | | | rxgte96 | txgte96 | err_state | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Status indicators are provided to report the CAN controller error state, receive error count, and transmit error count. Special flags report error counter values equal to or in excess of 96 errors are available to indicate heavily disturbed bus situations. The transmitter error counter according to the CAN standard. When it is greater than 255 Decimal, it is fixed at 255 Decimal.

| Bits | Name | Description |
|-------|-----------------|---|
| 19 | rxgte96 | Rx Error Count is greater or equal to 96 Decimal |
| 18 | txgte96 | Tx Error Count is greater or equal to 96 Decimal |
| 17:16 | err_state[1:0] | Error State of CAN node, 00 error active, 01 error passive, 1x bus off |
| 15:8 | rx_err_cnt[7:0] | Rx error Count. When in bus-off state,this counter is used to count 128 groups of 11 recessive bits |
| 7:0 | tx_err_cnt[7:0] | Tx error Count |

1.3.1128 CAN[0..0]_CSR_CMD

CMD

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_CMD: 0x4000A010

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|------|--------|----------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | NA:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | NA | R | R/W |
| Name | | | | | sram_test | | listen | run_stop |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The CAN can be used in different operating mode,by disabling transmitting data,it is possible to use the CAN in listen only mode,enabling feature such as automatic bit rate detection,SRAM Test Mode

| Bits | Name | Description |
|------|-----------|--|
| 3 | sram_test | SRAM test Mode. 0 Normal operation, 1 Enable SRAM test mode |
| 1 | listen | Listen only mode. 0 Active, 1 CAN listen only |
| 0 | run_stop | Run/Stop mode. 0 Sets the CAN controller to stop mode. Returns '1' when stopped, 1 Sets the CAN controller to run mode. Returns '1' when running |

1.3.1129 CAN[0..0]_CSR_CFG

CFG

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_CFG: 0x4000A014

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|----------|---------|---|---------------|-----------|
| SW Access:Reset | R/W:000 | | | R/W:0 | R/W:00 | | R/W:0 | R/W:0 |
| HW Access | R | | | R | R | | R | R |
| Name | cfg_tseg2 | | | auto_rst | cfg_sjw | | sampling_mode | edge_mode |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------|----|----|-------------|-----------|----|---|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0000 | | | |
| HW Access | NA | | | R | R | | | |
| Name | | | | cfg_arbiter | cfg_tseg1 | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | cfg_bitrate | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------|--------------|----|----|----|----|----|----|
| SW Access:Reset | NA:0 | R/W:00000000 | | | | | | |
| HW Access | NA | R | | | | | | |
| Name | | cfg_bitrate | | | | | | |

CAN module has to be configured prior to use, this register defines the effective CAN data rate, CAN data synchronization, message buffer arbitration

| Bits | Name | Description |
|-------|-------------------|---|
| 30:16 | cfg_bitrate[14:0] | CAN configuration Bit rate. 0 equals 1 clock cycle, 1 equals 2 clock cycles, ..., 32767 equals 32768 clock cycles |
| 12 | cfg_arbiter | Tx buffer Arbiter. 0 Round robin arbitration, 1 Fixed priority arbitration |
| 11:8 | cfg_tseg1[3:0] | Length of time segment1 |
| 7:5 | cfg_tseg2[2:0] | Length of time segment2 |
| 4 | auto_rst | auto_restart. 0 After bus-off, the CAN must be restarted 'by hand'. This is the recommended setting, 1 After bus-off, the CAN is restarting automatically after 128 groups of 11 recessive bits |
| 3:2 | cfg_sjw[1:0] | Synchronization Jump Width |
| 1 | sampling_mode | CAN bus Bit sampling. 0 One sampling point is used in the receiver path, 1 Three sampling points with majority decision are used |

1.3.1129 CAN[0..0]_CSR_CFG (continued)

| | | |
|---|-----------|--|
| 0 | edge_mode | CAN bus synchronization logic. 0 Edge from 'R' to 'D' is used for synchronization, 1 Both edges are used |
|---|-----------|--|

1.3.1130 CAN[0..0]_TX[0..7]_CMD

TXCMD

Reset: N/A

Register : Address

CAN0_TX0_CMD: 0x4000A020

CAN0_TX1_CMD: 0x4000A030

CAN0_TX2_CMD: 0x4000A040

CAN0_TX3_CMD: 0x4000A050

CAN0_TX4_CMD: 0x4000A060

CAN0_TX5_CMD: 0x4000A070

CAN0_TX6_CMD: 0x4000A080

CAN0_TX7_CMD: 0x4000A090

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------|-----------|---------|-------|
| SW Access:Reset | NA:0000 | | | | R:U | R:U | R:U | R:U |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | wpn1 | txint_ebl | txabort | txreq |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | RSVD0 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------|-------|-------|-------|----------|----|----|----|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:UUUU | | | |
| HW Access | R/W | R/W | R | R | R | | | |
| Name | wpn2 | RSVD1 | rtr | ide | dlc | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | RSVD2 | | | | | | | |

This is the Interrupt Enable bit. 0 interrupt disabled. 1 interrupt enables, successful message transmission sets the TxMsg flag in the Interrupt Controller.

| Bits | Name | Description |
|-------|------------------------------------|--|
| 31:24 | RSVD2[7:0] | Reserved bits. Since data read from these bits is from memory, the value at reset is undefined |
| 23 | Write Protect Bit (wpn2) {wpn2} | This Write Protect bit does not have a register within the RTL. It functions as a control input. Hence neither does it have a known reset value, nor can software read back a written value. The 0 or 1 Readback value for the bit comes as a Read to that register results in Memory data being sent out in that bit position, hence resulting in an unpredictable read value, completely independent of the written value. |
| 22 | RSVD1 | Reserved bits. Since data read from these bits is from memory, the value at reset is undefined |
| 21 | rtr | RTR Remote bit. 0 Standard message, 1 RTR message |
| 20 | ide | Extended identifier. 0 Standard format message, 1 Extended format message |

1.3.1130 CAN[0..0]_TX[0..7]_CMD (continued)

| | | |
|-------|------------|---|
| 19:16 | dlc[3:0] | Data Length of the Tx Msg. Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0 Message has 0 data byte, data[63:0] is not used, 1 Message has 1 data byte, data[63:56] is used, ..., 8 Message has 8 data bytes, data [63:0] is used, 9-15 Message has 8 data bytes |
| 15:8 | RSVD0[7:0] | Reserved bits. Since data read from these bits is from memory, the value at reset is undefined |
| 3 | wpn1 | WPN Write protect not Flag. 0 Bit[2] remains unchanged, 1 Bit[2] is modified, default. This bit is always zero for readback |
| 2 | txint_ebl | Transmit Interrupt Enable. 0 Interrupt disabled, 1 Interrupt enabled, succesful message transmission setst the TxMsg flag in the interrupt controller |
| 1 | txabort | Transmit Abort Request. 0 idle, 1 Requests removal of a pending message. The message is removed the next time an arbitration loss happened. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time |
| 0 | txreq | Transmit Request. For Write: 0 Idle, 1 Message Transmit request. For Read: 0 TxReq completed, 1 TxReq pending |

1.3.1131 CAN[0..0]_TX[0..7]_ID

TXID

Reset: N/A

Register : Address

CAN0_TX0_ID: 0x4000A024

CAN0_TX1_ID: 0x4000A034

CAN0_TX2_ID: 0x4000A044

CAN0_TX3_ID: 0x4000A054

CAN0_TX4_ID: 0x4000A064

CAN0_TX5_ID: 0x4000A074

CAN0_TX6_ID: 0x4000A084

CAN0_TX7_ID: 0x4000A094

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|--------|---|---|
| SW Access:Reset | R/W:UUUUU | | | | | NA:000 | | |
| HW Access | R | | | | | NA | | |
| Name | id | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

CAN Tx Msg Identifier

| Bits | Name | Description |
|------|----------|-------------------|
| 31:3 | id[28:0] | Tx Msg Identifier |

1.3.1132 CAN[0..0]_TX[0..7]_DH

TXDH

Reset: N/A

Register : Address

CAN0_TX0_DH: 0x4000A028

CAN0_TX1_DH: 0x4000A038

CAN0_TX2_DH: 0x4000A048

CAN0_TX3_DH: 0x4000A058

CAN0_TX4_DH: 0x4000A068

CAN0_TX5_DH: 0x4000A078

CAN0_TX6_DH: 0x4000A088

CAN0_TX7_DH: 0x4000A098

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_high | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_high | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_high | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_high | | | | | | | |

CAN Tx Msg Upper Data Bytes

| Bits | Name | Description |
|------|-----------------|------------------|
| 31:0 | data_high[31:0] | Upper Data Bytes |

1.3.1133 CAN[0..0]_TX[0..7]_DL

TXDL

Reset: N/A

Register : Address

CAN0_TX0_DL: 0x4000A02C

CAN0_TX1_DL: 0x4000A03C

CAN0_TX2_DL: 0x4000A04C

CAN0_TX3_DL: 0x4000A05C

CAN0_TX4_DL: 0x4000A06C

CAN0_TX5_DL: 0x4000A07C

CAN0_TX6_DL: 0x4000A08C

CAN0_TX7_DL: 0x4000A09C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_low | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_low | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_low | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_low | | | | | | | |

CAN Tx Msg Lower Data Bytes

| Bits | Name | Description |
|------|----------------|------------------|
| 31:0 | data_low[31:0] | Lower Data Bytes |

1.3.1134 CAN[0..0]_RX[0..15]_CMD

RXCMD

Reset: N/A

Register : Address

CAN0_RX0_CMD: 0x4000A0A0

CAN0_RX1_CMD: 0x4000A0C0

CAN0_RX2_CMD: 0x4000A0E0

CAN0_RX3_CMD: 0x4000A100

CAN0_RX4_CMD: 0x4000A120

CAN0_RX5_CMD: 0x4000A140

CAN0_RX6_CMD: 0x4000A160

CAN0_RX7_CMD: 0x4000A180

CAN0_RX8_CMD: 0x4000A1A0

CAN0_RX9_CMD: 0x4000A1C0

CAN0_RX10_CMD: 0x4000A1E0

CAN0_RX11_CMD: 0x4000A200

CAN0_RX12_CMD: 0x4000A220

CAN0_RX13_CMD: 0x4000A240

CAN0_RX14_CMD: 0x4000A260

CAN0_RX15_CMD: 0x4000A280

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|--------|------------|----------|---------|-----------|-------------|--------|
| SW Access:Reset | W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | R | R | R | R | R | R | R |
| Name | wpnl | lk_flg | rx_int_ebl | rtr_rply | buf_ebl | rtr_abort | rtr_rpy_pnd | msg_av |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | RSVD0 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------|-------|-------|-------|----------|----|----|----|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:UUUU | | | |
| HW Access | R/W | R/W | R | R | R | | | |
| Name | wpnh | RSVD1 | rtr | ide | dlc | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | RSVD2 | | | | | | | |

Rx Msg Control register have receive interrupt enable,buffer enable,link flag,identifier

| Bits | Name | Description |
|-------|------------------------------------|--|
| 31:24 | RSVD2[7:0] | Reserved bits. Since data read from these bits is from memory, the value at reset is undefined |
| 23 | Write Protect Bit (wpnh) {wpnh} | This Write Protect bit does not have a register within the RTL. It functions as a control input. Hence neither does it have a known reset value, nor can software read back a written value. The 0 or 1 Readback value for the bit comes as a Read to that register results in Memory data being sent out in that bit position, hence resulting in an unpredictable read value, completely independent of the written value. |

1.3.1134 CAN[0..0]_RX[0..15]_CMD (continued)

| | | |
|-------|-------------|--|
| 22 | RSVD1 | Reserved bits. Since data read from these bits is from memory, the value at reset is undefined |
| 21 | rtr | RTR Remote Bit. 0 This is a regular message, 1 This is an RTR message |
| 20 | ide | Extended Identifier Bit. 0 This is a standard format message, 1 This is an extended format message |
| 19:16 | dlc[3:0] | Data Length Code. 0 Message has 0 data bytes, data[63:0] is not valid, 1 Message has 1 data byte, data[63:56] is valid, ..., 8 Message has 8 data bytes, data [63:0] is valid, 9-15 Message has 8 data bytes |
| 15:8 | RSVD0[7:0] | Reserved bits. Since data read from these bits is from memory, the value at reset is undefined |
| 7 | wpnl | WPNL Write Protect Not Low flag. 0 Bits[6:3] remain unchanged, 1 Bits[6:3] are modified, default. The bit is always zero for readback |
| 6 | lk_flg | Link Flag used to link the Rx Buffer. 0 This buffer is not linked to the next, 1 This buffer is linked with the next buffer |
| 5 | rx_int_ebl | Receive Interrupt Enable. 0 Interrupt generation is disabled, 1 Interrupt generation is enabled |
| 4 | rtr_rply | Automatic RTR Message Handling. 0 Automatic RTR message handling disabled, 1 Automatic RTR message handling enabled |
| 3 | buf_ebl | Buffer Enable. 0 Buffer is disabled, 1 Buffer is enabled |
| 2 | rtr_abort | RTR Abort Request. 0 Idle, 1 Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. |
| 1 | rtr_rpy_pnd | RTR Reply request Pending. 0 No RTR reply request pending, 1 RTR reply request pending |
| 0 | msg_av | Message Available. For Read: 0 No new message available, 1 New message available. For Write: 0 Idle, 1 Acknowledges receipt of new message |

1.3.1135 CAN[0..0]_RX[0..15]_ID

RXID

Reset: N/A

Register : Address

CAN0_RX0_ID: 0x4000A0A4

CAN0_RX1_ID: 0x4000A0C4

CAN0_RX2_ID: 0x4000A0E4

CAN0_RX3_ID: 0x4000A104

CAN0_RX4_ID: 0x4000A124

CAN0_RX5_ID: 0x4000A144

CAN0_RX6_ID: 0x4000A164

CAN0_RX7_ID: 0x4000A184

CAN0_RX8_ID: 0x4000A1A4

CAN0_RX9_ID: 0x4000A1C4

CAN0_RX10_ID: 0x4000A1E4

CAN0_RX11_ID: 0x4000A204

CAN0_RX12_ID: 0x4000A224

CAN0_RX13_ID: 0x4000A244

CAN0_RX14_ID: 0x4000A264

CAN0_RX15_ID: 0x4000A284

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---------|---|---|
| SW Access:Reset | R/W:UUUUU | | | | | R/W:UUU | | |
| HW Access | R | | | | | R | | |
| Name | id | | | | | zeroes | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

The register contains Rx Msg Identifier

| Bits | Name | Description |
|------|-------------|-------------------|
| 31:3 | id[28:0] | Rx Msg Identifier |
| 2:0 | zeroes[2:0] | zeros |

1.3.1136 CAN[0..0]_RX[0..15]_DH

RXDH

Reset: N/A

Register : Address

CAN0_RX0_DH: 0x4000A0A8

CAN0_RX1_DH: 0x4000A0C8

CAN0_RX2_DH: 0x4000A0E8

CAN0_RX3_DH: 0x4000A108

CAN0_RX4_DH: 0x4000A128

CAN0_RX5_DH: 0x4000A148

CAN0_RX6_DH: 0x4000A168

CAN0_RX7_DH: 0x4000A188

CAN0_RX8_DH: 0x4000A1A8

CAN0_RX9_DH: 0x4000A1C8

CAN0_RX10_DH: 0x4000A1E8

CAN0_RX11_DH: 0x4000A208

CAN0_RX12_DH: 0x4000A228

CAN0_RX13_DH: 0x4000A248

CAN0_RX14_DH: 0x4000A268

CAN0_RX15_DH: 0x4000A288

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_high | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_high | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_high | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_high | | | | | | | |

The register contains the Upper Data Bytes

| Bits | Name | Description |
|------|-----------------|------------------|
| 31:0 | data_high[31:0] | Upper Data bytes |

1.3.1137 CAN[0..0]_RX[0..15]_DL

RXDL

Reset: N/A

Register : Address

| | |
|--------------------------|--------------------------|
| CAN0_RX0_DL: 0x4000A0AC | CAN0_RX1_DL: 0x4000A0CC |
| CAN0_RX2_DL: 0x4000A0EC | CAN0_RX3_DL: 0x4000A10C |
| CAN0_RX4_DL: 0x4000A12C | CAN0_RX5_DL: 0x4000A14C |
| CAN0_RX6_DL: 0x4000A16C | CAN0_RX7_DL: 0x4000A18C |
| CAN0_RX8_DL: 0x4000A1AC | CAN0_RX9_DL: 0x4000A1CC |
| CAN0_RX10_DL: 0x4000A1EC | CAN0_RX11_DL: 0x4000A20C |
| CAN0_RX12_DL: 0x4000A22C | CAN0_RX13_DL: 0x4000A24C |
| CAN0_RX14_DL: 0x4000A26C | CAN0_RX15_DL: 0x4000A28C |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data | | | | | | | |

The Register Contains the Lower data bytes

| Bits | Name | Description |
|------|------------|------------------|
| 31:0 | data[31:0] | Lower Data bytes |

1.3.1138 CAN[0..0]_RX[0..15]_AMR

RXAMR

Reset: N/A

Register : Address

CAN0_RX0_AMR: 0x4000A0B0

CAN0_RX1_AMR: 0x4000A0D0

CAN0_RX2_AMR: 0x4000A0F0

CAN0_RX3_AMR: 0x4000A110

CAN0_RX4_AMR: 0x4000A130

CAN0_RX5_AMR: 0x4000A150

CAN0_RX6_AMR: 0x4000A170

CAN0_RX7_AMR: 0x4000A190

CAN0_RX8_AMR: 0x4000A1B0

CAN0_RX9_AMR: 0x4000A1D0

CAN0_RX10_AMR: 0x4000A1F0

CAN0_RX11_AMR: 0x4000A210

CAN0_RX12_AMR: 0x4000A230

CAN0_RX13_AMR: 0x4000A250

CAN0_RX14_AMR: 0x4000A270

CAN0_RX15_AMR: 0x4000A290

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|-------|-------|------|
| SW Access:Reset | R/W:UUUUU | | | | | R/W:U | R/W:U | NA:0 |
| HW Access | R | | | | | R | R | NA |
| Name | id | | | | | ide | rtr | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

The Register contains the Acceptance mask value

| Bits | Name | Description |
|------|----------|---------------------|
| 31:3 | id[28:0] | Identifier |
| 2 | ide | Extended Identifier |
| 1 | rtr | RTR Bit |

1.3.1139 CAN[0..0]_RX[0..15]_ACR

RXACR

Reset: N/A

Register : Address

CAN0_RX0_ACR: 0x4000A0B4

CAN0_RX1_ACR: 0x4000A0D4

CAN0_RX2_ACR: 0x4000A0F4

CAN0_RX3_ACR: 0x4000A114

CAN0_RX4_ACR: 0x4000A134

CAN0_RX5_ACR: 0x4000A154

CAN0_RX6_ACR: 0x4000A174

CAN0_RX7_ACR: 0x4000A194

CAN0_RX8_ACR: 0x4000A1B4

CAN0_RX9_ACR: 0x4000A1D4

CAN0_RX10_ACR: 0x4000A1F4

CAN0_RX11_ACR: 0x4000A214

CAN0_RX12_ACR: 0x4000A234

CAN0_RX13_ACR: 0x4000A254

CAN0_RX14_ACR: 0x4000A274

CAN0_RX15_ACR: 0x4000A294

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|-------|-------|------|
| SW Access:Reset | R/W:UUUUU | | | | | R/W:U | R/W:U | NA:0 |
| HW Access | R | | | | | R | R | NA |
| Name | id | | | | | ide | rtr | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | id | | | | | | | |

The Register contains the Acceptance Code value

| Bits | Name | Description |
|------|----------|---------------------|
| 31:3 | id[28:0] | Identifier |
| 2 | ide | Extended Identifier |
| 1 | rtr | RTR Bit |

1.3.1140 CAN[0..0]_RX[0..15]_AMRD

RXAMRD

Reset: N/A

Register : Address

CAN0_RX0_AMRD: 0x4000A0B8

CAN0_RX1_AMRD: 0x4000A0D8

CAN0_RX2_AMRD: 0x4000A0F8

CAN0_RX3_AMRD: 0x4000A118

CAN0_RX4_AMRD: 0x4000A138

CAN0_RX5_AMRD: 0x4000A158

CAN0_RX6_AMRD: 0x4000A178

CAN0_RX7_AMRD: 0x4000A198

CAN0_RX8_AMRD: 0x4000A1B8

CAN0_RX9_AMRD: 0x4000A1D8

CAN0_RX10_AMRD: 0x4000A1F8

CAN0_RX11_AMRD: 0x4000A218

CAN0_RX12_AMRD: 0x4000A238

CAN0_RX13_AMRD: 0x4000A258

CAN0_RX14_AMRD: 0x4000A278

CAN0_RX15_AMRD: 0x4000A298

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_lsb | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_lsb | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The register contains the Acceptance mask data

| Bits | Name | Description |
|------|----------------|-----------------------|
| 15:0 | data_lsb[15:0] | Upper 2 Bytes of Data |

1.3.1141 CAN[0..0]_RX[0..15]_ACRD

RXACRD

Reset: N/A

Register : Address

CAN0_RX0_ACRD: 0x4000A0BC

CAN0_RX1_ACRD: 0x4000A0DC

CAN0_RX2_ACRD: 0x4000A0FC

CAN0_RX3_ACRD: 0x4000A11C

CAN0_RX4_ACRD: 0x4000A13C

CAN0_RX5_ACRD: 0x4000A15C

CAN0_RX6_ACRD: 0x4000A17C

CAN0_RX7_ACRD: 0x4000A19C

CAN0_RX8_ACRD: 0x4000A1BC

CAN0_RX9_ACRD: 0x4000A1DC

CAN0_RX10_ACRD: 0x4000A1FC

CAN0_RX11_ACRD: 0x4000A21C

CAN0_RX12_ACRD: 0x4000A23C

CAN0_RX13_ACRD: 0x4000A25C

CAN0_RX14_ACRD: 0x4000A27C

CAN0_RX15_ACRD: 0x4000A29C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_lsb | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_lsb | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The register contains the Acceptance code data

| Bits | Name | Description |
|------|----------------|-----------------------|
| 15:0 | data_lsb[15:0] | Upper 2 Bytes of Data |

1.3.1142 DFB[0..0]_DPA_SRAM_DATA[0..127]

Data RAM A

Reset: N/A

Register : Address

DFB_DPA_SRAM_DATA: 0x4000C000-0x4000C1FF

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Data Storage SRAM

| Bits | Name | Description |
|------|----------------|------------------|
| 23:0 | sramdata[23:0] | (no description) |

1.3.1143 DFB[0..0]_DPB_SRAM_DATA[0..127]

DFB Data RAM B

Reset: N/A

Register : Address

DFB_DPB_SRAM_DATA: 0x4000C200-0x4000C3FF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Data Storage SRAM

| Bits | Name | Description |
|------|----------------|------------------|
| 23:0 | sramdata[23:0] | (no description) |

1.3.1144 DFB[0..0]_CSA_SRAM_DATA[0..63]

DFB Control Store A

Reset: N/A

Register : Address

DFB_CSA_SRAM_DATA: 0x4000C400-0x4000C4FF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

Control Storage SRAM

| Bits | Name | Description |
|------|----------------|------------------|
| 31:0 | sramdata[31:0] | (no description) |

1.3.1145 DFB[0..0]_CSB_SRAM_DATA[0..63]

DFB Control Store B

Reset: N/A

Register : Address

DFB_CSBSRAM_DATA: 0x4000C500-0x4000C5FF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

Control Storage SRAM

| Bits | Name | Description |
|------|----------------|------------------|
| 31:0 | sramdata[31:0] | (no description) |

1.3.1146 DFB[0..0]_FSM_SRAM_DATA[0..63]

DFB Code Store B

Reset: N/A

Register : Address

DFB_FSM_SRAM_DATA: 0x4000C600-0x4000C6FF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

Code Storage SRAM

| Bits | Name | Description |
|------|----------------|------------------|
| 31:0 | sramdata[31:0] | (no description) |

1.3.1147 DFB[0..0]_ACU_SRAM_DATA[0..15]

DFB Address Store

Reset: N/A

Register : Address

DFB_ACU_SRAM_DATA: 0x4000C700-0x4000C73F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | sramdata | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------|----|----|----|---|---|
| SW Access:Reset | NA:00 | | R/W:UUUUUU | | | | | |
| HW Access | NA | | R/W | | | | | |
| Name | | | sramdata | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Address Storage SRAM

| Bits | Name | Description |
|------|----------------|------------------|
| 13:0 | sramdata[13:0] | (no description) |

1.3.1148 DFB[0..0]_CR

DFB Command Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_CR: 0x4000C780

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|-----------------|-------|-------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | CORECLK_DISABLE | ADDR6 | RUN |

This register enables/disables DFB operation and sets FSM memory bank. Also, the internal core clock gater is controlled. A read of this register produces the last value written to this register.

| Bits | Name | Description |
|------|-----------------|---|
| 2 | CORECLK_DISABLE | This bit when set high disables (gates off) the clock to the entire core of the block. This includes all FFs except those used for the AHB interface and CSRs and all 6 RAMs. When disabled (set high) the AHB interface to the CSR is still fully functional. This bit is ANDed with the primary input signal <code>dfb_clk_en</code> to control the clock gate. <code>dfb_clk_en</code> must be high and <code>CoreCLK_Disable</code> must be low for the clock to run. See Table 1-734. |
| 1 | ADDR6 | This bit is literally address bit 5 (6th bit) of the FSM RAM when addressed by the DFB Controller. It has no affect on the FSM RAM when addressed on the AHB interface. It controls the Banking feature of the FSM. See Table 1-733. |
| 0 | RUN | Setting this bit to 1 enables the DFB to run. Setting it to 0 forces the next state address of the FSM to zero of the active Bank, reinitializes the ACU's and PC's and clears the round flag, saturation flag, saturation detect flag and all 6 extended Enables in the Controller. See Table 1-735. |

Table 1-733. Bit field encoding: `addr6_enum`

| Value | Name | Description |
|-------|------------|---------------|
| 1'b1 | ADDR6_HIGH | ADDR6 is High |
| 1'b0 | ADDR6_LOW | ADDR6 is Low |

Table 1-734. Bit field encoding: `coreclk_disable_enum`

| Value | Name | Description |
|-------|--------------------|--------------------------------------|
| 1'b1 | CORECLK_DISABLE_HI | Core Clock is Disabled (gated) GH |
| 1'b0 | CORECLK_DISABLE_L | Core Clock is Enabled OW |

Table 1-735. Bit field encoding: `run_bit_enum`

| Value | Name | Description |
|-------|---------|----------------------------|
| 1'b1 | RUN_EN | DFB is enabled to operate. |
| 1'b0 | RUN_DIS | DFB operation is halted. |

1.3.1149 DFB[0..0]_SR

DFB Status Register

Reset: Reset Signals Listed Below

Register : Address

DFB0_SR: 0x4000C784

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---------------|---------------|----------------|----------------|--------------|----------|---------|
| SW Access:Reset | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R:U | R:U | R:U |
| HW Access | W | W | W | W | W | W | W | W |
| Name | INTR_SEM 2 | INTR_SEM 1 | INTR_SEM 0 | INTR_HOL DB | INTR_HOL DA | RND_MOD E | SAT_MODE | RAM_SEL |

This register contains 5 bits indicating the status of block generated interrupts and 3 bits of status from the Datapath unit. Of the 5 sources of interrupts, only those configured in INT_CTRL are activated. If not activated in INT_CTRL they will never assert in this register. If an interrupt source bit (7:3) is set this indicates it is at least one of the sources of the currently driven interrupt on dfb_intr. More than one of the 5 could be asserted. Note that if the system SW wishes to poll for an event and not have an interrupt generated, the interrupt must be enabled in the INT_CTRL register so that it can be polled here and then disable the interrupt in the Interrupt Controller or not connect the dfb_intr signal to the Interrupt Controller at all by not configuring the DSI path. Bits 2:0 are read-only - writes to these bits have no affect. Writes to bits 7:3 of '1' clear the bit, writes of 0 have no affect.

| Bits | Name | Description |
|------|-------------|---|
| 7 | INTR_SEM2 | If this bit is high, semaphore register bit 2 is a source of the current interrupt. Write a '1' to this bit to clear it. See Table 1-740. |
| 6 | INTR_SEM1 | If this bit is high, semaphore register bit 1 is a source of the current interrupt. Write a '1' to this bit to clear it. See Table 1-739. |
| 5 | INTR_SEM0 | If this bit is high, semaphore register bit 0 is a source of the current interrupt. Write a '1' to this bit to clear it. See Table 1-738. |
| 4 | INTR_HOLDDB | If this bit is high, Holding register B is a source of the current interrupt. Write a '1' to this bit to clear it. Reading the Holding register B also clears this bit. See Table 1-737. |
| 3 | INTR_HOLDDA | If this bit is high, Holding register A is a source of the current interrupt. Write a '1' to this bit to clear it. Reading the Holding register A also clears this bit. See Table 1-736. |
| 2 | RND_MODE | Indicates that the DP is in Round mode - meaning that any result passing out of the DP unit is being rounded to a 16-bit value. See Table 1-742. |

1.3.1149 DFB[0..0]_SR (continued)

| | | |
|---|----------|---|
| 1 | SAT_MODE | Indicates that the DP unit is in Saturation mode - meaning that any mathematic operation executed that produces a number outside the range of a 24-bit 2's compliment number is clamped to the mode positive or negative number allowed. Saturation mode is set/unset under Assembly control in the DFB Controller. See Table 1-743. |
| 0 | RAM_SEL | This bit indicates which Control Store memory is in use, RAM A or RAM B. See Table 1-741. |

Reset Table

| resetsignal | field(s) |
|---|---|
| N/A | RAM_SEL, SAT_MODE, RND_MODE |
| Domain reset for non-retention flops [reset_all_nonretention] | INTR_HOLD_A, INTR_HOLD_B, INTR_SEM0, INTR_SEM1, INTR_SEM2 |

Table 1-736. Bit field encoding: intr_holda_enum

| Value | Name | Description |
|-------|-----------|--|
| 1'b0 | HOLDA_OFF | Indicates no pending Holding A Register Interrupt. |
| 1'b1 | HOLDA_ON | Indicates a pending Holding A Register Interrupt. |

Table 1-737. Bit field encoding: intr_holdb_enum

| Value | Name | Description |
|-------|-----------|--|
| 1'b0 | HOLDB_OFF | Indicates no pending Holding B Register Interrupt. |
| 1'b1 | HOLDB_ON | Indicates a pending Holding B Register Interrupt. |

Table 1-738. Bit field encoding: intr_sem0_enum

| Value | Name | Description |
|-------|----------|---|
| 1'b0 | SEM0_OFF | Indicates no pending Semaphore 0 Interrupt. |
| 1'b1 | SEM0_ON | Indicates a pending Semaphore 0 Interrupt. |

Table 1-739. Bit field encoding: intr_sem1_enum

| Value | Name | Description |
|-------|----------|---|
| 1'b0 | SEM1_OFF | Indicates no pending Semaphore 1 Interrupt. |
| 1'b1 | SEM1_ON | Indicates a pending Semaphore 1 Interrupt. |

Table 1-740. Bit field encoding: intr_sem2_enum

| Value | Name | Description |
|-------|----------|---|
| 1'b0 | SEM2_OFF | Indicates no pending Semaphore 2 Interrupt. |
| 1'b1 | SEM2_ON | Indicates a pending Semaphore 2 Interrupt. |

Table 1-741. Bit field encoding: ram_select_bit_enum

| Value | Name | Description |
|-------|-------------|-----------------------------------|
| 1'b0 | RAMSEL_LOW | Control Store memory A is in use. |
| 1'b1 | RAMSEL_HIGH | Control Store memory B is in use. |

Table 1-742. Bit field encoding: rnd_mode_enum

| Value | Name | Description |
|-------|---------|------------------------------|
| 1'b0 | RND_OFF | Indicates Round Mode is off. |
| 1'b1 | RND_ON | Indicates Round Mode is on. |

1.3.1149 DFB[0..0]_SR (continued)

Table 1-743. Bit field encoding: sat_mode_enum

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | SAT_OFF | Indicates Saturation mode is off. |
| 1'b1 | SAT_ON | Indicates Saturation mode is on. |

1.3.1150 DFB[0..0]_RAM_EN

DFB RAM Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_RAM_EN: 0x4000C788

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|--------|--------|--------|--------|--------|--------|
| SW Access:Reset | R/W:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | | R | R | R | R | R | R |
| Name | RAMWR_ADDRING | | DPB_EN | DPA_EN | ACU_EN | CSB_EN | CSA_EN | FSM_EN |

This register controls the DFB memory enables. These bits are tied directly to the enable pins of the RAMs in this block and should be used by System SW to power-down RAMs not in use. A read of this register produces the last value written to this register. The high two bits control the RAM overlay addressing.

| Bits | Name | Description |
|------|--------------------|--|
| 7:6 | RAMWR_ADDRING[1:0] | These two bits control the write addressing of the 4 largest RAMs embedded in the DFB (CS-A, CS-B, Data-A, Data-B). The setting of these bits allows overlaid writes to occur to these memories when it is desired to fill them with like data. This feature is primarily intended to enhance SW BIST test time but may also have functional uses as well like filling both CS RAMs concurrently as they typically hold identical data. Setting these bits to 01, for example, configures the HW to write to both CS-A and CS-B for any write to the address space of either CS-A or CS-B. Reads are not affected by these bits. See Table 1-745. |
| 5 | DPB_EN | Datapath RAM B RAM enable / disable. See Table 1-744. |
| 4 | DPA_EN | Datapath RAM A RAM enable / disable. See Table 1-744. |
| 3 | ACU_EN | ACU RAM RAM enable / disable. See Table 1-744. |
| 2 | CSB_EN | Control Store RAM B RAM enable / disable. See Table 1-744. |
| 1 | CSA_EN | Control Store RAM A RAM enable / disable. See Table 1-744. |
| 0 | FSM_EN | FSM RAM RAM enable / disable. See Table 1-744. |

Table 1-744. Bit field encoding: ram_enable_bit_enum

| Value | Name | Description |
|-------|---------|------------------|
| 1'b1 | RAM_EN | RAM is enabled. |
| 1'b0 | RAM_DIS | RAM is disabled. |

Table 1-745. Bit field encoding: ram_write_addressing_bits_enum

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1150 DFB[0..0]_RAM_EN (continued)

Table 1-745. Bit field encoding: ram_write_addressing_bits_enum

| | | |
|-------|-------------------|---|
| 2'b00 | NO_OVERLAY | No overlay mapping. |
| 2'b11 | OVERLAY_CS_A_CS_B | Overlay CS A with CS B. |
| 2'b10 | OVERLAY_DATA_A_DA | Overlay Data A with Data B. |
| | TA_B | |
| 2'b11 | OVERLAY_CS_AB_DAT | Overlay CS A/B with Data A with DATA B. |
| | A_AB | |

1.3.1151 DFB[0..0]_RAM_DIR

DFB RAM Direction Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_RAM_DIR: 0x4000C78C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------|---------|---------|---------|---------|---------|---------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 | R/W:1 |
| HW Access | NA | R | R | R | R | R | R | R |
| Name | | SNP_DABLE | DPB_DIR | DPA_DIR | ACU_DIR | CSB_DIR | CSA_DIR | FSM_DIR |

This register controls the DFB memory direction. These bits control if each RAM of this block is embedded to the DFB function or mapped in the system address space on the AHB bus. Mapping to the bus facilitates SW BIST, Configuration filling, and Block Mode transfers. A read to this register returns what was last written. When programming code into the CSA/B and FSM RAMs the RAM_DIR bits should be set and unset together. When in normal operating mode and the CSA/B, ACU and FSM are being filled with assembly code/data, it is high recommended that all four RAMs DIR bits be set and cleared together.

| Bits | Name | Description |
|------|-----------|---|
| 6 | SNP_DABLE | The CS and DP RAMs (optionally the FSM) have address snooping logic that watches for redundant back-to-back RD cycles and disables the RAM to conserve power. Writing a 1 to this bit disables this logic for all RAMs. See Table 1-747. |
| 5 | DPB_DIR | Datapath RAM B RAM Direction. See Table 1-746. |
| 4 | DPA_DIR | Datapath RAM A RAM Direction. See Table 1-746. |
| 3 | ACU_DIR | ACU RAM RAM Direction. See Table 1-746. |
| 2 | CSB_DIR | Control Store RAM B RAM Direction. See Table 1-746. |
| 1 | CSA_DIR | Control Store RAM A RAM Direction. See Table 1-746. |
| 0 | FSM_DIR | FSM RAM RAM Direction. See Table 1-746. |

Table 1-746. Bit field encoding: ram_direction_bit_enum

| Value | Name | Description |
|-------|---------|-------------|
| 1'b1 | RAM_AHB | System Bus |
| 1'b0 | RAM_DFB | DFB |

Table 1-747. Bit field encoding: snoop_disable_bit_enum

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1151 DFB[0..0]_RAM_DIR (continued)

Table 1-747. Bit field encoding: snoop_disable_bit_enum

| | | |
|------|-------------|----------|
| 1'b1 | SNP_DISABLE | Disabled |
| 1'b0 | SNP_ENABLE | Enabled |

1.3.1152 DFB[0..0]_SEMA

DFB Semaphore Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_SEMA: 0x4000C790

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------|---|---|------|---------|---|---|
| SW Access:Reset | NA:0 | W:000 | | | NA:0 | R/W:000 | | |
| HW Access | NA | R | | | NA | R | | |
| Name | | SEMA_MASK | | | | SEMA | | |

This register controls the DFB Semaphore register. These bits are used to pass semaphores between the DFB Controller and the System SW. Their use and purpose is user defined. A read to this register returns what was last written by either System SW or the DFB Controller.

| Bits | Name | Description |
|------|----------------|---|
| 6:4 | SEMA_MASK[2:0] | These bits are used to mask writes to bits 2-0. They are write-only. If bit 4 is a 1 then the value on bit 0 will be written to SEM0, otherwise SEM0 will not be altered. Likewise for MASK1 and SEM1, and MASK2 and SEM2. |
| 2:0 | SEMA[2:0] | These bits are used to pass semaphores between the DFB Controller and the System SW. Their definition is user defined. There is no HW implementing an arbitration methodology should both the System and Control access the same SEM bit at the same time. Coherency of the SEM bits is the responsibility of the SW running on the Controller and the System CPU. If the same SEM bit is written by the Controller and the System in the exact same cycle (a collision), the System write takes precedence over the Controller. In this manner, each of the 3 bits are treated individually. |

1.3.1153 DFB[0..0]_DSI_CTRL

DFB Global Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_DSI_CTRL: 0x4000C794

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|----------|---|
| SW Access:Reset | NA:0000 | | | | R/W:00 | | R/W:00 | |
| HW Access | NA | | | | R | | R | |
| Name | | | | | GBL2_OUT | | GBL1_OUT | |

This register controls what internal signals are mapped to the two primary output global signals `dfb_globalo1` and `dfb_globalo2`. A read of this register produces the last value written to this register. These two outputs are registered (pclk rising) just before leaving the block - giving them a 1 cycle delay and a full clock cycle to propagate to their DSI destinations.

| Bits | Name | Description |
|------|---------------|--|
| 3:2 | GBL2_OUT[1:0] | These bits are used to control what internal signals are mapped to the primary output signal <code>dfb_globalo2</code> . See Table 1-749. |
| 1:0 | GBL1_OUT[1:0] | These bits are used to control what internal signals are mapped to the primary output signal <code>dfb_globalo1</code> . See Table 1-748. |

Table 1-748. Bit field encoding: `global_output_1_encoding_bits_enum`

| Value | Name | Description |
|-------|----------|--|
| 2'b00 | DFB_RUN | DFB RUN Bit. This is the same bit as the RUN bit in the DFB0_CR register. |
| 2'b01 | SEM0 | Semaphore Bit 0. This is the same signal described in the DFB0_SEMA CSR. |
| 2'b10 | SEM1 | Semaphore Bit 1. This is the same signal described in the DFB0_SEMA CSR. |
| 2'b11 | DFB_INTR | DFB Interrupt. This is the same signal as the primary <code>dfb_intr</code> output signal. |

Table 1-749. Bit field encoding: `global_output_2_encoding_bits_enum`

| Value | Name | Description |
|-------|-----------|---|
| 2'b00 | SEM2 | Semaphore Bit 2. This is the same signal described in the DFB0_SEMA CSR. |
| 2'b01 | DPSIGN | Datapath Sign. This signal asserts anytime the output of the ALU in the Datapath unit is negative. It will remain high for each cycle this condition is true. |
| 2'b10 | DPTHREASH | Datapath Threshold Crossed. This signal asserts anytime the threshold of 0 is crossed in the ALU when one of the following instructions is executing: TDECA, TSUBA, TSUBB, TADDABSA, TADDABSB. It will remain high for each cycle this condition is true. |
| 2'b11 | DPEQ | Datapath ALU=0. This signal asserts high when the output of the ALU in the Datapath unit equals 0 and one of the following ALU commands is executing: TDECA, TSUBA, TSUBB, TADDABSA, TADDABSB. It will remain high for each cycle this condition is true. |

1.3.1154 DFB[0..0]_INT_CTRL

DFB Interrupt Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_INT_CTRL: 0x4000C798

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|----------|----------|----------|----------|----------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | SEMA2_EN | SEMA1_EN | SEMA0_EN | HOLDB_EN | HOLDA_EN |

This register allows control of what events generate an interrupt. Each of the events enabled by the bits in this register are ORed together to produce the `dfb_intr` signal. A read to this register returns what was last written. System SW should see that a semaphore is never configured as both a DMA request and an interrupt (see `DMA_CTRL`).

| Bits | Name | Description |
|------|----------|--|
| 4 | SEMA2_EN | If this bit is set high, an interrupt is generated each time a 1 is written into the semaphore register bit 2. See Table 1-751. |
| 3 | SEMA1_EN | If this bit is set high, an interrupt is generated each time a 1 is written into the semaphore register bit 1. See Table 1-751. |
| 2 | SEMA0_EN | If this bit is set high, an interrupt is generated each time a 1 is written into the semaphore register bit 0. See Table 1-751. |
| 1 | HOLDB_EN | If this bit is set high, an interrupt is generated each time new valid data is written into the output Holding register B. See Table 1-750. |
| 0 | HOLDA_EN | If this bit is set high, an interrupt is generated each time new valid data is written into the output Holding register A. See Table 1-750. |

Table 1-750. Bit field encoding: `enable_holding_reg_bit_enum`

| Value | Name | Description |
|-------|------------------------|--|
| 1'b1 | ENABLE_HOLDING_IRQ_EN | Interrupt is generated each time new valid data is written into the output Holding register. |
| 1'b0 | ENABLE_HOLDING_IRQ_DIS | Holding register interrupt masked. |

Table 1-751. Bit field encoding: `enable_semaphore_bit_enum`

| Value | Name | Description |
|-------|--------------------------|--|
| 1'b1 | ENABLE_SEMAPHORE_IRQ_EN | Interrupt is generated each time a 1 is written to the semaphore register. |
| 1'b0 | ENABLE_SEMAPHORE_IRQ_DIS | Semaphore register interrupt masked. |

1.3.1155 DFB[0..0]_DMA_CTRL

DFB DMAREQ Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_DMA_CTRL: 0x4000C79C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---|---------|---|
| SW Access:Reset | NA:0000 | | | | R/W:00 | | R/W:00 | |
| HW Access | NA | | | | R | | R | |
| Name | | | | | DMAREQ2 | | DMAREQ1 | |

This register allows control of what events generate DMAREQ events. Each field allows the user to configure what event drives each of the two DMAREQ primary output signals. Note that if a semaphore is configured as the DMAREQ the HW automatically clears the appropriate semaphore register after one pclk cycle - creating a single cycle pulse on the dmareq output as is required. Otherwise, the semaphores are sticky. If a Holding register is programmed as a DMAREQ, the DMAREQ is level sensed, instead of a pulse. The DMAREQ in this case will stay asserted until the Holding register is read. Level sensed is the preferred method of PHUB even though a strobe will work. System SW should see that a semaphore is never configured as both a DMA request and an interrupt (see INT_CTRL). A read of this register returns the last value written.

| Bits | Name | Description |
|------|--------------|--|
| 3:2 | DMAREQ2[1:0] | The value in these two bits selects which event drives dma_req2. See Table 1-753. |
| 1:0 | DMAREQ1[1:0] | The value in these two bits selects which event drives dma_req1. See Table 1-752. |

Table 1-752. Bit field encoding: dma_req_1_source_bits_enum

| Value | Name | Description |
|-------|------------------|---------------------------------|
| 2'b00 | DMAREQ1_DISABLED | Disabled |
| 2'b01 | DMAREQ1_HOLDING_ | New data in Holding Register A. |
| | REG_A | |
| 2'b10 | DMAREQ1_SEMAPHO | Semaphore 0. |
| | RE_0 | |
| 2'b11 | DMAREQ1_SEMAPHO | Semaphore 1. |
| | RE_1 | |

Table 1-753. Bit field encoding: dma_req_2_source_bits_enum

| Value | Name | Description |
|-------|------------------|---------------------------------|
| 2'b00 | DMAREQ2_DISABLED | Disabled |
| 2'b01 | DMAREQ2_HOLDING_ | New data in Holding Register B. |
| | REG_B | |
| 2'b10 | DMAREQ2_SEMAPHO | Semaphore 0. |
| | RE_0 | |
| 2'b11 | DMAREQ2_SEMAPHO | Semaphore 1. |
| | RE_1 | |

1.3.1156 DFB[0..0]_STAGEA

DFB Low Byte Staging Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEA: 0x4000C7A0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | STGA_LOW | | | | | | | |

This is the low byte of the Streaming input Staging Register - Port A. If the Staging A Data Alignment bit is set in the DALIGN register then data written to this address will be written into bits 15:8 instead. Although the Staging A/B registers are shown here as 3 byte-wide registers, it is primarily intended that they be treated as 24-bit registers at a 32-bit offset. Due to the architecture of the DFB, any value written to the Staging A or B registers that is less than 24 bits in size must be msb aligned. For example, a 16-bit value written to the Staging A register must be written to STAGExM and STAGExH with STAGEx set to 0. The Staging registers support byte and half-word accesses as well. However, if byte and half-word accesses are used then the Key Coherency Byte feature must be used. Also see the COHER register description below. In some use models it is desirable to write 16-bit values on bus bits 15:0 and have them actually writing to bits 23:8 of the register. A System SW convenience feature to accomplish this is provided. If the Data Alignment bit for these registers is set in the DALIGN register the byte written is shifted up (left) to the next byte position. This is only true of the two lower bytes. READ: AHB: What was last written. The DFB Controller reads this register (and the other 2 bytes) by asserting busrd and setting the low-order ACU RAM address bit low. WRITE: Writes the low byte of the input Staging Register for Port A or the middle byte if the Data Alignment bit is set in the DALIGN register.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | STGA_LOW[7:0] | A write to this register sets the low byte of the input Staging Register for Port A. |

1.3.1157 DFB[0..0]_STAGEAM

DFB Middle Byte Staging Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEAM: 0x4000C7A1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | STGA_MID | | | | | | | |

This is the middle byte of the Streaming input Staging Register - Port A. If the Staging A Data Alignment bit is set in the DALIGN register then data written to this address will be written into bits 23:16 instead. See usage notes in STAGEA register description above.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | STGA_MID[7:0] | A write to this register sets the middle byte of the input Staging Register for Port A. |

1.3.1158 DFB[0..0]_STAGEAH

DFB High Byte Staging Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEAH: 0x4000C7A2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | STGA_HIGH | | | | | | | |

This is the high byte of the Streaming input Staging Register - Port A. See usage notes in STAGEA register description above.

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | STGA_HIGH[7:0] | A write to this register sets the high byte of the input Staging Register for Port A. |

1.3.1159 DFB[0..0]_STAGEB

DFB Low Byte Staging Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEB: 0x4000C7A4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | STGB_LOW | | | | | | | |

This is the low byte of the Streaming input Staging Register - Port B. If the Staging B Data Alignment bit is set in the DALIGN register then data written to this address will be written into bits 15:8 instead. See usage notes in STAGEA register description above.

| Bits | Name | Description |
|------|---------------|--|
| 7:0 | STGB_LOW[7:0] | A write to this register sets the low byte of the input Staging Register for Port B. |

1.3.1160 DFB[0..0]_STAGEBM

DFB Middle Byte Staging Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEBM: 0x4000C7A5

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | STGB_MID | | | | | | | |

This is the middle byte of the Streaming input Staging Register - Port B. If the Staging B Data Alignment bit is set in the DALIGN register then data written to this address will be written into bits 23:16 instead. See usage notes in STAGEA register description above.

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | STGB_MID[7:0] | A write to this register sets the middle byte of the input Staging Register for Port B. |

1.3.1161 DFB[0..0]_STAGEBH

DFB High Byte Staging Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEBH: 0x4000C7A6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | STGB_HIGH | | | | | | | |

This is the high byte of the Streaming input Staging Register - Port B. See usage notes in STAGEA register description above.

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | STGB_HIGH[7:0] | A write to this register sets the high byte of the input Staging Register for Port B. |

1.3.1162 DFB[0..0]_HOLDA

DFB Low Byte Holding Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDA: 0x4000C7A8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | HOLDA_LOW | | | | | | | |

This is the low byte of the output Holding Register - Port A. If the Holding A Data Alignment bit is set in the DALIGN register then data read from this address will be bits 15:8 instead. Although the Holding A/B registers are shown here as 3 byte-wide registers, it is primarily intended that they be treated as 24-bit registers at a 32-bit offset. Due to the architecture of the DFB, any value read from the Holding A or B registers will be msb aligned unless shifted otherwise by the Datapath shifter. For example, if the resultant output samples are 16-bit values, a read of a Holding register will produce that data on bits 23:8, or HOLDxH and HOLDxM. The Holding registers support byte and half-word accesses as well. However, if byte and half-word accesses are used then the Key Coherency Byte feature must be used. Also see the COHER register description below. In some use models it is desirable to read 16-bit values on bus bits 15:0 and have them actually source from bits 23:8 of the register. A System SW convenience feature to accomplish this is provided. If the Data Alignment bit for these registers is set in the DALIGN register the byte read is shifted down (right) to the next byte position. This is only true of the two upper bytes. Also as a System SW convenience, reads of the Holding registers are sign extended up to bit 31 of the bus even though the top byte is not documented or implemented as a real register. If the DFB is configured (see INT_CTRL) to generate an interrupt based on valid data in the Holding register, the interrupt status bit in the SR register will be cleared when any portion (byte, 16-bit or full 32-bit read) of the Holding register is read, by the CPU or the DMA Controller. READ: What was last written by the DFB Controller. WRITE: Read-only by AHB, DFB Controller writes to this register (including the other 2 bytes) with a buswr command and the low-order ACU RAM address bit set low.

| Bits | Name | Description |
|------|----------------|--|
| 7:0 | HOLDA_LOW[7:0] | Low byte of the output Holding Register, Port A. |

1.3.1163 DFB[0..0]_HOLDAM

DFB Middle Byte Holding Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDAM: 0x4000C7A9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | HOLDA_MID | | | | | | | |

This is the middle byte of the output Holding Register - Port A. If the Holding A Data Alignment bit is set in the DALIGN register then data read from this address will be bits 23:16 instead. See usage notes in HOLDA register description above.

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | HOLDA_MID[7:0] | Middle byte of the output Holding Register, Port A. |

1.3.1164 DFB[0..0]_HOLDAH

DFB High Byte Holding Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDAH: 0x4000C7AA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | HOLDA_HIGH | | | | | | | |

This is the high byte of the output Holding Register - Port A. See usage notes in HOLDA register description above.

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | HOLDA_HIGH[7:0] | High byte of the output Holding Register, Port A. |

1.3.1165 DFB[0..0]_HOLDAS

DFB Holding Register A Sign Extension

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDAS: 0x4000C7AB

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | HOLDA_SIGNEXT | | | | | | | |

* This is a pseudo register. There are no FFs or even an address decode for this pseudo register. If read or written as a byte it acts the same as all other unused byte addresses in the block's address space - writes are ignored and reads produce 0 on the bus. However, if HOLDA is read as a 32-bit value or HOLDAH is read as a 16-bit value, the sign is extended onto this byte lane. This pseudo register definition is here simply to document this sign extension functionality. See usage notes in HOLDA register description above. READ: Always 0 if read as a byte. Always the sign extension if HOLDA is read as a 32-bit value or HOLDAH is read as a 16-bit value. WRITE: Ignored.

| Bits | Name | Description |
|------|--------------------|---|
| 7:0 | HOLDA_SIGNEXT[7:0] | Output Holding Register Sign Extension, Port A. |

1.3.1166 DFB[0..0]_HOLDB

DFB Low Byte Holding Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDB: 0x4000C7AC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | HOLDB_LOW | | | | | | | |

This is the low byte of the output Holding Register - Port B. If the Holding B Data Alignment bit is set in the DALIGN register then data read from this address will be bits 15:8 instead. See usage notes in HOLDA register description above.

| Bits | Name | Description |
|------|----------------|--|
| 7:0 | HOLDB_LOW[7:0] | Low byte of the output Holding Register, Port B. |

1.3.1167 DFB[0..0]_HOLDBM

DFB Middle Byte Holding Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDBM: 0x4000C7AD

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | HOLDB_MID | | | | | | | |

This is the middle byte of the output Holding Register - Port B. If the Holding B Data Alignment bit is set in the DALIGN register then data read from this address will be bits 23:16 instead. See usage notes in HOLDA register description above.

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | HOLDB_MID[7:0] | Middle byte of the output Holding Register, Port B. |

1.3.1168 DFB[0..0]_HOLDBH

DFB High Byte Holding Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDBH: 0x4000C7AE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | HOLDB_HIGH | | | | | | | |

This is the high byte of the output Holding Register - Port B. See usage notes in HOLDA register description above.

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | HOLDB_HIGH[7:0] | High byte of the output Holding Register, Port B. |

1.3.1169 DFB[0..0]_HOLDBS

DFB Holding Register B Sign Extension

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDBS: 0x4000C7AF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | HOLDB_SIGNEXT | | | | | | | |

* This is a pseudo register. There are no FFs or even an address decode for this pseudo register. If read or written as a byte it acts the same as all other unused byte addresses in the block's address space - writes are ignored and reads produce 0 on the bus. However, if HOLDB is read as a 32-bit value or HOLDBH is read as a 16-bit value, the sign is extended onto this byte lane. This pseudo register definition is here simply to document this sign extension functionality. See usage notes in HOLDA register description above. READ: Always 0 if read as a byte. Always the sign extension if HOLDB is read as a 32-bit value or HOLDBH is read as a 16-bit value. WRITE: Ignored.

| Bits | Name | Description |
|------|--------------------|---|
| 7:0 | HOLDB_SIGNEXT[7:0] | Output Holding Register Sign Extension, Port B. |

1.3.1170 DFB[0..0]_COHER

DFB Coherency Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_COHER: 0x4000C7B0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|-----------|---|----------|---|----------|---|
| SW Access:Reset | R/W:10 | | R/W:10 | | R/W:10 | | R/W:10 | |
| HW Access | R | | R | | R | | R | |
| Name | holdb_key | | holda_key | | stgb_key | | stga_key | |

The 4 2-bit fields of this register are used to select which of the 3 bytes of each of the STAGEA, STAGEB, HOLDA and HOLDB will be used as the Key Coherency Byte. Coherency refers to the HW added to this block to protect against malfunctions of the block in cases where register fields are wider than the bus access, leaving intervals in time when fields are partially written/read (incoherent). The Key Coherency Byte is the SW's way of telling the HW which byte of the field will be written/read last when an update to the field is desired. When the Key byte is written/read, the field is flagged coherent. If any other byte is written/read, the field is flagged incoherent.

| Bits | Name | Description |
|------|----------------|---|
| 7:6 | holdb_key[1:0] | Sets the Key Coherency Byte of the Holding B register See Table 1-755. |
| 5:4 | holda_key[1:0] | Sets the Key Coherency Byte of the Holding A register See Table 1-754. |
| 3:2 | stgb_key[1:0] | Sets the Key Coherency Byte of the Staging B register See Table 1-757. |
| 1:0 | stga_key[1:0] | Sets the Key Coherency Byte of the Staging A register See Table 1-756. |

Table 1-754. Bit field encoding: holda_key_enum

| Value | Name | Description |
|-------|----------------|------------------------|
| 2'b00 | HOLDA_KEY_LOW | Key Byte is low byte. |
| 2'b01 | HOLDA_KEY_MID | Key Byte is med byte. |
| 2'b10 | HOLDA_KEY_HIGH | Key Byte is high byte. |

Table 1-755. Bit field encoding: holdb_key_enum

| Value | Name | Description |
|-------|----------------|------------------------|
| 2'b00 | HOLDB_KEY_LOW | Key Byte is low byte. |
| 2'b01 | HOLDB_KEY_MID | Key Byte is med byte. |
| 2'b10 | HOLDB_KEY_HIGH | Key Byte is high byte. |

Table 1-756. Bit field encoding: stga_key_enum

| Value | Name | Description |
|-------|---------------|------------------------|
| 2'b00 | STGA_KEY_LOW | Key Byte is low byte. |
| 2'b01 | STGA_KEY_MID | Key Byte is med byte. |
| 2'b10 | STGA_KEY_HIGH | Key Byte is high byte. |

1.3.1170 DFB[0..0]_COHER (continued)

Table 1-757. Bit field encoding: stgb_key_enum

| Value | Name | Description |
|-------|---------------|------------------------|
| 2'b00 | STGB_KEY_LOW | Key Byte is low byte. |
| 2'b01 | STGB_KEY_MID | Key Byte is med byte. |
| 2'b10 | STGB_KEY_HIGH | Key Byte is high byte. |

1.3.1171 DFB[0..0]_DALIGN

DFB Data Alignment Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_DALIGN: 0x4000C7B4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|--------------|--------------|-------------|-------------|
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | holdb_dalign | holda_dalign | stgb_dalign | stga_dalign |

These bits when set high causes an 8-bit shift in the data to all access of the corresponding Staging and Holding registers. The purpose of this feature is to allow 9 to 16 bit input and output samples to travel as 16-bit values on the AHB bus. Because the DFB datapath is inherently msb aligned, it is convenient to the System SW to align values on bits 23:8 of the Staging and Holding register to bits 15:0 of the bus. A read of this register produces the last value written to this register.

| Bits | Name | Description |
|------|--------------|--|
| 3 | holdb_dalign | Shifts the read right by a byte. See Table 1-759. |
| 2 | holda_dalign | Shifts the read right by a byte. See Table 1-758. |
| 1 | stgb_dalign | Shifts the write left by a byte. See Table 1-761. |
| 0 | stga_dalign | Shifts the write left by a byte. See Table 1-760. |

Table 1-758. Bit field encoding: holda_dalign_enum

| Value | Name | Description |
|-------|-------------------|--------------------------------|
| 1'b0 | HOLDA_DALIGN_LOW | Reads normally. |
| 1'b1 | HOLDA_DALIGN_HIGH | Reads shifted right by 8-bits. |

Table 1-759. Bit field encoding: holdb_dalign_enum

| Value | Name | Description |
|-------|-------------------|--------------------------------|
| 1'b0 | HOLDB_DALIGN_LOW | Reads normally. |
| 1'b1 | HOLDB_DALIGN_HIGH | Reads shifted right by 8-bits. |

Table 1-760. Bit field encoding: stga_dalign_enum

| Value | Name | Description |
|-------|------------------|--------------------------------|
| 1'b0 | STGA_DALIGN_LOW | Writes normally. |
| 1'b1 | STGA_DALIGN_HIGH | Writes shifted left by 8-bits. |

Table 1-761. Bit field encoding: stgb_dalign_enum

| Value | Name | Description |
|-------|------------------|--------------------------------|
| 1'b0 | STGB_DALIGN_LOW | Writes normally. |
| 1'b1 | STGB_DALIGN_HIGH | Writes shifted left by 8-bits. |

1.3.1172 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] PLD_IT

Reset: N/A

Register : Address

B0_P0_U0_PLD_IT0: 0x40010000
 B0_P0_U0_PLD_IT1: 0x40010004
 B0_P0_U0_PLD_IT2: 0x40010008
 B0_P0_U0_PLD_IT3: 0x4001000C
 B0_P0_U0_PLD_IT4: 0x40010010
 B0_P0_U0_PLD_IT5: 0x40010014
 B0_P0_U0_PLD_IT6: 0x40010018
 B0_P0_U0_PLD_IT7: 0x4001001C
 B0_P0_U0_PLD_IT8: 0x40010020
 B0_P0_U0_PLD_IT9: 0x40010024
 B0_P0_U0_PLD_IT10: 0x40010028
 B0_P0_U0_PLD_IT11: 0x4001002C
 B0_P0_U1_PLD_IT0: 0x40010080
 B0_P0_U1_PLD_IT1: 0x40010084
 B0_P0_U1_PLD_IT2: 0x40010088
 B0_P0_U1_PLD_IT3: 0x4001008C
 B0_P0_U1_PLD_IT4: 0x40010090
 B0_P0_U1_PLD_IT5: 0x40010094
 B0_P0_U1_PLD_IT6: 0x40010098
 B0_P0_U1_PLD_IT7: 0x4001009C
 B0_P0_U1_PLD_IT8: 0x400100A0
 B0_P0_U1_PLD_IT9: 0x400100A4
 B0_P0_U1_PLD_IT10: 0x400100A8
 B0_P0_U1_PLD_IT11: 0x400100AC
 B0_P1_U0_PLD_IT0: 0x40010200
 B0_P1_U0_PLD_IT1: 0x40010204
 B0_P1_U0_PLD_IT2: 0x40010208
 B0_P1_U0_PLD_IT3: 0x4001020C
 B0_P1_U0_PLD_IT4: 0x40010210
 B0_P1_U0_PLD_IT5: 0x40010214
 B0_P1_U0_PLD_IT6: 0x40010218
 B0_P1_U0_PLD_IT7: 0x4001021C

1.3.1172 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B0_P1_U0_PLD_IT8: 0x40010220
B0_P1_U0_PLD_IT9: 0x40010224
B0_P1_U0_PLD_IT10: 0x40010228
B0_P1_U0_PLD_IT11: 0x4001022C
B0_P1_U1_PLD_IT0: 0x40010280
B0_P1_U1_PLD_IT1: 0x40010284
B0_P1_U1_PLD_IT2: 0x40010288
B0_P1_U1_PLD_IT3: 0x4001028C
B0_P1_U1_PLD_IT4: 0x40010290
B0_P1_U1_PLD_IT5: 0x40010294
B0_P1_U1_PLD_IT6: 0x40010298
B0_P1_U1_PLD_IT7: 0x4001029C
B0_P1_U1_PLD_IT8: 0x400102A0
B0_P1_U1_PLD_IT9: 0x400102A4
B0_P1_U1_PLD_IT10: 0x400102A8
B0_P1_U1_PLD_IT11: 0x400102AC
B0_P2_U0_PLD_IT0: 0x40010400
B0_P2_U0_PLD_IT1: 0x40010404
B0_P2_U0_PLD_IT2: 0x40010408
B0_P2_U0_PLD_IT3: 0x4001040C
B0_P2_U0_PLD_IT4: 0x40010410
B0_P2_U0_PLD_IT5: 0x40010414
B0_P2_U0_PLD_IT6: 0x40010418
B0_P2_U0_PLD_IT7: 0x4001041C
B0_P2_U0_PLD_IT8: 0x40010420
B0_P2_U0_PLD_IT9: 0x40010424
B0_P2_U0_PLD_IT10: 0x40010428
B0_P2_U0_PLD_IT11: 0x4001042C
B0_P2_U1_PLD_IT0: 0x40010480
B0_P2_U1_PLD_IT1: 0x40010484
B0_P2_U1_PLD_IT2: 0x40010488
B0_P2_U1_PLD_IT3: 0x4001048C
B0_P2_U1_PLD_IT4: 0x40010490
B0_P2_U1_PLD_IT5: 0x40010494
B0_P2_U1_PLD_IT6: 0x40010498
B0_P2_U1_PLD_IT7: 0x4001049C

1.3.1172 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B0_P2_U1_PLD_IT8: 0x400104A0
 B0_P2_U1_PLD_IT9: 0x400104A4
 B0_P2_U1_PLD_IT10: 0x400104A8
 B0_P2_U1_PLD_IT11: 0x400104AC
 B0_P3_U0_PLD_IT0: 0x40010600
 B0_P3_U0_PLD_IT1: 0x40010604
 B0_P3_U0_PLD_IT2: 0x40010608
 B0_P3_U0_PLD_IT3: 0x4001060C
 B0_P3_U0_PLD_IT4: 0x40010610
 B0_P3_U0_PLD_IT5: 0x40010614
 B0_P3_U0_PLD_IT6: 0x40010618
 B0_P3_U0_PLD_IT7: 0x4001061C
 B0_P3_U0_PLD_IT8: 0x40010620
 B0_P3_U0_PLD_IT9: 0x40010624
 B0_P3_U0_PLD_IT10: 0x40010628
 B0_P3_U0_PLD_IT11: 0x4001062C
 B0_P3_U1_PLD_IT0: 0x40010680
 B0_P3_U1_PLD_IT1: 0x40010684
 B0_P3_U1_PLD_IT2: 0x40010688
 B0_P3_U1_PLD_IT3: 0x4001068C
 B0_P3_U1_PLD_IT4: 0x40010690
 B0_P3_U1_PLD_IT5: 0x40010694
 B0_P3_U1_PLD_IT6: 0x40010698
 B0_P3_U1_PLD_IT7: 0x4001069C
 B0_P3_U1_PLD_IT8: 0x400106A0
 B0_P3_U1_PLD_IT9: 0x400106A4
 B0_P3_U1_PLD_IT10: 0x400106A8
 B0_P3_U1_PLD_IT11: 0x400106AC
 B0_P4_U0_PLD_IT0: 0x40010800
 B0_P4_U0_PLD_IT1: 0x40010804
 B0_P4_U0_PLD_IT2: 0x40010808
 B0_P4_U0_PLD_IT3: 0x4001080C
 B0_P4_U0_PLD_IT4: 0x40010810
 B0_P4_U0_PLD_IT5: 0x40010814
 B0_P4_U0_PLD_IT6: 0x40010818
 B0_P4_U0_PLD_IT7: 0x4001081C

1.3.1172 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B0_P4_U0_PLD_IT8: 0x40010820
B0_P4_U0_PLD_IT9: 0x40010824
B0_P4_U0_PLD_IT10: 0x40010828
B0_P4_U0_PLD_IT11: 0x4001082C
B0_P4_U1_PLD_IT0: 0x40010880
B0_P4_U1_PLD_IT1: 0x40010884
B0_P4_U1_PLD_IT2: 0x40010888
B0_P4_U1_PLD_IT3: 0x4001088C
B0_P4_U1_PLD_IT4: 0x40010890
B0_P4_U1_PLD_IT5: 0x40010894
B0_P4_U1_PLD_IT6: 0x40010898
B0_P4_U1_PLD_IT7: 0x4001089C
B0_P4_U1_PLD_IT8: 0x400108A0
B0_P4_U1_PLD_IT9: 0x400108A4
B0_P4_U1_PLD_IT10: 0x400108A8
B0_P4_U1_PLD_IT11: 0x400108AC
B0_P5_U0_PLD_IT0: 0x40010A00
B0_P5_U0_PLD_IT1: 0x40010A04
B0_P5_U0_PLD_IT2: 0x40010A08
B0_P5_U0_PLD_IT3: 0x40010A0C
B0_P5_U0_PLD_IT4: 0x40010A10
B0_P5_U0_PLD_IT5: 0x40010A14
B0_P5_U0_PLD_IT6: 0x40010A18
B0_P5_U0_PLD_IT7: 0x40010A1C
B0_P5_U0_PLD_IT8: 0x40010A20
B0_P5_U0_PLD_IT9: 0x40010A24
B0_P5_U0_PLD_IT10: 0x40010A28
B0_P5_U0_PLD_IT11: 0x40010A2C
B0_P5_U1_PLD_IT0: 0x40010A80
B0_P5_U1_PLD_IT1: 0x40010A84
B0_P5_U1_PLD_IT2: 0x40010A88
B0_P5_U1_PLD_IT3: 0x40010A8C
B0_P5_U1_PLD_IT4: 0x40010A90
B0_P5_U1_PLD_IT5: 0x40010A94
B0_P5_U1_PLD_IT6: 0x40010A98
B0_P5_U1_PLD_IT7: 0x40010A9C

1.3.1172 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B0_P5_U1_PLD_IT8: 0x40010AA0
 B0_P5_U1_PLD_IT9: 0x40010AA4
 B0_P5_U1_PLD_IT10: 0x40010AA8
 B0_P5_U1_PLD_IT11: 0x40010AAC
 B0_P6_U0_PLD_IT0: 0x40010C00
 B0_P6_U0_PLD_IT1: 0x40010C04
 B0_P6_U0_PLD_IT2: 0x40010C08
 B0_P6_U0_PLD_IT3: 0x40010C0C
 B0_P6_U0_PLD_IT4: 0x40010C10
 B0_P6_U0_PLD_IT5: 0x40010C14
 B0_P6_U0_PLD_IT6: 0x40010C18
 B0_P6_U0_PLD_IT7: 0x40010C1C
 B0_P6_U0_PLD_IT8: 0x40010C20
 B0_P6_U0_PLD_IT9: 0x40010C24
 B0_P6_U0_PLD_IT10: 0x40010C28
 B0_P6_U0_PLD_IT11: 0x40010C2C
 B0_P6_U1_PLD_IT0: 0x40010C80
 B0_P6_U1_PLD_IT1: 0x40010C84
 B0_P6_U1_PLD_IT2: 0x40010C88
 B0_P6_U1_PLD_IT3: 0x40010C8C
 B0_P6_U1_PLD_IT4: 0x40010C90
 B0_P6_U1_PLD_IT5: 0x40010C94
 B0_P6_U1_PLD_IT6: 0x40010C98
 B0_P6_U1_PLD_IT7: 0x40010C9C
 B0_P6_U1_PLD_IT8: 0x40010CA0
 B0_P6_U1_PLD_IT9: 0x40010CA4
 B0_P6_U1_PLD_IT10: 0x40010CA8
 B0_P6_U1_PLD_IT11: 0x40010CAC
 B0_P7_U0_PLD_IT0: 0x40010E00
 B0_P7_U0_PLD_IT1: 0x40010E04
 B0_P7_U0_PLD_IT2: 0x40010E08
 B0_P7_U0_PLD_IT3: 0x40010E0C
 B0_P7_U0_PLD_IT4: 0x40010E10
 B0_P7_U0_PLD_IT5: 0x40010E14
 B0_P7_U0_PLD_IT6: 0x40010E18
 B0_P7_U0_PLD_IT7: 0x40010E1C

1.3.1172 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B0_P7_U0_PLD_IT8: 0x40010E20
B0_P7_U0_PLD_IT9: 0x40010E24
B0_P7_U0_PLD_IT10: 0x40010E28
B0_P7_U0_PLD_IT11: 0x40010E2C
B0_P7_U1_PLD_IT0: 0x40010E80
B0_P7_U1_PLD_IT1: 0x40010E84
B0_P7_U1_PLD_IT2: 0x40010E88
B0_P7_U1_PLD_IT3: 0x40010E8C
B0_P7_U1_PLD_IT4: 0x40010E90
B0_P7_U1_PLD_IT5: 0x40010E94
B0_P7_U1_PLD_IT6: 0x40010E98
B0_P7_U1_PLD_IT7: 0x40010E9C
B0_P7_U1_PLD_IT8: 0x40010EA0
B0_P7_U1_PLD_IT9: 0x40010EA4
B0_P7_U1_PLD_IT10: 0x40010EA8
B0_P7_U1_PLD_IT11: 0x40010EAC
B1_P2_U0_PLD_IT0: 0x40011400
B1_P2_U0_PLD_IT1: 0x40011404
B1_P2_U0_PLD_IT2: 0x40011408
B1_P2_U0_PLD_IT3: 0x4001140C
B1_P2_U0_PLD_IT4: 0x40011410
B1_P2_U0_PLD_IT5: 0x40011414
B1_P2_U0_PLD_IT6: 0x40011418
B1_P2_U0_PLD_IT7: 0x4001141C
B1_P2_U0_PLD_IT8: 0x40011420
B1_P2_U0_PLD_IT9: 0x40011424
B1_P2_U0_PLD_IT10: 0x40011428
B1_P2_U0_PLD_IT11: 0x4001142C
B1_P2_U1_PLD_IT0: 0x40011480
B1_P2_U1_PLD_IT1: 0x40011484
B1_P2_U1_PLD_IT2: 0x40011488
B1_P2_U1_PLD_IT3: 0x4001148C
B1_P2_U1_PLD_IT4: 0x40011490
B1_P2_U1_PLD_IT5: 0x40011494
B1_P2_U1_PLD_IT6: 0x40011498
B1_P2_U1_PLD_IT7: 0x4001149C

1.3.1172 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B1_P2_U1_PLD_IT8: 0x400114A0
 B1_P2_U1_PLD_IT9: 0x400114A4
 B1_P2_U1_PLD_IT10: 0x400114A8
 B1_P2_U1_PLD_IT11: 0x400114AC
 B1_P3_U0_PLD_IT0: 0x40011600
 B1_P3_U0_PLD_IT1: 0x40011604
 B1_P3_U0_PLD_IT2: 0x40011608
 B1_P3_U0_PLD_IT3: 0x4001160C
 B1_P3_U0_PLD_IT4: 0x40011610
 B1_P3_U0_PLD_IT5: 0x40011614
 B1_P3_U0_PLD_IT6: 0x40011618
 B1_P3_U0_PLD_IT7: 0x4001161C
 B1_P3_U0_PLD_IT8: 0x40011620
 B1_P3_U0_PLD_IT9: 0x40011624
 B1_P3_U0_PLD_IT10: 0x40011628
 B1_P3_U0_PLD_IT11: 0x4001162C
 B1_P3_U1_PLD_IT0: 0x40011680
 B1_P3_U1_PLD_IT1: 0x40011684
 B1_P3_U1_PLD_IT2: 0x40011688
 B1_P3_U1_PLD_IT3: 0x4001168C
 B1_P3_U1_PLD_IT4: 0x40011690
 B1_P3_U1_PLD_IT5: 0x40011694
 B1_P3_U1_PLD_IT6: 0x40011698
 B1_P3_U1_PLD_IT7: 0x4001169C
 B1_P3_U1_PLD_IT8: 0x400116A0
 B1_P3_U1_PLD_IT9: 0x400116A4
 B1_P3_U1_PLD_IT10: 0x400116A8
 B1_P3_U1_PLD_IT11: 0x400116AC
 B1_P4_U0_PLD_IT0: 0x40011800
 B1_P4_U0_PLD_IT1: 0x40011804
 B1_P4_U0_PLD_IT2: 0x40011808
 B1_P4_U0_PLD_IT3: 0x4001180C
 B1_P4_U0_PLD_IT4: 0x40011810
 B1_P4_U0_PLD_IT5: 0x40011814
 B1_P4_U0_PLD_IT6: 0x40011818
 B1_P4_U0_PLD_IT7: 0x4001181C

1.3.1172 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B1_P4_U0_PLD_IT8: 0x40011820
B1_P4_U0_PLD_IT9: 0x40011824
B1_P4_U0_PLD_IT10: 0x40011828
B1_P4_U0_PLD_IT11: 0x4001182C
B1_P4_U1_PLD_IT0: 0x40011880
B1_P4_U1_PLD_IT1: 0x40011884
B1_P4_U1_PLD_IT2: 0x40011888
B1_P4_U1_PLD_IT3: 0x4001188C
B1_P4_U1_PLD_IT4: 0x40011890
B1_P4_U1_PLD_IT5: 0x40011894
B1_P4_U1_PLD_IT6: 0x40011898
B1_P4_U1_PLD_IT7: 0x4001189C
B1_P4_U1_PLD_IT8: 0x400118A0
B1_P4_U1_PLD_IT9: 0x400118A4
B1_P4_U1_PLD_IT10: 0x400118A8
B1_P4_U1_PLD_IT11: 0x400118AC
B1_P5_U0_PLD_IT0: 0x40011A00
B1_P5_U0_PLD_IT1: 0x40011A04
B1_P5_U0_PLD_IT2: 0x40011A08
B1_P5_U0_PLD_IT3: 0x40011A0C
B1_P5_U0_PLD_IT4: 0x40011A10
B1_P5_U0_PLD_IT5: 0x40011A14
B1_P5_U0_PLD_IT6: 0x40011A18
B1_P5_U0_PLD_IT7: 0x40011A1C
B1_P5_U0_PLD_IT8: 0x40011A20
B1_P5_U0_PLD_IT9: 0x40011A24
B1_P5_U0_PLD_IT10: 0x40011A28
B1_P5_U0_PLD_IT11: 0x40011A2C
B1_P5_U1_PLD_IT0: 0x40011A80
B1_P5_U1_PLD_IT1: 0x40011A84
B1_P5_U1_PLD_IT2: 0x40011A88
B1_P5_U1_PLD_IT3: 0x40011A8C
B1_P5_U1_PLD_IT4: 0x40011A90
B1_P5_U1_PLD_IT5: 0x40011A94
B1_P5_U1_PLD_IT6: 0x40011A98
B1_P5_U1_PLD_IT7: 0x40011A9C

1.3.1172 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B1_P5_U1_PLD_IT8: 0x40011AA0

B1_P5_U1_PLD_IT9: 0x40011AA4

B1_P5_U1_PLD_IT10: 0x40011AA8

B1_P5_U1_PLD_IT11: 0x40011AAC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | R | R | R | R | R | R | R |
| Name | PLD0_ITxC _7 | PLD0_ITxC _6 | PLD0_ITxC _5 | PLD0_ITxC _4 | PLD0_ITxC _3 | PLD0_ITxC _2 | PLD0_ITxC _1 | PLD0_ITxC _0 |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | R | R | R | R | R | R | R |
| Name | PLD1_ITxC _7 | PLD1_ITxC _6 | PLD1_ITxC _5 | PLD1_ITxC _4 | PLD1_ITxC _3 | PLD1_ITxC _2 | PLD1_ITxC _1 | PLD1_ITxC _0 |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | R | R | R | R | R | R | R |
| Name | PLD0_ITxT _7 | PLD0_ITxT _6 | PLD0_ITxT _5 | PLD0_ITxT _4 | PLD0_ITxT _3 | PLD0_ITxT _2 | PLD0_ITxT _1 | PLD0_ITxT _0 |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | R | R | R | R | R | R | R |
| Name | PLD1_ITxT _7 | PLD1_ITxT _6 | PLD1_ITxT _5 | PLD1_ITxT _4 | PLD1_ITxT _3 | PLD1_ITxT _2 | PLD1_ITxT _1 | PLD1_ITxT _0 |

Complement input term byte

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 31 | PLD1_ITxT_7 | True input term. Bit position corresponds to product term. |
| 30 | PLD1_ITxT_6 | True input term. Bit position corresponds to product term. |
| 29 | PLD1_ITxT_5 | True input term. Bit position corresponds to product term. |
| 28 | PLD1_ITxT_4 | True input term. Bit position corresponds to product term. |
| 27 | PLD1_ITxT_3 | True input term. Bit position corresponds to product term. |
| 26 | PLD1_ITxT_2 | True input term. Bit position corresponds to product term. |
| 25 | PLD1_ITxT_1 | True input term. Bit position corresponds to product term. |

1.3.1172 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

| | | |
|----|-------------|---|
| 24 | PLD1_ITxT_0 | True input term. Bit position corresponds to product term. |
| 23 | PLD0_ITxT_7 | True input term. Bit position corresponds to product term. |
| 22 | PLD0_ITxT_6 | True input term. Bit position corresponds to product term. |
| 21 | PLD0_ITxT_5 | True input term. Bit position corresponds to product term. |
| 20 | PLD0_ITxT_4 | True input term. Bit position corresponds to product term. |
| 19 | PLD0_ITxT_3 | True input term. Bit position corresponds to product term. |
| 18 | PLD0_ITxT_2 | True input term. Bit position corresponds to product term. |
| 17 | PLD0_ITxT_1 | True input term. Bit position corresponds to product term. |
| 16 | PLD0_ITxT_0 | True input term. Bit position corresponds to product term. |
| 15 | PLD1_ITxC_7 | Complement input term. Bit position corresponds to product term |
| 14 | PLD1_ITxC_6 | Complement input term. Bit position corresponds to product term |
| 13 | PLD1_ITxC_5 | Complement input term. Bit position corresponds to product term |
| 12 | PLD1_ITxC_4 | Complement input term. Bit position corresponds to product term |
| 11 | PLD1_ITxC_3 | Complement input term. Bit position corresponds to product term |
| 10 | PLD1_ITxC_2 | Complement input term. Bit position corresponds to product term |
| 9 | PLD1_ITxC_1 | Complement input term. Bit position corresponds to product term |
| 8 | PLD1_ITxC_0 | Complement input term. Bit position corresponds to product term |
| 7 | PLD0_ITxC_7 | Complement input term. Bit position corresponds to product term |
| 6 | PLD0_ITxC_6 | Complement input term. Bit position corresponds to product term |
| 5 | PLD0_ITxC_5 | Complement input term. Bit position corresponds to product term |
| 4 | PLD0_ITxC_4 | Complement input term. Bit position corresponds to product term |
| 3 | PLD0_ITxC_3 | Complement input term. Bit position corresponds to product term |
| 2 | PLD0_ITxC_2 | Complement input term. Bit position corresponds to product term |
| 1 | PLD0_ITxC_1 | Complement input term. Bit position corresponds to product term |
| 0 | PLD0_ITxC_0 | Complement input term. Bit position corresponds to product term |

1.3.1173 B[0..3]_P[0..7]_U[0..1]_PLD_ORT[0..3] PLD_ORT

Reset: N/A

Register : Address

B0_P0_U0_PLD_ORT0: 0x40010030
 B0_P0_U0_PLD_ORT1: 0x40010032
 B0_P0_U0_PLD_ORT2: 0x40010034
 B0_P0_U0_PLD_ORT3: 0x40010036
 B0_P0_U1_PLD_ORT0: 0x400100B0
 B0_P0_U1_PLD_ORT1: 0x400100B2
 B0_P0_U1_PLD_ORT2: 0x400100B4
 B0_P0_U1_PLD_ORT3: 0x400100B6
 B0_P1_U0_PLD_ORT0: 0x40010230
 B0_P1_U0_PLD_ORT1: 0x40010232
 B0_P1_U0_PLD_ORT2: 0x40010234
 B0_P1_U0_PLD_ORT3: 0x40010236
 B0_P1_U1_PLD_ORT0: 0x400102B0
 B0_P1_U1_PLD_ORT1: 0x400102B2
 B0_P1_U1_PLD_ORT2: 0x400102B4
 B0_P1_U1_PLD_ORT3: 0x400102B6
 B0_P2_U0_PLD_ORT0: 0x40010430
 B0_P2_U0_PLD_ORT1: 0x40010432
 B0_P2_U0_PLD_ORT2: 0x40010434
 B0_P2_U0_PLD_ORT3: 0x40010436
 B0_P2_U1_PLD_ORT0: 0x400104B0
 B0_P2_U1_PLD_ORT1: 0x400104B2
 B0_P2_U1_PLD_ORT2: 0x400104B4
 B0_P2_U1_PLD_ORT3: 0x400104B6
 B0_P3_U0_PLD_ORT0: 0x40010630
 B0_P3_U0_PLD_ORT1: 0x40010632
 B0_P3_U0_PLD_ORT2: 0x40010634
 B0_P3_U0_PLD_ORT3: 0x40010636
 B0_P3_U1_PLD_ORT0: 0x400106B0
 B0_P3_U1_PLD_ORT1: 0x400106B2
 B0_P3_U1_PLD_ORT2: 0x400106B4
 B0_P3_U1_PLD_ORT3: 0x400106B6

1.3.1173 B[0..3]_P[0..7]_U[0..1]_PLD_OR[0..3] (continued)

Register : Address

B0_P4_U0_PLD_OR[0]: 0x40010830
B0_P4_U0_PLD_OR[1]: 0x40010832
B0_P4_U0_PLD_OR[2]: 0x40010834
B0_P4_U0_PLD_OR[3]: 0x40010836
B0_P4_U1_PLD_OR[0]: 0x400108B0
B0_P4_U1_PLD_OR[1]: 0x400108B2
B0_P4_U1_PLD_OR[2]: 0x400108B4
B0_P4_U1_PLD_OR[3]: 0x400108B6
B0_P5_U0_PLD_OR[0]: 0x40010A30
B0_P5_U0_PLD_OR[1]: 0x40010A32
B0_P5_U0_PLD_OR[2]: 0x40010A34
B0_P5_U0_PLD_OR[3]: 0x40010A36
B0_P5_U1_PLD_OR[0]: 0x40010AB0
B0_P5_U1_PLD_OR[1]: 0x40010AB2
B0_P5_U1_PLD_OR[2]: 0x40010AB4
B0_P5_U1_PLD_OR[3]: 0x40010AB6
B0_P6_U0_PLD_OR[0]: 0x40010C30
B0_P6_U0_PLD_OR[1]: 0x40010C32
B0_P6_U0_PLD_OR[2]: 0x40010C34
B0_P6_U0_PLD_OR[3]: 0x40010C36
B0_P6_U1_PLD_OR[0]: 0x40010CB0
B0_P6_U1_PLD_OR[1]: 0x40010CB2
B0_P6_U1_PLD_OR[2]: 0x40010CB4
B0_P6_U1_PLD_OR[3]: 0x40010CB6
B0_P7_U0_PLD_OR[0]: 0x40010E30
B0_P7_U0_PLD_OR[1]: 0x40010E32
B0_P7_U0_PLD_OR[2]: 0x40010E34
B0_P7_U0_PLD_OR[3]: 0x40010E36
B0_P7_U1_PLD_OR[0]: 0x40010EB0
B0_P7_U1_PLD_OR[1]: 0x40010EB2
B0_P7_U1_PLD_OR[2]: 0x40010EB4
B0_P7_U1_PLD_OR[3]: 0x40010EB6
B1_P2_U0_PLD_OR[0]: 0x40011430
B1_P2_U0_PLD_OR[1]: 0x40011432
B1_P2_U0_PLD_OR[2]: 0x40011434
B1_P2_U0_PLD_OR[3]: 0x40011436

1.3.1173 B[0..3]_P[0..7]_U[0..1]_PLD_OR[0..3] (continued)

Register : Address

B1_P2_U1_PLD_OR0: 0x400114B0
 B1_P2_U1_PLD_OR1: 0x400114B2
 B1_P2_U1_PLD_OR2: 0x400114B4
 B1_P2_U1_PLD_OR3: 0x400114B6
 B1_P3_U0_PLD_OR0: 0x40011630
 B1_P3_U0_PLD_OR1: 0x40011632
 B1_P3_U0_PLD_OR2: 0x40011634
 B1_P3_U0_PLD_OR3: 0x40011636
 B1_P3_U1_PLD_OR0: 0x400116B0
 B1_P3_U1_PLD_OR1: 0x400116B2
 B1_P3_U1_PLD_OR2: 0x400116B4
 B1_P3_U1_PLD_OR3: 0x400116B6
 B1_P4_U0_PLD_OR0: 0x40011830
 B1_P4_U0_PLD_OR1: 0x40011832
 B1_P4_U0_PLD_OR2: 0x40011834
 B1_P4_U0_PLD_OR3: 0x40011836
 B1_P4_U1_PLD_OR0: 0x400118B0
 B1_P4_U1_PLD_OR1: 0x400118B2
 B1_P4_U1_PLD_OR2: 0x400118B4
 B1_P4_U1_PLD_OR3: 0x400118B6
 B1_P5_U0_PLD_OR0: 0x40011A30
 B1_P5_U0_PLD_OR1: 0x40011A32
 B1_P5_U0_PLD_OR2: 0x40011A34
 B1_P5_U0_PLD_OR3: 0x40011A36
 B1_P5_U1_PLD_OR0: 0x40011AB0
 B1_P5_U1_PLD_OR1: 0x40011AB2
 B1_P5_U1_PLD_OR2: 0x40011AB4
 B1_P5_U1_PLD_OR3: 0x40011AB6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | R | R | R | R | R | R | R |
| Name | PLD0_OR _PTx_7 | PLD0_OR _PTx_6 | PLD0_OR _PTx_5 | PLD0_OR _PTx_4 | PLD0_OR _PTx_3 | PLD0_OR _PTx_2 | PLD0_OR _PTx_1 | PLD0_OR _PTx_0 |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |

1.3.1173 B[0..3]_P[0..7]_U[0..1]_PLD_OR_T[0..3] (continued)

| | | | | | | | | |
|-----------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| HW Access | R | R | R | R | R | R | R | R |
| Name | PLD1_OR_T_PT_x_7 | PLD1_OR_T_PT_x_6 | PLD1_OR_T_PT_x_5 | PLD1_OR_T_PT_x_4 | PLD1_OR_T_PT_x_3 | PLD1_OR_T_PT_x_2 | PLD1_OR_T_PT_x_1 | PLD1_OR_T_PT_x_0 |

OR term byte

Register Segment: 2

| Bits | Name | Description |
|------|------------------|--|
| 15 | PLD1_OR_T_PT_x_7 | OR term. Bit position corresponds to product term. |
| 14 | PLD1_OR_T_PT_x_6 | OR term. Bit position corresponds to product term. |
| 13 | PLD1_OR_T_PT_x_5 | OR term. Bit position corresponds to product term. |
| 12 | PLD1_OR_T_PT_x_4 | OR term. Bit position corresponds to product term. |
| 11 | PLD1_OR_T_PT_x_3 | OR term. Bit position corresponds to product term. |
| 10 | PLD1_OR_T_PT_x_2 | OR term. Bit position corresponds to product term. |
| 9 | PLD1_OR_T_PT_x_1 | OR term. Bit position corresponds to product term. |
| 8 | PLD1_OR_T_PT_x_0 | OR term. Bit position corresponds to product term. |
| 7 | PLD0_OR_T_PT_x_7 | OR term. Bit position corresponds to product term. |
| 6 | PLD0_OR_T_PT_x_6 | OR term. Bit position corresponds to product term. |
| 5 | PLD0_OR_T_PT_x_5 | OR term. Bit position corresponds to product term. |
| 4 | PLD0_OR_T_PT_x_4 | OR term. Bit position corresponds to product term. |
| 3 | PLD0_OR_T_PT_x_3 | OR term. Bit position corresponds to product term. |
| 2 | PLD0_OR_T_PT_x_2 | OR term. Bit position corresponds to product term. |
| 1 | PLD0_OR_T_PT_x_1 | OR term. Bit position corresponds to product term. |
| 0 | PLD0_OR_T_PT_x_0 | OR term. Bit position corresponds to product term. |

1.3.1174 B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST

MC_CFG_CEN_CONST

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_CEN_CONST: 0x40010038
 B0_P0_U1_MC_CFG_CEN_CONST: 0x400100B8
 B0_P1_U0_MC_CFG_CEN_CONST: 0x40010238
 B0_P1_U1_MC_CFG_CEN_CONST: 0x400102B8
 B0_P2_U0_MC_CFG_CEN_CONST: 0x40010438
 B0_P2_U1_MC_CFG_CEN_CONST: 0x400104B8
 B0_P3_U0_MC_CFG_CEN_CONST: 0x40010638
 B0_P3_U1_MC_CFG_CEN_CONST: 0x400106B8
 B0_P4_U0_MC_CFG_CEN_CONST: 0x40010838
 B0_P4_U1_MC_CFG_CEN_CONST: 0x400108B8
 B0_P5_U0_MC_CFG_CEN_CONST: 0x40010A38
 B0_P5_U1_MC_CFG_CEN_CONST: 0x40010AB8
 B0_P6_U0_MC_CFG_CEN_CONST: 0x40010C38
 B0_P6_U1_MC_CFG_CEN_CONST: 0x40010CB8
 B0_P7_U0_MC_CFG_CEN_CONST: 0x40010E38
 B0_P7_U1_MC_CFG_CEN_CONST: 0x40010EB8
 B1_P2_U0_MC_CFG_CEN_CONST: 0x40011438
 B1_P2_U1_MC_CFG_CEN_CONST: 0x400114B8
 B1_P3_U0_MC_CFG_CEN_CONST: 0x40011638
 B1_P3_U1_MC_CFG_CEN_CONST: 0x400116B8
 B1_P4_U0_MC_CFG_CEN_CONST: 0x40011838
 B1_P4_U1_MC_CFG_CEN_CONST: 0x400118B8
 B1_P5_U0_MC_CFG_CEN_CONST: 0x40011A38
 B1_P5_U1_MC_CFG_CEN_CONST: 0x40011AB8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|--------------|----------------|--------------|----------------|--------------|----------------|--------------|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | R | R | R | R | R | R | R |
| Name | PLD0_MC3_DFF_C | PLD0_MC3_CEN | PLD0_MC2_DFF_C | PLD0_MC2_CEN | PLD0_MC1_DFF_C | PLD0_MC1_CEN | PLD0_MC0_DFF_C | PLD0_MC0_CEN |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | R | R | R | R | R | R | R |

1.3.1174 B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST (continued)

| Name | PLD1_MC3_DFF_C | PLD1_MC3_CEN | PLD1_MC2_DFF_C | PLD1_MC2_CEN | PLD1_MC1_DFF_C | PLD1_MC1_CEN | PLD1_MC0_DFF_C | PLD1_MC0_CEN |
|------|----------------|--------------|----------------|--------------|----------------|--------------|----------------|--------------|
|------|----------------|--------------|----------------|--------------|----------------|--------------|----------------|--------------|

Macrocell configuration for Carry Enable and Constant

Register Segment: 2

| Bits | Name | Description |
|------|----------------|--|
| 15 | PLD1_MC3_DFF_C | DFF Constant See Table 1-763. |
| 14 | PLD1_MC3_CEN | Carry enable See Table 1-762. |
| 13 | PLD1_MC2_DFF_C | DFF Constant See Table 1-763. |
| 12 | PLD1_MC2_CEN | Carry enable See Table 1-762. |
| 11 | PLD1_MC1_DFF_C | DFF Constant See Table 1-763. |
| 10 | PLD1_MC1_CEN | Carry enable See Table 1-762. |
| 9 | PLD1_MC0_DFF_C | DFF Constant See Table 1-763. |
| 8 | PLD1_MC0_CEN | Carry enable See Table 1-762. |
| 7 | PLD0_MC3_DFF_C | DFF Constant See Table 1-763. |
| 6 | PLD0_MC3_CEN | Carry enable See Table 1-762. |
| 5 | PLD0_MC2_DFF_C | DFF Constant See Table 1-763. |
| 4 | PLD0_MC2_CEN | Carry enable See Table 1-762. |
| 3 | PLD0_MC1_DFF_C | DFF Constant See Table 1-763. |
| 2 | PLD0_MC1_CEN | Carry enable See Table 1-762. |

@((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) +

1.3.1174 B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST (continued)

1 PLD0_MC0_DFF_C DFF Constant

[See Table 1-763.](#)

0 PLD0_MC0_CEN Carry enable

[See Table 1-762.](#)

Table 1-762. Bit field encoding: CEN_ENUM

| Value | Name | Description |
|-------|---------|-------------|
| 1'b0 | DISABLE | Disabled |
| 1'b1 | ENABLE | Enabled |

Table 1-763. Bit field encoding: DFF_ENUM

| Value | Name | Description |
|-------|----------|------------------|
| 1'b0 | TRUE | DFF non-inverted |
| 1'b1 | INVERTED | DFF inverted |

1.3.1175 B[0..3]_P[0..7]_U[0..1]_MC_CFG_XORFB

MC_CFG_XORFB

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_XORFB: 0x4001003A
 B0_P0_U1_MC_CFG_XORFB: 0x400100BA
 B0_P1_U0_MC_CFG_XORFB: 0x4001023A
 B0_P1_U1_MC_CFG_XORFB: 0x400102BA
 B0_P2_U0_MC_CFG_XORFB: 0x4001043A
 B0_P2_U1_MC_CFG_XORFB: 0x400104BA
 B0_P3_U0_MC_CFG_XORFB: 0x4001063A
 B0_P3_U1_MC_CFG_XORFB: 0x400106BA
 B0_P4_U0_MC_CFG_XORFB: 0x4001083A
 B0_P4_U1_MC_CFG_XORFB: 0x400108BA
 B0_P5_U0_MC_CFG_XORFB: 0x40010A3A
 B0_P5_U1_MC_CFG_XORFB: 0x40010ABA
 B0_P6_U0_MC_CFG_XORFB: 0x40010C3A
 B0_P6_U1_MC_CFG_XORFB: 0x40010CBA
 B0_P7_U0_MC_CFG_XORFB: 0x40010E3A
 B0_P7_U1_MC_CFG_XORFB: 0x40010EBA
 B1_P2_U0_MC_CFG_XORFB: 0x4001143A
 B1_P2_U1_MC_CFG_XORFB: 0x400114BA
 B1_P3_U0_MC_CFG_XORFB: 0x4001163A
 B1_P3_U1_MC_CFG_XORFB: 0x400116BA
 B1_P4_U0_MC_CFG_XORFB: 0x4001183A
 B1_P4_U1_MC_CFG_XORFB: 0x400118BA
 B1_P5_U0_MC_CFG_XORFB: 0x40011A3A
 B1_P5_U1_MC_CFG_XORFB: 0x40011ABA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|----------------|---|----------------|---|----------------|---|
| SW Access:Reset | R/W:UU | | R/W:UU | | R/W:UU | | R/W:UU | |
| HW Access | R | | R | | R | | R | |
| Name | PLD0_MC3_XORFB | | PLD0_MC2_XORFB | | PLD0_MC1_XORFB | | PLD0_MC0_XORFB | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|----------------|----|----------------|----|----------------|----|----------------|---|
| SW Access:Reset | R/W:UU | | R/W:UU | | R/W:UU | | R/W:UU | |
| HW Access | R | | R | | R | | R | |
| Name | PLD1_MC3_XORFB | | PLD1_MC2_XORFB | | PLD1_MC1_XORFB | | PLD1_MC0_XORFB | |

```
@((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) +
```

1.3.1175 B[0..3]_P[0..7]_U[0..1]_MC_CFG_XORFB (continued)

Macrocell configuration for XOR feedback

Register Segment: 2

| Bits | Name | Description |
|-------|---------------------|--|
| 15:14 | PLD1_MC3_XORFB[1:0] | XOR feedback See Table 1-764. |
| 13:12 | PLD1_MC2_XORFB[1:0] | XOR feedback See Table 1-764. |
| 11:10 | PLD1_MC1_XORFB[1:0] | XOR feedback See Table 1-764. |
| 9:8 | PLD1_MC0_XORFB[1:0] | XOR feedback See Table 1-764. |
| 7:6 | PLD0_MC3_XORFB[1:0] | XOR feedback See Table 1-764. |
| 5:4 | PLD0_MC2_XORFB[1:0] | XOR feedback See Table 1-764. |
| 3:2 | PLD0_MC1_XORFB[1:0] | XOR feedback See Table 1-764. |
| 1:0 | PLD0_MC0_XORFB[1:0] | XOR feedback See Table 1-764. |

Table 1-764. Bit field encoding: XORFB_ENUM

| Value | Name | Description |
|-------|-------|-------------|
| 2'b00 | DFF | DFF |
| 2'b01 | CARRY | Carry |
| 2'b10 | TFF_H | TFF on high |
| 2'b11 | TFF_L | TFF on low |

1.3.1176 B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET

MC_CFG_SET_RESET

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_SET_RESET: 0x4001003C

B0_P0_U1_MC_CFG_SET_RESET: 0x400100BC

B0_P1_U0_MC_CFG_SET_RESET: 0x4001023C

B0_P1_U1_MC_CFG_SET_RESET: 0x400102BC

B0_P2_U0_MC_CFG_SET_RESET: 0x4001043C

B0_P2_U1_MC_CFG_SET_RESET: 0x400104BC

B0_P3_U0_MC_CFG_SET_RESET: 0x4001063C

B0_P3_U1_MC_CFG_SET_RESET: 0x400106BC

B0_P4_U0_MC_CFG_SET_RESET: 0x4001083C

B0_P4_U1_MC_CFG_SET_RESET: 0x400108BC

B0_P5_U0_MC_CFG_SET_RESET: 0x40010A3C

B0_P5_U1_MC_CFG_SET_RESET: 0x40010ABC

B0_P6_U0_MC_CFG_SET_RESET: 0x40010C3C

B0_P6_U1_MC_CFG_SET_RESET: 0x40010CBC

B0_P7_U0_MC_CFG_SET_RESET: 0x40010E3C

B0_P7_U1_MC_CFG_SET_RESET: 0x40010EBC

B1_P2_U0_MC_CFG_SET_RESET: 0x4001143C

B1_P2_U1_MC_CFG_SET_RESET: 0x400114BC

B1_P3_U0_MC_CFG_SET_RESET: 0x4001163C

B1_P3_U1_MC_CFG_SET_RESET: 0x400116BC

B1_P4_U0_MC_CFG_SET_RESET: 0x4001183C

B1_P4_U1_MC_CFG_SET_RESET: 0x400118BC

B1_P5_U0_MC_CFG_SET_RESET: 0x40011A3C

B1_P5_U1_MC_CFG_SET_RESET: 0x40011ABC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------------------|----------------------|----------------------------|----------------------|----------------------------|----------------------|----------------------------|----------------------|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | R | R | R | R | R | R | R |
| Name | PLD0_MC3 _RESET_S EL | PLD0_MC3 _SET_SEL | PLD0_MC2 _RESET_S EL | PLD0_MC2 _SET_SEL | PLD0_MC1 _RESET_S EL | PLD0_MC1 _SET_SEL | PLD0_MC0 _RESET_S EL | PLD0_MC0 _SET_SEL |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U | R/W:U |

$$@((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) +$$

1.3.1176 B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET (continued)

| HW Access | R | R | R | R | R | R | R | R |
|-----------|--------------------|------------------|--------------------|------------------|--------------------|------------------|--------------------|------------------|
| Name | PLD1_MC3_RESET_SEL | PLD1_MC3_SET_SEL | PLD1_MC2_RESET_SEL | PLD1_MC2_SET_SEL | PLD1_MC1_RESET_SEL | PLD1_MC1_SET_SEL | PLD1_MC0_RESET_SEL | PLD1_MC0_SET_SEL |

Macrocell configuration for set and reset

Register Segment: 2

| Bits | Name | Description |
|------|--------------------|---|
| 15 | PLD1_MC3_RESET_SEL | Reset select enable See Table 1-765. |
| 14 | PLD1_MC3_SET_SEL | Set select enable See Table 1-766. |
| 13 | PLD1_MC2_RESET_SEL | Reset select enable See Table 1-765. |
| 12 | PLD1_MC2_SET_SEL | Set select enable See Table 1-766. |
| 11 | PLD1_MC1_RESET_SEL | Reset select enable See Table 1-765. |
| 10 | PLD1_MC1_SET_SEL | Set select enable See Table 1-766. |
| 9 | PLD1_MC0_RESET_SEL | Reset select enable See Table 1-765. |
| 8 | PLD1_MC0_SET_SEL | Set select enable See Table 1-766. |
| 7 | PLD0_MC3_RESET_SEL | Reset select enable See Table 1-765. |
| 6 | PLD0_MC3_SET_SEL | Set select enable See Table 1-766. |
| 5 | PLD0_MC2_RESET_SEL | Reset select enable See Table 1-765. |
| 4 | PLD0_MC2_SET_SEL | Set select enable See Table 1-766. |
| 3 | PLD0_MC1_RESET_SEL | Reset select enable See Table 1-765. |
| 2 | PLD0_MC1_SET_SEL | Set select enable See Table 1-766. |

1.3.1176 B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET (continued)

| | | |
|---|--------------------|---|
| 1 | PLD0_MC0_RESET_SEL | Reset select enable See Table 1-765. |
| 0 | PLD0_MC0_SET_SEL | Set select enable See Table 1-766. |

Table 1-765. Bit field encoding: RESET_SEL_ENUM

| Value | Name | Description |
|-------|---------|----------------|
| 1'b0 | DISABLE | Reset not used |
| 1'b1 | ENABLE | Reset enabled |

Table 1-766. Bit field encoding: SET_SEL_ENUM

| Value | Name | Description |
|-------|---------|-------------------|
| 1'b0 | DISABLE | Set not used |
| 1'b1 | ENABLE | Set reset enabled |

1.3.1177 B[0..3]_P[0..7]_U[0..1]_MC_CFG_BYPASS

MC_CFG_BYPASS

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_BYPASS: 0x4001003E
 B0_P0_U1_MC_CFG_BYPASS: 0x400100BE
 B0_P1_U0_MC_CFG_BYPASS: 0x4001023E
 B0_P1_U1_MC_CFG_BYPASS: 0x400102BE
 B0_P2_U0_MC_CFG_BYPASS: 0x4001043E
 B0_P2_U1_MC_CFG_BYPASS: 0x400104BE
 B0_P3_U0_MC_CFG_BYPASS: 0x4001063E
 B0_P3_U1_MC_CFG_BYPASS: 0x400106BE
 B0_P4_U0_MC_CFG_BYPASS: 0x4001083E
 B0_P4_U1_MC_CFG_BYPASS: 0x400108BE
 B0_P5_U0_MC_CFG_BYPASS: 0x40010A3E
 B0_P5_U1_MC_CFG_BYPASS: 0x40010ABE
 B0_P6_U0_MC_CFG_BYPASS: 0x40010C3E
 B0_P6_U1_MC_CFG_BYPASS: 0x40010CBE
 B0_P7_U0_MC_CFG_BYPASS: 0x40010E3E
 B0_P7_U1_MC_CFG_BYPASS: 0x40010EBE
 B1_P2_U0_MC_CFG_BYPASS: 0x4001143E
 B1_P2_U1_MC_CFG_BYPASS: 0x400114BE
 B1_P3_U0_MC_CFG_BYPASS: 0x4001163E
 B1_P3_U1_MC_CFG_BYPASS: 0x400116BE
 B1_P4_U0_MC_CFG_BYPASS: 0x4001183E
 B1_P4_U1_MC_CFG_BYPASS: 0x400118BE
 B1_P5_U0_MC_CFG_BYPASS: 0x40011A3E
 B1_P5_U1_MC_CFG_BYPASS: 0x40011ABE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------------|------|-----------------|------|-----------------|------|-----------------|
| SW Access:Reset | NA:0 | R/W:U | NA:0 | R/W:U | NA:0 | R/W:U | NA:0 | R/W:U |
| HW Access | NA | R | NA | R | NA | R | NA | R |
| Name | | PLD0_MC3_BYPASS | | PLD0_MC2_BYPASS | | PLD0_MC1_BYPASS | | PLD0_MC0_BYPASS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|-------|------|-------|------|-------|------|-------|
| SW Access:Reset | NA:0 | R/W:U | NA:0 | R/W:U | NA:0 | R/W:U | NA:0 | R/W:U |
| HW Access | NA | R | NA | R | NA | R | NA | R |

1.3.1177 B[0..3]_P[0..7]_U[0..1]_MC_CFG_BYPASS (continued)

| | | | | | | | | |
|------|--|-----------------|--|-----------------|--|-----------------|--|-----------------|
| Name | | PLD1_MC3_BYPASS | | PLD1_MC2_BYPASS | | PLD1_MC1_BYPASS | | PLD1_MC0_BYPASS |
|------|--|-----------------|--|-----------------|--|-----------------|--|-----------------|

Macrocell configuration for bypass

Register Segment: 2

| Bits | Name | Description |
|------|-----------------|--|
| 14 | PLD1_MC3_BYPASS | Bypass selection See Table 1-767. |
| 12 | PLD1_MC2_BYPASS | Bypass selection See Table 1-767. |
| 10 | PLD1_MC1_BYPASS | Bypass selection See Table 1-767. |
| 8 | PLD1_MC0_BYPASS | Bypass selection See Table 1-767. |
| 6 | PLD0_MC3_BYPASS | Bypass selection See Table 1-767. |
| 4 | PLD0_MC2_BYPASS | Bypass selection See Table 1-767. |
| 2 | PLD0_MC1_BYPASS | Bypass selection See Table 1-767. |
| 0 | PLD0_MC0_BYPASS | Bypass selection See Table 1-767. |

Table 1-767. Bit field encoding: BYPASS_ENUM

| Value | Name | Description |
|-------|---------------|----------------------|
| 1'b0 | REGISTER | Registered output |
| 1'b1 | COMBINATIONAL | Combinational output |

1.3.1178 B[0..3]_P[0..7]_U[0..1]_CFG0 CFG0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|---------------------------|
| B0_P0_U0_CFG0: 0x40010040 | B0_P0_U1_CFG0: 0x400100C0 |
| B0_P1_U0_CFG0: 0x40010240 | B0_P1_U1_CFG0: 0x400102C0 |
| B0_P2_U0_CFG0: 0x40010440 | B0_P2_U1_CFG0: 0x400104C0 |
| B0_P3_U0_CFG0: 0x40010640 | B0_P3_U1_CFG0: 0x400106C0 |
| B0_P4_U0_CFG0: 0x40010840 | B0_P4_U1_CFG0: 0x400108C0 |
| B0_P5_U0_CFG0: 0x40010A40 | B0_P5_U1_CFG0: 0x40010AC0 |
| B0_P6_U0_CFG0: 0x40010C40 | B0_P6_U1_CFG0: 0x40010CC0 |
| B0_P7_U0_CFG0: 0x40010E40 | B0_P7_U1_CFG0: 0x40010EC0 |
| B1_P2_U0_CFG0: 0x40011440 | B1_P2_U1_CFG0: 0x400114C0 |
| B1_P3_U0_CFG0: 0x40011640 | B1_P3_U1_CFG0: 0x400116C0 |
| B1_P4_U0_CFG0: 0x40011840 | B1_P4_U1_CFG0: 0x400118C0 |
| B1_P5_U0_CFG0: 0x40011A40 | B1_P5_U1_CFG0: 0x40011AC0 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---|---|------|---------|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | NA:0 | R/W:000 | | |
| HW Access | NA | R | | | NA | R | | |
| Name | | RAD1 | | | | RAD0 | | |

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Register Segment: 2

| Bits | Name | Description |
|------|-----------|---|
| 6:4 | RAD1[2:0] | Datapath Permutable Input Mux See Table 1-768. |
| 2:0 | RAD0[2:0] | Datapath Permutable Input Mux See Table 1-768. |

Table 1-768. Bit field encoding: DP_INPUT_MUX_ENUM

| Value | Name | Description |
|--------|----------|-----------------|
| 3'b000 | OFF | Input off |
| 3'b001 | DP_IN0 | Set to dp_in[0] |
| 3'b010 | DP_IN1 | Set to dp_in[1] |
| 3'b011 | DP_IN2 | Set to dp_in[2] |
| 3'b100 | DP_IN3 | Set to dp_in[3] |
| 3'b101 | DP_IN4 | Set to dp_in[4] |
| 3'b110 | DP_IN5 | Set to dp_in[5] |
| 3'b111 | RESERVED | Reserved |

1.3.1179 B[0..3]_P[0..7]_U[0..1]_CFG1 CFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|---------------------------|
| B0_P0_U0_CFG1: 0x40010041 | B0_P0_U1_CFG1: 0x400100C1 |
| B0_P1_U0_CFG1: 0x40010241 | B0_P1_U1_CFG1: 0x400102C1 |
| B0_P2_U0_CFG1: 0x40010441 | B0_P2_U1_CFG1: 0x400104C1 |
| B0_P3_U0_CFG1: 0x40010641 | B0_P3_U1_CFG1: 0x400106C1 |
| B0_P4_U0_CFG1: 0x40010841 | B0_P4_U1_CFG1: 0x400108C1 |
| B0_P5_U0_CFG1: 0x40010A41 | B0_P5_U1_CFG1: 0x40010AC1 |
| B0_P6_U0_CFG1: 0x40010C41 | B0_P6_U1_CFG1: 0x40010CC1 |
| B0_P7_U0_CFG1: 0x40010E41 | B0_P7_U1_CFG1: 0x40010EC1 |
| B1_P2_U0_CFG1: 0x40011441 | B1_P2_U1_CFG1: 0x400114C1 |
| B1_P3_U0_CFG1: 0x40011641 | B1_P3_U1_CFG1: 0x400116C1 |
| B1_P4_U0_CFG1: 0x40011841 | B1_P4_U1_CFG1: 0x400118C1 |
| B1_P5_U0_CFG1: 0x40011A41 | B1_P5_U1_CFG1: 0x40011AC1 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|---|---|
| SW Access:Reset | NA:00000 | | | | | R/W:000 | | |
| HW Access | NA | | | | | R | | |
| Name | | | | | | RAD2 | | |

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Register Segment: 2

| Bits | Name | Description |
|------|-----------|-------------------------------|
| 2:0 | RAD2[2:0] | Datapath Permutable Input Mux |

[See Table 1-769.](#)

Table 1-769. Bit field encoding: DP_INPUT_MUX_ENUM

| Value | Name | Description |
|--------|----------|-----------------|
| 3'b000 | OFF | Input off |
| 3'b001 | DP_IN0 | Set to dp_in[0] |
| 3'b010 | DP_IN1 | Set to dp_in[1] |
| 3'b011 | DP_IN2 | Set to dp_in[2] |
| 3'b100 | DP_IN3 | Set to dp_in[3] |
| 3'b101 | DP_IN4 | Set to dp_in[4] |
| 3'b110 | DP_IN5 | Set to dp_in[5] |
| 3'b111 | RESERVED | Reserved |

1.3.1180 B[0..3]_P[0..7]_U[0..1]_CFG2

CFG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|---------------------------|
| B0_P0_U0_CFG2: 0x40010042 | B0_P0_U1_CFG2: 0x400100C2 |
| B0_P1_U0_CFG2: 0x40010242 | B0_P1_U1_CFG2: 0x400102C2 |
| B0_P2_U0_CFG2: 0x40010442 | B0_P2_U1_CFG2: 0x400104C2 |
| B0_P3_U0_CFG2: 0x40010642 | B0_P3_U1_CFG2: 0x400106C2 |
| B0_P4_U0_CFG2: 0x40010842 | B0_P4_U1_CFG2: 0x400108C2 |
| B0_P5_U0_CFG2: 0x40010A42 | B0_P5_U1_CFG2: 0x40010AC2 |
| B0_P6_U0_CFG2: 0x40010C42 | B0_P6_U1_CFG2: 0x40010CC2 |
| B0_P7_U0_CFG2: 0x40010E42 | B0_P7_U1_CFG2: 0x40010EC2 |
| B1_P2_U0_CFG2: 0x40011442 | B1_P2_U1_CFG2: 0x400114C2 |
| B1_P3_U0_CFG2: 0x40011642 | B1_P3_U1_CFG2: 0x400116C2 |
| B1_P4_U0_CFG2: 0x40011842 | B1_P4_U1_CFG2: 0x400118C2 |
| B1_P5_U0_CFG2: 0x40011A42 | B1_P5_U1_CFG2: 0x40011AC2 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---|---|------|---------|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | NA:0 | R/W:000 | | |
| HW Access | NA | R | | | NA | R | | |
| Name | | F1_LD | | | | F0_LD | | |

Datapath Input Selection - F1_LD F0_LD. FIFO load strobes. When in input mode, the FIFO loads from the system bus. When in output mode, the FIFOs load from either the A0, A1 or the ALU

Register Segment: 2

| Bits | Name | Description |
|------|------------|---|
| 6:4 | F1_LD[2:0] | Datapath Permutable Input Mux See Table 1-770. |
| 2:0 | F0_LD[2:0] | Datapath Permutable Input Mux See Table 1-770. |

Table 1-770. Bit field encoding: DP_INPUT_MUX_ENUM

| Value | Name | Description |
|--------|--------|-----------------|
| 3'b000 | OFF | Input off |
| 3'b001 | DP_IN0 | Set to dp_in[0] |
| 3'b010 | DP_IN1 | Set to dp_in[1] |
| 3'b011 | DP_IN2 | Set to dp_in[2] |
| 3'b100 | DP_IN3 | Set to dp_in[3] |
| 3'b101 | DP_IN4 | Set to dp_in[4] |
| 3'b110 | DP_IN5 | Set to dp_in[5] |

1.3.1180 B[0..3]_P[0..7]_U[0..1]_CFG2 (continued)

Table 1-770. Bit field encoding: DP_INPUT_MUX_ENUM

| | | |
|--------|----------|----------|
| 3'b111 | RESERVED | Reserved |
|--------|----------|----------|

1.3.1181 B[0..3]_P[0..7]_U[0..1]_CFG3

CFG3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|---------------------------|
| B0_P0_U0_CFG3: 0x40010043 | B0_P0_U1_CFG3: 0x400100C3 |
| B0_P1_U0_CFG3: 0x40010243 | B0_P1_U1_CFG3: 0x400102C3 |
| B0_P2_U0_CFG3: 0x40010443 | B0_P2_U1_CFG3: 0x400104C3 |
| B0_P3_U0_CFG3: 0x40010643 | B0_P3_U1_CFG3: 0x400106C3 |
| B0_P4_U0_CFG3: 0x40010843 | B0_P4_U1_CFG3: 0x400108C3 |
| B0_P5_U0_CFG3: 0x40010A43 | B0_P5_U1_CFG3: 0x40010AC3 |
| B0_P6_U0_CFG3: 0x40010C43 | B0_P6_U1_CFG3: 0x40010CC3 |
| B0_P7_U0_CFG3: 0x40010E43 | B0_P7_U1_CFG3: 0x40010EC3 |
| B1_P2_U0_CFG3: 0x40011443 | B1_P2_U1_CFG3: 0x400114C3 |
| B1_P3_U0_CFG3: 0x40011643 | B1_P3_U1_CFG3: 0x400116C3 |
| B1_P4_U0_CFG3: 0x40011843 | B1_P4_U1_CFG3: 0x400118C3 |
| B1_P5_U0_CFG3: 0x40011A43 | B1_P5_U1_CFG3: 0x40011AC3 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---|---|------|---------|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | NA:0 | R/W:000 | | |
| HW Access | NA | R | | | NA | R | | |
| Name | | D1_LD | | | | D0_LD | | |

Datapath Input Selection - D1_LD D0_LD. Data Register load strobes. These are edge sensitive signals. On the positive edge, a byte is transferred from the associated FIFO to the Data Register.

Register Segment: 2

| Bits | Name | Description |
|------|------------|---|
| 6:4 | D1_LD[2:0] | Datapath Permutable Input Mux See Table 1-771. |
| 2:0 | D0_LD[2:0] | Datapath Permutable Input Mux See Table 1-771. |

Table 1-771. Bit field encoding: DP_INPUT_MUX_ENUM

| Value | Name | Description |
|--------|--------|-----------------|
| 3'b000 | OFF | Input off |
| 3'b001 | DP_IN0 | Set to dp_in[0] |
| 3'b010 | DP_IN1 | Set to dp_in[1] |
| 3'b011 | DP_IN2 | Set to dp_in[2] |
| 3'b100 | DP_IN3 | Set to dp_in[3] |
| 3'b101 | DP_IN4 | Set to dp_in[4] |
| 3'b110 | DP_IN5 | Set to dp_in[5] |

1.3.1181 B[0..3]_P[0..7]_U[0..1]_CFG3 (continued)

Table 1-771. Bit field encoding: DP_INPUT_MUX_ENUM

| | | |
|--------|----------|----------|
| 3'b111 | RESERVED | Reserved |
|--------|----------|----------|

1.3.1182 B[0..3]_P[0..7]_U[0..1]_CFG4

CFG4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|---------------------------|
| B0_P0_U0_CFG4: 0x40010044 | B0_P0_U1_CFG4: 0x400100C4 |
| B0_P1_U0_CFG4: 0x40010244 | B0_P1_U1_CFG4: 0x400102C4 |
| B0_P2_U0_CFG4: 0x40010444 | B0_P2_U1_CFG4: 0x400104C4 |
| B0_P3_U0_CFG4: 0x40010644 | B0_P3_U1_CFG4: 0x400106C4 |
| B0_P4_U0_CFG4: 0x40010844 | B0_P4_U1_CFG4: 0x400108C4 |
| B0_P5_U0_CFG4: 0x40010A44 | B0_P5_U1_CFG4: 0x40010AC4 |
| B0_P6_U0_CFG4: 0x40010C44 | B0_P6_U1_CFG4: 0x40010CC4 |
| B0_P7_U0_CFG4: 0x40010E44 | B0_P7_U1_CFG4: 0x40010EC4 |
| B1_P2_U0_CFG4: 0x40011444 | B1_P2_U1_CFG4: 0x400114C4 |
| B1_P3_U0_CFG4: 0x40011644 | B1_P3_U1_CFG4: 0x400116C4 |
| B1_P4_U0_CFG4: 0x40011844 | B1_P4_U1_CFG4: 0x400118C4 |
| B1_P5_U0_CFG4: 0x40011A44 | B1_P5_U1_CFG4: 0x40011AC4 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|---|---|------|---------|---|---|
| SW Access:Reset | NA:0 | R/W:000 | | | NA:0 | R/W:000 | | |
| HW Access | NA | R | | | NA | R | | |
| Name | | CI_MUX | | | | SI_MUX | | |

Datapath Input Selection - CI_MUX SI_MUX. Carry In data and Shift In data from routing

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 6:4 | CI_MUX[2:0] | Datapath Permutable Input Mux See Table 1-772. |
| 2:0 | SI_MUX[2:0] | Datapath Permutable Input Mux See Table 1-772. |

Table 1-772. Bit field encoding: DP_INPUT_MUX_ENUM

| Value | Name | Description |
|--------|----------|-----------------|
| 3'b000 | OFF | Input off |
| 3'b001 | DP_IN0 | Set to dp_in[0] |
| 3'b010 | DP_IN1 | Set to dp_in[1] |
| 3'b011 | DP_IN2 | Set to dp_in[2] |
| 3'b100 | DP_IN3 | Set to dp_in[3] |
| 3'b101 | DP_IN4 | Set to dp_in[4] |
| 3'b110 | DP_IN5 | Set to dp_in[5] |
| 3'b111 | RESERVED | Reserved |

1.3.1183 B[0..3]_P[0..7]_U[0..1]_CFG5

CFG5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|---------------------------|
| B0_P0_U0_CFG5: 0x40010045 | B0_P0_U1_CFG5: 0x400100C5 |
| B0_P1_U0_CFG5: 0x40010245 | B0_P1_U1_CFG5: 0x400102C5 |
| B0_P2_U0_CFG5: 0x40010445 | B0_P2_U1_CFG5: 0x400104C5 |
| B0_P3_U0_CFG5: 0x40010645 | B0_P3_U1_CFG5: 0x400106C5 |
| B0_P4_U0_CFG5: 0x40010845 | B0_P4_U1_CFG5: 0x400108C5 |
| B0_P5_U0_CFG5: 0x40010A45 | B0_P5_U1_CFG5: 0x40010AC5 |
| B0_P6_U0_CFG5: 0x40010C45 | B0_P6_U1_CFG5: 0x40010CC5 |
| B0_P7_U0_CFG5: 0x40010E45 | B0_P7_U1_CFG5: 0x40010EC5 |
| B1_P2_U0_CFG5: 0x40011445 | B1_P2_U1_CFG5: 0x400114C5 |
| B1_P3_U0_CFG5: 0x40011645 | B1_P3_U1_CFG5: 0x400116C5 |
| B1_P4_U0_CFG5: 0x40011845 | B1_P4_U1_CFG5: 0x400118C5 |
| B1_P5_U0_CFG5: 0x40011A45 | B1_P5_U1_CFG5: 0x40011AC5 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0000 | | | | R/W:0000 | | | |
| HW Access | R | | | | R | | | |
| Name | OUT1 | | | | OUT0 | | | |

Datapath Output Selection for OUT1 OUT0, a 1 of 16 select

Register Segment: 2

| Bits | Name | Description |
|------|-----------|---|
| 7:4 | OUT1[3:0] | Datapath Permutable Ouput Mux See Table 1-773. |
| 3:0 | OUT0[3:0] | Datapath Permutable Ouput Mux See Table 1-773. |

Table 1-773. Bit field encoding: DP_OUTPUT_MUX_ENUM

| Value | Name | Description |
|---------|--------|---------------------------|
| 4'b0000 | CE0 | Comparator 0 equal |
| 4'b0001 | CL0 | Comparator 0 less than |
| 4'b0010 | Z0 | Accumulator 0 zero detect |
| 4'b0011 | FF0 | Accumulator 0 ones detect |
| 4'b0100 | CE1 | Comparator 1 equal |
| 4'b0101 | CL1 | Comparator 1 less than |
| 4'b0110 | Z1 | Accumulator 1 zero detect |
| 4'b0111 | FF1 | Accumulator 1 ones detect |
| 4'b1000 | OV_MSB | Overflow of MSB |

@((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) +

1.3.1183 B[0..3]_P[0..7]_U[0..1]_CFG5 (continued)

Table 1-773. Bit field encoding: DP_OUTPUT_MUX_ENUM

| | | |
|---------|-------------|--|
| 4'b1001 | CO_MSB | Carry out of MSB |
| 4'b1010 | CMSBO | CRC MSB |
| 4'b1011 | SO | Shift out |
| 4'b1100 | F0_BLK_STAT | FIFO 0 block status defined by direction |
| 4'b1101 | F1_BLK_STAT | FIFO 1 block status defined by direction |
| 4'b1110 | F0_BUS_STAT | FIFO 0 bus status defined by direction and level |
| 4'b1111 | F1_BUS_STAT | FIFO 1 bus status defined by direction and level |

1.3.1184 B[0..3]_P[0..7]_U[0..1]_CFG6

CFG6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|---------------------------|
| B0_P0_U0_CFG6: 0x40010046 | B0_P0_U1_CFG6: 0x400100C6 |
| B0_P1_U0_CFG6: 0x40010246 | B0_P1_U1_CFG6: 0x400102C6 |
| B0_P2_U0_CFG6: 0x40010446 | B0_P2_U1_CFG6: 0x400104C6 |
| B0_P3_U0_CFG6: 0x40010646 | B0_P3_U1_CFG6: 0x400106C6 |
| B0_P4_U0_CFG6: 0x40010846 | B0_P4_U1_CFG6: 0x400108C6 |
| B0_P5_U0_CFG6: 0x40010A46 | B0_P5_U1_CFG6: 0x40010AC6 |
| B0_P6_U0_CFG6: 0x40010C46 | B0_P6_U1_CFG6: 0x40010CC6 |
| B0_P7_U0_CFG6: 0x40010E46 | B0_P7_U1_CFG6: 0x40010EC6 |
| B1_P2_U0_CFG6: 0x40011446 | B1_P2_U1_CFG6: 0x400114C6 |
| B1_P3_U0_CFG6: 0x40011646 | B1_P3_U1_CFG6: 0x400116C6 |
| B1_P4_U0_CFG6: 0x40011846 | B1_P4_U1_CFG6: 0x400118C6 |
| B1_P5_U0_CFG6: 0x40011A46 | B1_P5_U1_CFG6: 0x40011AC6 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0000 | | | | R/W:0000 | | | |
| HW Access | R | | | | R | | | |
| Name | OUT3 | | | | OUT2 | | | |

Datapath Output Selection for OUT3 OUT2, a 1 of 16 select

Register Segment: 2

| Bits | Name | Description |
|------|-----------|---|
| 7:4 | OUT3[3:0] | Datapath Permutable Ouput Mux See Table 1-774. |
| 3:0 | OUT2[3:0] | Datapath Permutable Ouput Mux See Table 1-774. |

Table 1-774. Bit field encoding: DP_OUTPUT_MUX_ENUM

| Value | Name | Description |
|---------|--------|---------------------------|
| 4'b0000 | CE0 | Comparator 0 equal |
| 4'b0001 | CL0 | Comparator 0 less than |
| 4'b0010 | Z0 | Accumulator 0 zero detect |
| 4'b0011 | FF0 | Accumulator 0 ones detect |
| 4'b0100 | CE1 | Comparator 1 equal |
| 4'b0101 | CL1 | Comparator 1 less than |
| 4'b0110 | Z1 | Accumulator 1 zero detect |
| 4'b0111 | FF1 | Accumulator 1 ones detect |
| 4'b1000 | OV_MSB | Overflow of MSB |

@((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) +

1.3.1184 B[0..3]_P[0..7]_U[0..1]_CFG6 (continued)

Table 1-774. Bit field encoding: DP_OUTPUT_MUX_ENUM

| | | |
|---------|-------------|--|
| 4'b1001 | CO_MSB | Carry out of MSB |
| 4'b1010 | CMSBO | CRC MSB |
| 4'b1011 | SO | Shift out |
| 4'b1100 | F0_BLK_STAT | FIFO 0 block status defined by direction |
| 4'b1101 | F1_BLK_STAT | FIFO 1 block status defined by direction |
| 4'b1110 | F0_BUS_STAT | FIFO 0 bus status defined by direction and level |
| 4'b1111 | F1_BUS_STAT | FIFO 1 bus status defined by direction and level |

1.3.1185 B[0..3]_P[0..7]_U[0..1]_CFG7 CFG7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|---------------------------|
| B0_P0_U0_CFG7: 0x40010047 | B0_P0_U1_CFG7: 0x400100C7 |
| B0_P1_U0_CFG7: 0x40010247 | B0_P1_U1_CFG7: 0x400102C7 |
| B0_P2_U0_CFG7: 0x40010447 | B0_P2_U1_CFG7: 0x400104C7 |
| B0_P3_U0_CFG7: 0x40010647 | B0_P3_U1_CFG7: 0x400106C7 |
| B0_P4_U0_CFG7: 0x40010847 | B0_P4_U1_CFG7: 0x400108C7 |
| B0_P5_U0_CFG7: 0x40010A47 | B0_P5_U1_CFG7: 0x40010AC7 |
| B0_P6_U0_CFG7: 0x40010C47 | B0_P6_U1_CFG7: 0x40010CC7 |
| B0_P7_U0_CFG7: 0x40010E47 | B0_P7_U1_CFG7: 0x40010EC7 |
| B1_P2_U0_CFG7: 0x40011447 | B1_P2_U1_CFG7: 0x400114C7 |
| B1_P3_U0_CFG7: 0x40011647 | B1_P3_U1_CFG7: 0x400116C7 |
| B1_P4_U0_CFG7: 0x40011847 | B1_P4_U1_CFG7: 0x400118C7 |
| B1_P5_U0_CFG7: 0x40011A47 | B1_P5_U1_CFG7: 0x40011AC7 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:0000 | | | | R/W:0000 | | | |
| HW Access | R | | | | R | | | |
| Name | OUT5 | | | | OUT4 | | | |

Datapath Output Selection for OUT5 OUT4, a 1 of 16 select

Register Segment: 2

| Bits | Name | Description |
|------|-----------|--|
| 7:4 | OUT5[3:0] | Datapath Permutable Output Mux See Table 1-775. |
| 3:0 | OUT4[3:0] | Datapath Permutable Output Mux See Table 1-775. |

Table 1-775. Bit field encoding: DP_OUTPUT_MUX_ENUM

| Value | Name | Description |
|---------|--------|---------------------------|
| 4'b0000 | CE0 | Comparator 0 equal |
| 4'b0001 | CL0 | Comparator 0 less than |
| 4'b0010 | Z0 | Accumulator 0 zero detect |
| 4'b0011 | FF0 | Accumulator 0 ones detect |
| 4'b0100 | CE1 | Comparator 1 equal |
| 4'b0101 | CL1 | Comparator 1 less than |
| 4'b0110 | Z1 | Accumulator 1 zero detect |
| 4'b0111 | FF1 | Accumulator 1 ones detect |
| 4'b1000 | OV_MSB | Overflow of MSB |

1.3.1185 B[0..3]_P[0..7]_U[0..1]_CFG7 (continued)

Table 1-775. Bit field encoding: DP_OUTPUT_MUX_ENUM

| | | |
|---------|-------------|--|
| 4'b1001 | CO_MSB | Carry out of MSB |
| 4'b1010 | CMSBO | CRC MSB |
| 4'b1011 | SO | Shift out |
| 4'b1100 | F0_BLK_STAT | FIFO 0 block status defined by direction |
| 4'b1101 | F1_BLK_STAT | FIFO 1 block status defined by direction |
| 4'b1110 | F0_BUS_STAT | FIFO 0 bus status defined by direction and level |
| 4'b1111 | F1_BUS_STAT | FIFO 1 bus status defined by direction and level |

1.3.1186 B[0..3]_P[0..7]_U[0..1]_CFG8

CFG8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|---------------------------|
| B0_P0_U0_CFG8: 0x40010048 | B0_P0_U1_CFG8: 0x400100C8 |
| B0_P1_U0_CFG8: 0x40010248 | B0_P1_U1_CFG8: 0x400102C8 |
| B0_P2_U0_CFG8: 0x40010448 | B0_P2_U1_CFG8: 0x400104C8 |
| B0_P3_U0_CFG8: 0x40010648 | B0_P3_U1_CFG8: 0x400106C8 |
| B0_P4_U0_CFG8: 0x40010848 | B0_P4_U1_CFG8: 0x400108C8 |
| B0_P5_U0_CFG8: 0x40010A48 | B0_P5_U1_CFG8: 0x40010AC8 |
| B0_P6_U0_CFG8: 0x40010C48 | B0_P6_U1_CFG8: 0x40010CC8 |
| B0_P7_U0_CFG8: 0x40010E48 | B0_P7_U1_CFG8: 0x40010EC8 |
| B1_P2_U0_CFG8: 0x40011448 | B1_P2_U1_CFG8: 0x400114C8 |
| B1_P3_U0_CFG8: 0x40011648 | B1_P3_U1_CFG8: 0x400116C8 |
| B1_P4_U0_CFG8: 0x40011848 | B1_P4_U1_CFG8: 0x400118C8 |
| B1_P5_U0_CFG8: 0x40011A48 | B1_P5_U1_CFG8: 0x40011AC8 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|---|---|---|---|---|
| SW Access:Reset | NA:00 | | R/W:000000 | | | | | |
| HW Access | NA | | R | | | | | |
| Name | | | OUT_SYNC | | | | | |

Datapath Output Synchronization Option

Register Segment: 2

| Bits | Name | Description |
|------|---------------|---|
| 5:0 | OUT_SYNC[5:0] | Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) |

1.3.1187 B[0..3]_P[0..7]_U[0..1]_CFG9 CFG9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|---------------------------|---------------------------|
| B0_P0_U0_CFG9: 0x40010049 | B0_P0_U1_CFG9: 0x400100C9 |
| B0_P1_U0_CFG9: 0x40010249 | B0_P1_U1_CFG9: 0x400102C9 |
| B0_P2_U0_CFG9: 0x40010449 | B0_P2_U1_CFG9: 0x400104C9 |
| B0_P3_U0_CFG9: 0x40010649 | B0_P3_U1_CFG9: 0x400106C9 |
| B0_P4_U0_CFG9: 0x40010849 | B0_P4_U1_CFG9: 0x400108C9 |
| B0_P5_U0_CFG9: 0x40010A49 | B0_P5_U1_CFG9: 0x40010AC9 |
| B0_P6_U0_CFG9: 0x40010C49 | B0_P6_U1_CFG9: 0x40010CC9 |
| B0_P7_U0_CFG9: 0x40010E49 | B0_P7_U1_CFG9: 0x40010EC9 |
| B1_P2_U0_CFG9: 0x40011449 | B1_P2_U1_CFG9: 0x400114C9 |
| B1_P3_U0_CFG9: 0x40011649 | B1_P3_U1_CFG9: 0x400116C9 |
| B1_P4_U0_CFG9: 0x40011849 | B1_P4_U1_CFG9: 0x400118C9 |
| B1_P5_U0_CFG9: 0x40011A49 | B1_P5_U1_CFG9: 0x40011AC9 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | AMASK | | | | | | | |

Datapath ALU Mask

Register Segment: 2

| Bits | Name | Description |
|------|------------|--|
| 7:0 | AMASK[7:0] | Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational. |

1.3.1188 B[0..3]_P[0..7]_U[0..1]_CFG10 CFG10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG10: 0x4001004A | B0_P0_U1_CFG10: 0x400100CA |
| B0_P1_U0_CFG10: 0x4001024A | B0_P1_U1_CFG10: 0x400102CA |
| B0_P2_U0_CFG10: 0x4001044A | B0_P2_U1_CFG10: 0x400104CA |
| B0_P3_U0_CFG10: 0x4001064A | B0_P3_U1_CFG10: 0x400106CA |
| B0_P4_U0_CFG10: 0x4001084A | B0_P4_U1_CFG10: 0x400108CA |
| B0_P5_U0_CFG10: 0x40010A4A | B0_P5_U1_CFG10: 0x40010ACA |
| B0_P6_U0_CFG10: 0x40010C4A | B0_P6_U1_CFG10: 0x40010CCA |
| B0_P7_U0_CFG10: 0x40010E4A | B0_P7_U1_CFG10: 0x40010ECA |
| B1_P2_U0_CFG10: 0x4001144A | B1_P2_U1_CFG10: 0x400114CA |
| B1_P3_U0_CFG10: 0x4001164A | B1_P3_U1_CFG10: 0x400116CA |
| B1_P4_U0_CFG10: 0x4001184A | B1_P4_U1_CFG10: 0x400118CA |
| B1_P5_U0_CFG10: 0x40011A4A | B1_P5_U1_CFG10: 0x40011ACA |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CMASK0 | | | | | | | |

Datapath Compare 0 Mask

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | CMASK0[7:0] | Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational. |

1.3.1189 B[0..3]_P[0..7]_U[0..1]_CFG11 CFG11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG11: 0x4001004B | B0_P0_U1_CFG11: 0x400100CB |
| B0_P1_U0_CFG11: 0x4001024B | B0_P1_U1_CFG11: 0x400102CB |
| B0_P2_U0_CFG11: 0x4001044B | B0_P2_U1_CFG11: 0x400104CB |
| B0_P3_U0_CFG11: 0x4001064B | B0_P3_U1_CFG11: 0x400106CB |
| B0_P4_U0_CFG11: 0x4001084B | B0_P4_U1_CFG11: 0x400108CB |
| B0_P5_U0_CFG11: 0x40010A4B | B0_P5_U1_CFG11: 0x40010ACB |
| B0_P6_U0_CFG11: 0x40010C4B | B0_P6_U1_CFG11: 0x40010CCB |
| B0_P7_U0_CFG11: 0x40010E4B | B0_P7_U1_CFG11: 0x40010ECB |
| B1_P2_U0_CFG11: 0x4001144B | B1_P2_U1_CFG11: 0x400114CB |
| B1_P3_U0_CFG11: 0x4001164B | B1_P3_U1_CFG11: 0x400116CB |
| B1_P4_U0_CFG11: 0x4001184B | B1_P4_U1_CFG11: 0x400118CB |
| B1_P5_U0_CFG11: 0x40011A4B | B1_P5_U1_CFG11: 0x40011ACB |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CMASK1 | | | | | | | |

Datapath Compare 1 Mask

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:0 | CMASK1[7:0] | Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational. |

1.3.1190 B[0..3]_P[0..7]_U[0..1]_CFG12

CFG12

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG12: 0x4001004C | B0_P0_U1_CFG12: 0x400100CC |
| B0_P1_U0_CFG12: 0x4001024C | B0_P1_U1_CFG12: 0x400102CC |
| B0_P2_U0_CFG12: 0x4001044C | B0_P2_U1_CFG12: 0x400104CC |
| B0_P3_U0_CFG12: 0x4001064C | B0_P3_U1_CFG12: 0x400106CC |
| B0_P4_U0_CFG12: 0x4001084C | B0_P4_U1_CFG12: 0x400108CC |
| B0_P5_U0_CFG12: 0x40010A4C | B0_P5_U1_CFG12: 0x40010ACC |
| B0_P6_U0_CFG12: 0x40010C4C | B0_P6_U1_CFG12: 0x40010CCC |
| B0_P7_U0_CFG12: 0x40010E4C | B0_P7_U1_CFG12: 0x40010ECC |
| B1_P2_U0_CFG12: 0x4001144C | B1_P2_U1_CFG12: 0x400114CC |
| B1_P3_U0_CFG12: 0x4001164C | B1_P3_U1_CFG12: 0x400116CC |
| B1_P4_U0_CFG12: 0x4001184C | B1_P4_U1_CFG12: 0x400118CC |
| B1_P5_U0_CFG12: 0x40011A4C | B1_P5_U1_CFG12: 0x40011ACC |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|-----------|----------|--------|---------|---|---------|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | | R/W:00 | |
| HW Access | R | R | R | R | R | | R | |
| Name | CMASK1_EN | CMASK0_EN | AMASK_EN | DEF_SI | SI_SELB | | SI_SELA | |

Datapath mask enables and shift in configuration

Register Segment: 2

| Bits | Name | Description |
|------|--------------|---|
| 7 | CMASK1_EN | Datapath mask enable See Table 1-777. |
| 6 | CMASK0_EN | Datapath mask enable See Table 1-777. |
| 5 | AMASK_EN | Datapath mask enable See Table 1-777. |
| 4 | DEF_SI | Datapath default shift value See Table 1-776. |
| 3:2 | SI_SELB[1:0] | Datapath shift in source select See Table 1-778. |

```
@((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) +
```

1.3.1190 B[0..3]_P[0..7]_U[0..1]_CFG12 (continued)

1:0 SI_SEL[1:0] Datapath shift in source select

[See Table 1-778.](#)

Table 1-776. Bit field encoding: DEF_SHIFT_ENUM

| Value | Name | Description |
|-------|-----------|--------------------|
| 1'b0 | DEFAULT_0 | Default shift is 0 |
| 1'b1 | DEFAULT_1 | Default shift is 1 |

Table 1-777. Bit field encoding: MASK_ENABLE_ENUM

| Value | Name | Description |
|-------|---------|------------------|
| 1'b0 | DISABLE | Masking disabled |
| 1'b1 | ENABLE | Masking enabled |

Table 1-778. Bit field encoding: SI_SEL_ENUM

| Value | Name | Description |
|-------|------------|--|
| 2'b00 | DEFAULT | Default value specified in default shift field |
| 2'b01 | REGISTERED | Shift in is the shift out registered from previous cycle |
| 2'b10 | ROUTE | Shift in is selected from datapath routing input |
| 2'b11 | CHAIN | Shift in is chained from the previous datapath |

1.3.1191 B[0..3]_P[0..7]_U[0..1]_CFG13

CFG13

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG13: 0x4001004D | B0_P0_U1_CFG13: 0x400100CD |
| B0_P1_U0_CFG13: 0x4001024D | B0_P1_U1_CFG13: 0x400102CD |
| B0_P2_U0_CFG13: 0x4001044D | B0_P2_U1_CFG13: 0x400104CD |
| B0_P3_U0_CFG13: 0x4001064D | B0_P3_U1_CFG13: 0x400106CD |
| B0_P4_U0_CFG13: 0x4001084D | B0_P4_U1_CFG13: 0x400108CD |
| B0_P5_U0_CFG13: 0x40010A4D | B0_P5_U1_CFG13: 0x40010ACD |
| B0_P6_U0_CFG13: 0x40010C4D | B0_P6_U1_CFG13: 0x40010CCD |
| B0_P7_U0_CFG13: 0x40010E4D | B0_P7_U1_CFG13: 0x40010ECD |
| B1_P2_U0_CFG13: 0x4001144D | B1_P2_U1_CFG13: 0x400114CD |
| B1_P3_U0_CFG13: 0x4001164D | B1_P3_U1_CFG13: 0x400116CD |
| B1_P4_U0_CFG13: 0x4001184D | B1_P4_U1_CFG13: 0x400118CD |
| B1_P5_U0_CFG13: 0x40011A4D | B1_P5_U1_CFG13: 0x40011ACD |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|----------|---|---------|---|---------|---|
| SW Access:Reset | R/W:00 | | R/W:00 | | R/W:00 | | R/W:00 | |
| HW Access | R | | R | | R | | R | |
| Name | CMP_SELB | | CMP_SELA | | CI_SELB | | CI_SELA | |

Datapath carry in and compare configuration

Register Segment: 2

| Bits | Name | Description |
|------|---------------|---|
| 7:6 | CMP_SELB[1:0] | Datapath compare select See Table 1-780. |
| 5:4 | CMP_SELA[1:0] | Datapath compare select See Table 1-780. |
| 3:2 | CI_SELB[1:0] | Datapath carry in source select See Table 1-779. |
| 1:0 | CI_SELA[1:0] | Datapath carry in source select See Table 1-779. |

Table 1-779. Bit field encoding: CI_SEL_ENUM

| Value | Name | Description |
|-------|------------|--|
| 2'b00 | DEFAULT | Default arithmetic mode |
| 2'b01 | REGISTERED | Carry in is the carry out registered from previous cycle |

@((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) +

1.3.1191 B[0..3]_P[0..7]_U[0..1]_CFG13 (continued)

Table 1-779. Bit field encoding: CI_SEL_ENUM

| | | |
|-------|-------|--|
| 2'b10 | ROUTE | Carry in is selected from datapath routing input |
| 2'b11 | CHAIN | Carry in is chained from the previous datapath |

Table 1-780. Bit field encoding: CMP_SEL_ENUM

| Value | Name | Description |
|-------|-------|------------------|
| 2'b00 | A1_D1 | Compare A1 to D1 |
| 2'b01 | A1_A0 | Compare A1 to A0 |
| 2'b10 | A0_D1 | Compare A0 to D1 |
| 2'b11 | A0_A0 | Compare A0 to A0 |

1.3.1192 B[0..3]_P[0..7]_U[0..1]_CFG14

CFG14

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG14: 0x4001004E | B0_P0_U1_CFG14: 0x400100CE |
| B0_P1_U0_CFG14: 0x4001024E | B0_P1_U1_CFG14: 0x400102CE |
| B0_P2_U0_CFG14: 0x4001044E | B0_P2_U1_CFG14: 0x400104CE |
| B0_P3_U0_CFG14: 0x4001064E | B0_P3_U1_CFG14: 0x400106CE |
| B0_P4_U0_CFG14: 0x4001084E | B0_P4_U1_CFG14: 0x400108CE |
| B0_P5_U0_CFG14: 0x40010A4E | B0_P5_U1_CFG14: 0x40010ACE |
| B0_P6_U0_CFG14: 0x40010C4E | B0_P6_U1_CFG14: 0x40010CCE |
| B0_P7_U0_CFG14: 0x40010E4E | B0_P7_U1_CFG14: 0x40010ECE |
| B1_P2_U0_CFG14: 0x4001144E | B1_P2_U1_CFG14: 0x400114CE |
| B1_P3_U0_CFG14: 0x4001164E | B1_P3_U1_CFG14: 0x400116CE |
| B1_P4_U0_CFG14: 0x4001184E | B1_P4_U1_CFG14: 0x400118CE |
| B1_P5_U0_CFG14: 0x40011A4E | B1_P5_U1_CFG14: 0x40011ACE |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---------|---|---|------------|----------|--------|--------|
| SW Access:Reset | R/W:0 | R/W:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | | | R | R | R | R |
| Name | MSB_EN | MSB_SEL | | | CHAIN_CMSB | CHAIN_FB | CHAIN1 | CHAIN0 |

Datapath chaining and MSB configuration

Register Segment: 2

| Bits | Name | Description |
|------|--------------|---|
| 7 | MSB_EN | Datapath MSB selection enable See Table 1-784. |
| 6:4 | MSB_SEL[2:0] | Datapath MSB Selection See Table 1-785. |
| 3 | CHAIN_CMSB | Datapath CRC MSB chaining enable See Table 1-781. |
| 2 | CHAIN_FB | Datapath CRC feedback chaining enable See Table 1-783. |
| 1 | CHAIN1 | Datapath condition chaining enable See Table 1-782. |

@((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) +

1.3.1192 B[0..3]_P[0..7]_U[0..1]_CFG14 (continued)

0 CHAIN0 Datapath condition chaining enable

[See Table 1-782.](#)

Table 1-781. Bit field encoding: CHAIN_CMSB_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | CRC MSB is not chained |
| 1'b1 | ENABLE | CRC MSB is chained from the next (MSB) datapath |

Table 1-782. Bit field encoding: CHAIN_EN_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Conditions are not chained |
| 1'b1 | ENABLE | Conditions are chained from the previous (LSB) datapath |

Table 1-783. Bit field encoding: CHAIN_FB_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | CRC feedback is not chained |
| 1'b1 | ENABLE | CRC feedback is chained from the previous (LSB) datapath |

Table 1-784. Bit field encoding: MSB_EN_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | MSB selection is disabled, MSB is bit 7 |
| 1'b1 | ENABLE | MSB selection is controlled by MSB_SEL |

Table 1-785. Bit field encoding: MSB_SEL_ENUM

| Value | Name | Description |
|--------|------|---|
| 3'b000 | BIT0 | MSB is bit 0 |
| 3'b001 | BIT1 | MSB is bit 1 |
| 3'b010 | BIT2 | MSB is bit 2 |
| 3'b011 | BIT3 | MSB is bit 3 |
| 3'b100 | BIT4 | MSB is bit 4 |
| 3'b101 | BIT5 | MSB is bit 5 |
| 3'b110 | BIT6 | MSB is bit 6 |
| 3'b111 | BIT7 | MSB is bit 7 - equivalent to MSB EN = 0 |

1.3.1193 B[0..3]_P[0..7]_U[0..1]_CFG15

CFG15

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG15: 0x4001004F | B0_P0_U1_CFG15: 0x400100CF |
| B0_P1_U0_CFG15: 0x4001024F | B0_P1_U1_CFG15: 0x400102CF |
| B0_P2_U0_CFG15: 0x4001044F | B0_P2_U1_CFG15: 0x400104CF |
| B0_P3_U0_CFG15: 0x4001064F | B0_P3_U1_CFG15: 0x400106CF |
| B0_P4_U0_CFG15: 0x4001084F | B0_P4_U1_CFG15: 0x400108CF |
| B0_P5_U0_CFG15: 0x40010A4F | B0_P5_U1_CFG15: 0x40010ACF |
| B0_P6_U0_CFG15: 0x40010C4F | B0_P6_U1_CFG15: 0x40010CCF |
| B0_P7_U0_CFG15: 0x40010E4F | B0_P7_U1_CFG15: 0x40010ECF |
| B1_P2_U0_CFG15: 0x4001144F | B1_P2_U1_CFG15: 0x400114CF |
| B1_P3_U0_CFG15: 0x4001164F | B1_P3_U1_CFG15: 0x400116CF |
| B1_P4_U0_CFG15: 0x4001184F | B1_P4_U1_CFG15: 0x400118CF |
| B1_P5_U0_CFG15: 0x40011A4F | B1_P5_U1_CFG15: 0x40011ACF |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|-----------|--------|--------|----------|---|----------|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | | R/W:00 | |
| HW Access | R | R | R | R | R | | R | |
| Name | PI_SEL | SHIFT_SEL | PI_DYN | MSB_SI | F1_INSEL | | F0_INSEL | |

Datapath FIFO, shift and parallel input control

Register Segment: 2

| Bits | Name | Description |
|------|---------------|---|
| 7 | PI_SEL | Datapath parallel input selection See Table 1-789. |
| 6 | SHIFT_SEL | Datapath shift out selection See Table 1-790. |
| 5 | PI_DYN | Enable for dynamic control of parallel data input (PI) mux. See Table 1-788. |
| 4 | MSB_SI | Arithmetic shift right operation shift in selection See Table 1-787. |
| 3:2 | F1_INSEL[1:0] | Datapath FIFO Configuration See Table 1-786. |

```
@((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) +
```

1.3.1193 B[0..3]_P[0..7]_U[0..1]_CFG15 (continued)

1:0 F0_INSEL[1:0] Datapath FIFO Configuration

[See Table 1-786.](#)

Table 1-786. Bit field encoding: FIFO_CFG_ENUM

| Value | Name | Description |
|-------|------------|--|
| 2'b00 | INPUT | Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator |
| 2'b01 | OUTPUT_A0 | Output Mode: Write source is A0, read destination is the system bus |
| 2'b10 | OUTPUT_A1 | Output Mode: Write source is A1, read destination is the system bus |
| 2'b11 | OUTPUT_ALU | Output Mode: Write source is the ALU output, read destination is the system bus |

Table 1-787. Bit field encoding: MSB_SI_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DEFAULT | Shift in default value (when SI_SELA and/or SI_SELB == 0) |
| 1'b1 | MSB | Override default and shift in MSB value |

Table 1-788. Bit field encoding: PI_DYN_ENUM

| Value | Name | Description |
|-------|----------|--|
| 1'b0 | DISABLED | Parallel input mux select is only controlled by static configuration (PI_SEL). |
| 1'b1 | ENABLED | Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled. |

Table 1-789. Bit field encoding: PI_SEL_ENUM

| Value | Name | Description |
|-------|----------|--|
| 1'b0 | NORMAL | Normal operation, ALU source is from accumulator selection |
| 1'b1 | PARALLEL | ALU source A input is from the parallel data input |

Table 1-790. Bit field encoding: SHIFT_SEL_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | SOL_MSB | Routed shift out is shift out left (sol_msb) |
| 1'b1 | SOR | Routed shift out is shift out right (sor) |

1.3.1194 B[0..3]_P[0..7]_U[0..1]_CFG16

CFG16

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG16: 0x40010050 | B0_P0_U1_CFG16: 0x400100D0 |
| B0_P1_U0_CFG16: 0x40010250 | B0_P1_U1_CFG16: 0x400102D0 |
| B0_P2_U0_CFG16: 0x40010450 | B0_P2_U1_CFG16: 0x400104D0 |
| B0_P3_U0_CFG16: 0x40010650 | B0_P3_U1_CFG16: 0x400106D0 |
| B0_P4_U0_CFG16: 0x40010850 | B0_P4_U1_CFG16: 0x400108D0 |
| B0_P5_U0_CFG16: 0x40010A50 | B0_P5_U1_CFG16: 0x40010AD0 |
| B0_P6_U0_CFG16: 0x40010C50 | B0_P6_U1_CFG16: 0x40010CD0 |
| B0_P7_U0_CFG16: 0x40010E50 | B0_P7_U1_CFG16: 0x40010ED0 |
| B1_P2_U0_CFG16: 0x40011450 | B1_P2_U1_CFG16: 0x400114D0 |
| B1_P3_U0_CFG16: 0x40011650 | B1_P3_U1_CFG16: 0x400116D0 |
| B1_P4_U0_CFG16: 0x40011850 | B1_P4_U1_CFG16: 0x400118D0 |
| B1_P5_U0_CFG16: 0x40011A50 | B1_P5_U1_CFG16: 0x40011AD0 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|-----------|-----------|----------|-----------|------------|-------------|--------------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | F1_CK_INV | F0_CK_INV | FIFO_FAST | FIFO_CAP | FIFO_EDGE | FIFO_ASYNC | EXT_CRCP_RS | WRK16_CONCAT |

Datapath FIFO and register access configuration control

Register Segment: 2

| Bits | Name | Description |
|------|-----------|---|
| 7 | F1_CK_INV | FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. See Table 1-794. |
| 6 | F0_CK_INV | FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. See Table 1-794. |
| 5 | FIFO_FAST | FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. See Table 1-796. |

```
@((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) +
```

1.3.1194 B[0..3]_P[0..7]_U[0..1]_CFG16 (continued)

| | | |
|---|--------------|---|
| 4 | FIFO_CAP | FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are captured. Captured data may be read immediately from the FIFO. Only applies to FIFOs configured in output mode. See Table 1-793. |
| 3 | FIFO_EDGE | Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode See Table 1-795. |
| 2 | FIFO_ASYNC | Asynchronous FIFO clocking support See Table 1-792. |
| 1 | EXT_CRCPRS | External CRC/PRS mode See Table 1-791. |
| 0 | WRK16_CONCAT | Datapath register access mode See Table 1-797. |

Table 1-791. Bit field encoding: EXT_CRCPRS_ENUM

| Value | Name | Description |
|-------|----------|--------------------------|
| 1'b0 | INTERNAL | Internal CRC/PRS routing |
| 1'b1 | EXTERNAL | External CRC/PRS routing |

Table 1-792. Bit field encoding: FIFO_ASYNC_ENUM

| Value | Name | Description |
|-------|----------|------------------------------|
| 1'b0 | DISABLED | FIFO clocks are synchronous |
| 1'b1 | ENABLED | FIFO clocks are asynchronous |

Table 1-793. Bit field encoding: FIFO_CAP_ENUM

| Value | Name | Description |
|-------|----------|---|
| 1'b0 | DISABLED | FIFO capture is disabled. |
| 1'b1 | ENABLED | FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1. |

Table 1-794. Bit field encoding: FIFO_CK_INV_ENUM

| Value | Name | Description |
|-------|----------|--|
| 1'b0 | NORMAL | FIFO clock is the same polarity as the Datapath clock. |
| 1'b1 | INVERTED | FIFO clock is inverted with respect to the Datapath clock. |

Table 1-795. Bit field encoding: FIFO_EDGE_ENUM

| Value | Name | Description |
|-------|-------|---|
| 1'b0 | LEVEL | FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge. |
| 1'b1 | EDGE | FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge following a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be detected. |

Table 1-796. Bit field encoding: FIFO_FAST_ENUM

| Value | Name | Description |
|-------|----------|---|
| 1'b0 | DISABLED | FIFO is clocked with selected Datapath clock. |
| 1'b1 | ENABLED | FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled. |

Table 1-797. Bit field encoding: WRK16_SEL_ENUM

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1194 B[0..3]_P[0..7]_U[0..1]_CFG16 (continued)

Table 1-797. Bit field encoding: WRK16_SEL_ENUM

| | | |
|------|-------------|---|
| 1'b0 | DEFAULT | 16-bit default access mode: selects registers in two consecutive UDBs in chaining order |
| 1'b1 | CONCATENATE | 16-bit concat access mode: selects concatenated registers in a single UDB |

1.3.1195 B[0..3]_P[0..7]_U[0..1]_CFG17 CFG17

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG17: 0x40010051 | B0_P0_U1_CFG17: 0x400100D1 |
| B0_P1_U0_CFG17: 0x40010251 | B0_P1_U1_CFG17: 0x400102D1 |
| B0_P2_U0_CFG17: 0x40010451 | B0_P2_U1_CFG17: 0x400104D1 |
| B0_P3_U0_CFG17: 0x40010651 | B0_P3_U1_CFG17: 0x400106D1 |
| B0_P4_U0_CFG17: 0x40010851 | B0_P4_U1_CFG17: 0x400108D1 |
| B0_P5_U0_CFG17: 0x40010A51 | B0_P5_U1_CFG17: 0x40010AD1 |
| B0_P6_U0_CFG17: 0x40010C51 | B0_P6_U1_CFG17: 0x40010CD1 |
| B0_P7_U0_CFG17: 0x40010E51 | B0_P7_U1_CFG17: 0x40010ED1 |
| B1_P2_U0_CFG17: 0x40011451 | B1_P2_U1_CFG17: 0x400114D1 |
| B1_P3_U0_CFG17: 0x40011651 | B1_P3_U1_CFG17: 0x400116D1 |
| B1_P4_U0_CFG17: 0x40011851 | B1_P4_U1_CFG17: 0x400118D1 |
| B1_P5_U0_CFG17: 0x40011A51 | B1_P5_U1_CFG17: 0x40011AD1 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|---------------|-------|-------|--------|--------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R | R | R | R | R |
| Name | | | | FIFO_ADD_SYNC | NC1 | NC0 | F1_DYN | F0_DYN |

Datapath FIFO control

Register Segment: 2

| Bits | Name | Description |
|------|---------------|--|
| 4 | FIFO_ADD_SYNC | Adds an additional sync flip-flop to FIFO block status. See Table 1-798. |
| 3 | NC1 | Spare register bit |
| 2 | NC0 | Spare register bit |
| 1 | F1_DYN | When this bit is set, the associated FIFO configuration may be dynamically controlled. See Table 1-799. |
| 0 | F0_DYN | When this bit is set, the associated FIFO configuration may be dynamically controlled. See Table 1-799. |

Table 1-798. Bit field encoding: FIFO_ADD_SYNC_ENUM

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1195 B[0..3]_P[0..7]_U[0..1]_CFG17 (continued)

Table 1-798. Bit field encoding: FIFO_ADD_SYNC_ENUM

| | | |
|------|----------|--|
| 1'b0 | DISABLED | Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1) |
| 1'b1 | ENABLED | Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1) |

Table 1-799. Bit field encoding: FIFO_DYN_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | STATIC | Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). |
| 1'b1 | DYNAMIC | The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (destination path from Fx_INSEL bits). When the 'dx_load' signal is '1', the access is external, where the CPU can both write and read the FIFO. When dynamic mode is activated, the dx_load signals are disabled for use as Data Register load signals. |

1.3.1196 B[0..3]_P[0..7]_U[0..1]_CFG18 CFG18

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG18: 0x40010052 | B0_P0_U1_CFG18: 0x400100D2 |
| B0_P1_U0_CFG18: 0x40010252 | B0_P1_U1_CFG18: 0x400102D2 |
| B0_P2_U0_CFG18: 0x40010452 | B0_P2_U1_CFG18: 0x400104D2 |
| B0_P3_U0_CFG18: 0x40010652 | B0_P3_U1_CFG18: 0x400106D2 |
| B0_P4_U0_CFG18: 0x40010852 | B0_P4_U1_CFG18: 0x400108D2 |
| B0_P5_U0_CFG18: 0x40010A52 | B0_P5_U1_CFG18: 0x40010AD2 |
| B0_P6_U0_CFG18: 0x40010C52 | B0_P6_U1_CFG18: 0x40010CD2 |
| B0_P7_U0_CFG18: 0x40010E52 | B0_P7_U1_CFG18: 0x40010ED2 |
| B1_P2_U0_CFG18: 0x40011452 | B1_P2_U1_CFG18: 0x400114D2 |
| B1_P3_U0_CFG18: 0x40011652 | B1_P3_U1_CFG18: 0x400116D2 |
| B1_P4_U0_CFG18: 0x40011852 | B1_P4_U1_CFG18: 0x400118D2 |
| B1_P5_U0_CFG18: 0x40011A52 | B1_P5_U1_CFG18: 0x40011AD2 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MD0 | | | | | | | |

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Register Segment: 2

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | CTL_MD0[7:0] | CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Value '00' is Direct Mode, where the value written to that bit drives directly in the the routing. Value '01' is Sync Mode, where the control bit input is resampled by the selected SC clock before it is driven into the routing. Value '11' is Pulse Mode. Similar to Sync Mode, the control bit is resampled, then driven into the routing for a duration of 1 SC clock period. In addition, the control bit accessible by the CPU is reset at the end of the pulse period. The control bit can be polled for feedback with regard to this timing. |

1.3.1197 B[0..3]_P[0..7]_U[0..1]_CFG19

CFG19

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG19: 0x40010053 | B0_P0_U1_CFG19: 0x400100D3 |
| B0_P1_U0_CFG19: 0x40010253 | B0_P1_U1_CFG19: 0x400102D3 |
| B0_P2_U0_CFG19: 0x40010453 | B0_P2_U1_CFG19: 0x400104D3 |
| B0_P3_U0_CFG19: 0x40010653 | B0_P3_U1_CFG19: 0x400106D3 |
| B0_P4_U0_CFG19: 0x40010853 | B0_P4_U1_CFG19: 0x400108D3 |
| B0_P5_U0_CFG19: 0x40010A53 | B0_P5_U1_CFG19: 0x40010AD3 |
| B0_P6_U0_CFG19: 0x40010C53 | B0_P6_U1_CFG19: 0x40010CD3 |
| B0_P7_U0_CFG19: 0x40010E53 | B0_P7_U1_CFG19: 0x40010ED3 |
| B1_P2_U0_CFG19: 0x40011453 | B1_P2_U1_CFG19: 0x400114D3 |
| B1_P3_U0_CFG19: 0x40011653 | B1_P3_U1_CFG19: 0x400116D3 |
| B1_P4_U0_CFG19: 0x40011853 | B1_P4_U1_CFG19: 0x400118D3 |
| B1_P5_U0_CFG19: 0x40011A53 | B1_P5_U1_CFG19: 0x40011AD3 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | CTL_MD1 | | | | | | | |

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Register Segment: 2

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | CTL_MD1[7:0] | CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Value '00' is Direct Mode, where the value written to that bit drives directly in the the routing. Value '01' is Sync Mode, where the control bit input is resampled by the selected SC clock before it is driven into the routing. Value '11' is Pulse Mode. Similar to Sync Mode, the control bit is resampled, then driven into the routing for a duration of 1 SC clock period. In addition, the control bit accessible by the CPU is reset at the end of the pulse period. The control bit can be polled for feedback with regard to this timing. |

1.3.1198 B[0..3]_P[0..7]_U[0..1]_CFG20 CFG20

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG20: 0x40010054 | B0_P0_U1_CFG20: 0x400100D4 |
| B0_P1_U0_CFG20: 0x40010254 | B0_P1_U1_CFG20: 0x400102D4 |
| B0_P2_U0_CFG20: 0x40010454 | B0_P2_U1_CFG20: 0x400104D4 |
| B0_P3_U0_CFG20: 0x40010654 | B0_P3_U1_CFG20: 0x400106D4 |
| B0_P4_U0_CFG20: 0x40010854 | B0_P4_U1_CFG20: 0x400108D4 |
| B0_P5_U0_CFG20: 0x40010A54 | B0_P5_U1_CFG20: 0x40010AD4 |
| B0_P6_U0_CFG20: 0x40010C54 | B0_P6_U1_CFG20: 0x40010CD4 |
| B0_P7_U0_CFG20: 0x40010E54 | B0_P7_U1_CFG20: 0x40010ED4 |
| B1_P2_U0_CFG20: 0x40011454 | B1_P2_U1_CFG20: 0x400114D4 |
| B1_P3_U0_CFG20: 0x40011654 | B1_P3_U1_CFG20: 0x400116D4 |
| B1_P4_U0_CFG20: 0x40011854 | B1_P4_U1_CFG20: 0x400118D4 |
| B1_P5_U0_CFG20: 0x40011A54 | B1_P5_U1_CFG20: 0x40011AD4 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | STAT_MD | | | | | | | |

Status Register input mode selection

Register Segment: 2

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | STAT_MD[7:0] | Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read directly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. |

1.3.1199 B[0..3]_P[0..7]_U[0..1]_CFG21

CFG21

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG21: 0x40010055 | B0_P0_U1_CFG21: 0x400100D5 |
| B0_P1_U0_CFG21: 0x40010255 | B0_P1_U1_CFG21: 0x400102D5 |
| B0_P2_U0_CFG21: 0x40010455 | B0_P2_U1_CFG21: 0x400104D5 |
| B0_P3_U0_CFG21: 0x40010655 | B0_P3_U1_CFG21: 0x400106D5 |
| B0_P4_U0_CFG21: 0x40010855 | B0_P4_U1_CFG21: 0x400108D5 |
| B0_P5_U0_CFG21: 0x40010A55 | B0_P5_U1_CFG21: 0x40010AD5 |
| B0_P6_U0_CFG21: 0x40010C55 | B0_P6_U1_CFG21: 0x40010CD5 |
| B0_P7_U0_CFG21: 0x40010E55 | B0_P7_U1_CFG21: 0x40010ED5 |
| B1_P2_U0_CFG21: 0x40011455 | B1_P2_U1_CFG21: 0x400114D5 |
| B1_P3_U0_CFG21: 0x40011655 | B1_P3_U1_CFG21: 0x400116D5 |
| B1_P4_U0_CFG21: 0x40011855 | B1_P4_U1_CFG21: 0x400118D5 |
| B1_P5_U0_CFG21: 0x40011A55 | B1_P5_U1_CFG21: 0x40011AD5 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|-------|-------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | NC1 | NC0 |

Spare register bits

Register Segment: 2

| Bits | Name | Description |
|------|------|--------------------|
| 1 | NC1 | Spare register bit |
| 0 | NC0 | Spare register bit |

1.3.1200 B[0..3]_P[0..7]_U[0..1]_CFG22

CFG22

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG22: 0x40010056 | B0_P0_U1_CFG22: 0x400100D6 |
| B0_P1_U0_CFG22: 0x40010256 | B0_P1_U1_CFG22: 0x400102D6 |
| B0_P2_U0_CFG22: 0x40010456 | B0_P2_U1_CFG22: 0x400104D6 |
| B0_P3_U0_CFG22: 0x40010656 | B0_P3_U1_CFG22: 0x400106D6 |
| B0_P4_U0_CFG22: 0x40010856 | B0_P4_U1_CFG22: 0x400108D6 |
| B0_P5_U0_CFG22: 0x40010A56 | B0_P5_U1_CFG22: 0x40010AD6 |
| B0_P6_U0_CFG22: 0x40010C56 | B0_P6_U1_CFG22: 0x40010CD6 |
| B0_P7_U0_CFG22: 0x40010E56 | B0_P7_U1_CFG22: 0x40010ED6 |
| B1_P2_U0_CFG22: 0x40011456 | B1_P2_U1_CFG22: 0x400114D6 |
| B1_P3_U0_CFG22: 0x40011656 | B1_P3_U1_CFG22: 0x400116D6 |
| B1_P4_U0_CFG22: 0x40011856 | B1_P4_U1_CFG22: 0x400118D6 |
| B1_P5_U0_CFG22: 0x40011A56 | B1_P5_U1_CFG22: 0x40011AD6 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|------------|------------|-----------|------------|---|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:00 | |
| HW Access | NA | | | R | R | R | R | |
| Name | | | | SC_EXT_RES | SC_SYNC_MD | SC_INT_MD | SC_OUT_CTL | |

SC block configuration control

Register Segment: 2

| Bits | Name | Description |
|------|------------|--|
| 4 | SC_EXT_RES | Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. In other usage models, such as DMA data writing, an asynchronous routed reset may be needed. See Table 1-801. |
| 3 | SC_SYNC_MD | SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module. See Table 1-803. |
| 2 | SC_INT_MD | SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0. See Table 1-802. |

1.3.1200 B[0..3]_P[0..7]_U[0..1]_CFG22 (continued)

1:0 SC_OUT_CTL[1:0] Selects the output source for the Status and Control routing connections

See Table 1-800.

Table 1-800. Bit field encoding: OUT_CTL_ENUM

| Value | Name | Description |
|-------|----------|---|
| 2'b00 | CONTROL | Control out, 8-bits of control are driven to the routing connections |
| 2'b01 | PARALLEL | Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections |
| 2'b10 | COUNTER | Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections |
| 2'b11 | RESERVED | Reserved |

Table 1-801. Bit field encoding: SC_EXT_RES_ENUM

| Value | Name | Description |
|-------|----------|--|
| 1'b0 | DISABLED | When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared |
| 1'b1 | ENABLED | When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits. |

Table 1-802. Bit field encoding: SC_INT_MD_ENUM

| Value | Name | Description |
|-------|----------|--|
| 1'b0 | NORMAL | Normal Mode - Routing connection sc_io[3] is a normal input to the status register |
| 1'b1 | INT_MODE | Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output |

Table 1-803. Bit field encoding: SC_SYNC_MD_ENUM

| Value | Name | Description |
|-------|-----------|---|
| 1'b0 | NORMAL | Normal Mode - Status register operation |
| 1'b1 | SYNC_MODE | Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs |

1.3.1201 B[0..3]_P[0..7]_U[0..1]_CFG23

CFG23

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG23: 0x40010057 | B0_P0_U1_CFG23: 0x400100D7 |
| B0_P1_U0_CFG23: 0x40010257 | B0_P1_U1_CFG23: 0x400102D7 |
| B0_P2_U0_CFG23: 0x40010457 | B0_P2_U1_CFG23: 0x400104D7 |
| B0_P3_U0_CFG23: 0x40010657 | B0_P3_U1_CFG23: 0x400106D7 |
| B0_P4_U0_CFG23: 0x40010857 | B0_P4_U1_CFG23: 0x400108D7 |
| B0_P5_U0_CFG23: 0x40010A57 | B0_P5_U1_CFG23: 0x40010AD7 |
| B0_P6_U0_CFG23: 0x40010C57 | B0_P6_U1_CFG23: 0x40010CD7 |
| B0_P7_U0_CFG23: 0x40010E57 | B0_P7_U1_CFG23: 0x40010ED7 |
| B1_P2_U0_CFG23: 0x40011457 | B1_P2_U1_CFG23: 0x400114D7 |
| B1_P3_U0_CFG23: 0x40011657 | B1_P3_U1_CFG23: 0x400116D7 |
| B1_P4_U0_CFG23: 0x40011857 | B1_P4_U1_CFG23: 0x400118D7 |
| B1_P5_U0_CFG23: 0x40011A57 | B1_P5_U1_CFG23: 0x40011AD7 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|---------|----------|----------|------------|---|------------|---|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | | R/W:00 | |
| HW Access | NA | R | R | R | R | | R | |
| Name | | ALT_CNT | ROUTE_EN | ROUTE_LD | CNT_EN_SEL | | CNT_LD_SEL | |

Counter Control

Register Segment: 2

| Bits | Name | Description |
|------|-----------------|--|
| 6 | ALT_CNT | Configure the alternate operating mode of the counter See Table 1-804. |
| 5 | ROUTE_EN | Configure the counter enable signal for routing input See Table 1-807. |
| 4 | ROUTE_LD | Configure the counter load signal for routing input See Table 1-808. |
| 3:2 | CNT_EN_SEL[1:0] | Selects the routing inputs for the counter enable signal See Table 1-805. |
| 1:0 | CNT_LD_SEL[1:0] | Selects the routing inputs for the counter load signal See Table 1-806. |

1.3.1201 B[0..3]_P[0..7]_U[0..1]_CFG23 (continued)

Table 1-804. Bit field encoding: SC_ALT_CNT_ENUM

| Value | Name | Description |
|-------|--------------|----------------------------------|
| 1'b0 | DEFAULT_MODE | Default counter operating mode |
| 1'b1 | ALT_MODE | Alternate counter operating mode |

Table 1-805. Bit field encoding: SC_CNT_EN_ENUM

| Value | Name | Description |
|-------|--------|--|
| 2'b00 | SC_IN4 | sc_in[4] |
| 2'b01 | SC_IN5 | sc_in[5] |
| 2'b10 | SC_IN6 | sc_in[6] |
| 2'b11 | SC_IO | sc_io, (SC_IO_CTL must be set to Input Mode) |

Table 1-806. Bit field encoding: SC_CNT_LD_ENUM

| Value | Name | Description |
|-------|--------|-------------|
| 2'b00 | SC_IN0 | sc_in[0] |
| 2'b01 | SC_IN1 | sc_in[1] |
| 2'b10 | SC_IN2 | sc_in[2] |
| 2'b11 | SC_IN3 | sc_in[3] |

Table 1-807. Bit field encoding: SC_ROUTE_EN_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) |
| 1'b1 | ROUTED | Routed EN signal is used, CNT START must be set |

Table 1-808. Bit field encoding: SC_ROUTE_LD_ENUM

| Value | Name | Description |
|-------|---------|------------------------------|
| 1'b0 | DISABLE | Routed LD signal is not used |
| 1'b1 | ROUTED | Routed LD signal is used |

1.3.1202 B[0..3]_P[0..7]_U[0..1]_CFG24

CFG24

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG24: 0x40010058 | B0_P0_U1_CFG24: 0x400100D8 |
| B0_P1_U0_CFG24: 0x40010258 | B0_P1_U1_CFG24: 0x400102D8 |
| B0_P2_U0_CFG24: 0x40010458 | B0_P2_U1_CFG24: 0x400104D8 |
| B0_P3_U0_CFG24: 0x40010658 | B0_P3_U1_CFG24: 0x400106D8 |
| B0_P4_U0_CFG24: 0x40010858 | B0_P4_U1_CFG24: 0x400108D8 |
| B0_P5_U0_CFG24: 0x40010A58 | B0_P5_U1_CFG24: 0x40010AD8 |
| B0_P6_U0_CFG24: 0x40010C58 | B0_P6_U1_CFG24: 0x40010CD8 |
| B0_P7_U0_CFG24: 0x40010E58 | B0_P7_U1_CFG24: 0x40010ED8 |
| B1_P2_U0_CFG24: 0x40011458 | B1_P2_U1_CFG24: 0x400114D8 |
| B1_P3_U0_CFG24: 0x40011658 | B1_P3_U1_CFG24: 0x400116D8 |
| B1_P4_U0_CFG24: 0x40011858 | B1_P4_U1_CFG24: 0x400118D8 |
| B1_P5_U0_CFG24: 0x40011A58 | B1_P5_U1_CFG24: 0x40011AD8 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---------------------|--------|-----------|------------|---|-----------|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | | R/W:00 | |
| HW Access | R | R | R | R | R | | R | |
| Name | RC_RES_SEL1 | RC_RES_SEL0_OR_FRES | RC_INV | RC_EN_INV | RC_EN_MODE | | RC_EN_SEL | |

PLD0 Clock and Reset control

Register Segment: 2

| Bits | Name | Description |
|------|---------------------|--|
| 7 | RC_RES_SEL1 | Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] |
| 6 | RC_RES_SEL0_OR_FRES | Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] |
| 5 | RC_INV | Optionally inverts the clock selection for the associated UDB component block. See Table 1-812. |

1.3.1202 B[0..3]_P[0..7]_U[0..1]_CFG24 (continued)

| | | |
|-----|-----------------|--|
| 4 | RC_EN_INV | Optionally inverts the clock enable selection for the associated UDB component blocks. See Table 1-809. |
| 3:2 | RC_EN_MODE[1:0] | Selects the operating mode for the clock to the associated UDB component block. See Table 1-810. |
| 1:0 | RC_EN_SEL[1:0] | Selects channel route for enable control to the associated UDB component block See Table 1-811. |

Table 1-809. Bit field encoding: RC_EN_INV_ENUM

| Value | Name | Description |
|-------|----------|--------------|
| 1'b0 | TRUE | Non-inverted |
| 1'b1 | INVERTED | Inverted |

Table 1-810. Bit field encoding: RC_EN_MODE_ENUM

| Value | Name | Description |
|-------|---------|-----------------|
| 2'b00 | OFF | Always off |
| 2'b01 | ON | Always on |
| 2'b10 | POSEDGE | Positive edge |
| 2'b11 | LEVEL | Level sensitive |

Table 1-811. Bit field encoding: RC_EN_SEL_ENUM

| Value | Name | Description |
|-------|--------|-------------|
| 2'b00 | RC_IN0 | rc_in[0] |
| 2'b01 | RC_IN1 | rc_in[1] |
| 2'b10 | RC_IN2 | rc_in[2] |
| 2'b11 | RC_IN3 | rc_in[3] |

Table 1-812. Bit field encoding: RC_INV_ENUM

| Value | Name | Description |
|-------|----------|--------------|
| 1'b0 | TRUE | Non-inverted |
| 1'b1 | INVERTED | Inverted |

1.3.1203 B[0..3]_P[0..7]_U[0..1]_CFG25

CFG25

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG25: 0x40010059 | B0_P0_U1_CFG25: 0x400100D9 |
| B0_P1_U0_CFG25: 0x40010259 | B0_P1_U1_CFG25: 0x400102D9 |
| B0_P2_U0_CFG25: 0x40010459 | B0_P2_U1_CFG25: 0x400104D9 |
| B0_P3_U0_CFG25: 0x40010659 | B0_P3_U1_CFG25: 0x400106D9 |
| B0_P4_U0_CFG25: 0x40010859 | B0_P4_U1_CFG25: 0x400108D9 |
| B0_P5_U0_CFG25: 0x40010A59 | B0_P5_U1_CFG25: 0x40010AD9 |
| B0_P6_U0_CFG25: 0x40010C59 | B0_P6_U1_CFG25: 0x40010CD9 |
| B0_P7_U0_CFG25: 0x40010E59 | B0_P7_U1_CFG25: 0x40010ED9 |
| B1_P2_U0_CFG25: 0x40011459 | B1_P2_U1_CFG25: 0x400114D9 |
| B1_P3_U0_CFG25: 0x40011659 | B1_P3_U1_CFG25: 0x400116D9 |
| B1_P4_U0_CFG25: 0x40011859 | B1_P4_U1_CFG25: 0x400118D9 |
| B1_P5_U0_CFG25: 0x40011A59 | B1_P5_U1_CFG25: 0x40011AD9 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---------------------|--------|-----------|------------|---|-----------|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | | R/W:00 | |
| HW Access | R | R | R | R | R | | R | |
| Name | RC_RES_SEL1 | RC_RES_SELO_OR_FRES | RC_INV | RC_EN_INV | RC_EN_MODE | | RC_EN_SEL | |

PLD1 Clock and Reset control. Note: In alternate reset mode (ALT RES = 1), The PLD0 routed reset selection controls both PLD0 and PLD1, therefore the RC_SEL bits for PLD1 are not used.

Register Segment: 2

| Bits | Name | Description |
|------|---------------------|--|
| 7 | RC_RES_SEL1 | Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SELO_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] |
| 6 | RC_RES_SELO_OR_FRES | Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SELO_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] |
| 5 | RC_INV | Optionally inverts the clock selection for the associated UDB component block. See Table 1-816. |

1.3.1203 B[0..3]_P[0..7]_U[0..1]_CFG25 (continued)

| | | |
|-----|-----------------|--|
| 4 | RC_EN_INV | Optionally inverts the clock enable selection for the associated UDB component blocks. See Table 1-813. |
| 3:2 | RC_EN_MODE[1:0] | Selects the operating mode for the clock to the associated UDB component block. See Table 1-814. |
| 1:0 | RC_EN_SEL[1:0] | Selects channel route for enable control to the associated UDB component block See Table 1-815. |

Table 1-813. Bit field encoding: RC_EN_INV_ENUM

| Value | Name | Description |
|-------|----------|--------------|
| 1'b0 | TRUE | Non-inverted |
| 1'b1 | INVERTED | Inverted |

Table 1-814. Bit field encoding: RC_EN_MODE_ENUM

| Value | Name | Description |
|-------|---------|-----------------|
| 2'b00 | OFF | Always off |
| 2'b01 | ON | Always on |
| 2'b10 | POSEDGE | Positive edge |
| 2'b11 | LEVEL | Level sensitive |

Table 1-815. Bit field encoding: RC_EN_SEL_ENUM

| Value | Name | Description |
|-------|--------|-------------|
| 2'b00 | RC_IN0 | rc_in[0] |
| 2'b01 | RC_IN1 | rc_in[1] |
| 2'b10 | RC_IN2 | rc_in[2] |
| 2'b11 | RC_IN3 | rc_in[3] |

Table 1-816. Bit field encoding: RC_INV_ENUM

| Value | Name | Description |
|-------|----------|--------------|
| 1'b0 | TRUE | Non-inverted |
| 1'b1 | INVERTED | Inverted |

1.3.1204 B[0..3]_P[0..7]_U[0..1]_CFG26

CFG26

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG26: 0x4001005A | B0_P0_U1_CFG26: 0x400100DA |
| B0_P1_U0_CFG26: 0x4001025A | B0_P1_U1_CFG26: 0x400102DA |
| B0_P2_U0_CFG26: 0x4001045A | B0_P2_U1_CFG26: 0x400104DA |
| B0_P3_U0_CFG26: 0x4001065A | B0_P3_U1_CFG26: 0x400106DA |
| B0_P4_U0_CFG26: 0x4001085A | B0_P4_U1_CFG26: 0x400108DA |
| B0_P5_U0_CFG26: 0x40010A5A | B0_P5_U1_CFG26: 0x40010ADA |
| B0_P6_U0_CFG26: 0x40010C5A | B0_P6_U1_CFG26: 0x40010CDA |
| B0_P7_U0_CFG26: 0x40010E5A | B0_P7_U1_CFG26: 0x40010EDA |
| B1_P2_U0_CFG26: 0x4001145A | B1_P2_U1_CFG26: 0x400114DA |
| B1_P3_U0_CFG26: 0x4001165A | B1_P3_U1_CFG26: 0x400116DA |
| B1_P4_U0_CFG26: 0x4001185A | B1_P4_U1_CFG26: 0x400118DA |
| B1_P5_U0_CFG26: 0x40011A5A | B1_P5_U1_CFG26: 0x40011ADA |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---------------------|--------|-----------|------------|---|-----------|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | | R/W:00 | |
| HW Access | R | R | R | R | R | | R | |
| Name | RC_RES_SEL1 | RC_RES_SEL0_OR_FRES | RC_INV | RC_EN_INV | RC_EN_MODE | | RC_EN_SEL | |

Datapath Clock and Reset control

Register Segment: 2

| Bits | Name | Description |
|------|---------------------|--|
| 7 | RC_RES_SEL1 | Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] |
| 6 | RC_RES_SEL0_OR_FRES | Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] |
| 5 | RC_INV | Optionally inverts the clock selection for the associated UDB component block. See Table 1-820. |

1.3.1204 B[0..3]_P[0..7]_U[0..1]_CFG26 (continued)

| | | |
|-----|-----------------|--|
| 4 | RC_EN_INV | Optionally inverts the clock enable selection for the associated UDB component blocks. See Table 1-817. |
| 3:2 | RC_EN_MODE[1:0] | Selects the operating mode for the clock to the associated UDB component block. See Table 1-818. |
| 1:0 | RC_EN_SEL[1:0] | Selects channel route for enable control to the associated UDB component block See Table 1-819. |

Table 1-817. Bit field encoding: RC_EN_INV_ENUM

| Value | Name | Description |
|-------|----------|--------------|
| 1'b0 | TRUE | Non-inverted |
| 1'b1 | INVERTED | Inverted |

Table 1-818. Bit field encoding: RC_EN_MODE_ENUM

| Value | Name | Description |
|-------|---------|-----------------|
| 2'b00 | OFF | Always off |
| 2'b01 | ON | Always on |
| 2'b10 | POSEDGE | Positive edge |
| 2'b11 | LEVEL | Level sensitive |

Table 1-819. Bit field encoding: RC_EN_SEL_ENUM

| Value | Name | Description |
|-------|--------|-------------|
| 2'b00 | RC_IN0 | rc_in[0] |
| 2'b01 | RC_IN1 | rc_in[1] |
| 2'b10 | RC_IN2 | rc_in[2] |
| 2'b11 | RC_IN3 | rc_in[3] |

Table 1-820. Bit field encoding: RC_INV_ENUM

| Value | Name | Description |
|-------|----------|--------------|
| 1'b0 | TRUE | Non-inverted |
| 1'b1 | INVERTED | Inverted |

1.3.1205 B[0..3]_P[0..7]_U[0..1]_CFG27

CFG27

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG27: 0x4001005B | B0_P0_U1_CFG27: 0x400100DB |
| B0_P1_U0_CFG27: 0x4001025B | B0_P1_U1_CFG27: 0x400102DB |
| B0_P2_U0_CFG27: 0x4001045B | B0_P2_U1_CFG27: 0x400104DB |
| B0_P3_U0_CFG27: 0x4001065B | B0_P3_U1_CFG27: 0x400106DB |
| B0_P4_U0_CFG27: 0x4001085B | B0_P4_U1_CFG27: 0x400108DB |
| B0_P5_U0_CFG27: 0x40010A5B | B0_P5_U1_CFG27: 0x40010ADB |
| B0_P6_U0_CFG27: 0x40010C5B | B0_P6_U1_CFG27: 0x40010CDB |
| B0_P7_U0_CFG27: 0x40010E5B | B0_P7_U1_CFG27: 0x40010EDB |
| B1_P2_U0_CFG27: 0x4001145B | B1_P2_U1_CFG27: 0x400114DB |
| B1_P3_U0_CFG27: 0x4001165B | B1_P3_U1_CFG27: 0x400116DB |
| B1_P4_U0_CFG27: 0x4001185B | B1_P4_U1_CFG27: 0x400118DB |
| B1_P5_U0_CFG27: 0x40011A5B | B1_P5_U1_CFG27: 0x40011ADB |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---------------------|--------|-----------|------------|---|-----------|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | | R/W:00 | |
| HW Access | R | R | R | R | R | | R | |
| Name | RC_RES_SEL1 | RC_RES_SEL0_OR_FRES | RC_INV | RC_EN_INV | RC_EN_MODE | | RC_EN_SEL | |

Status/Control Clock and Reset control

Register Segment: 2

| Bits | Name | Description |
|------|---------------------|--|
| 7 | RC_RES_SEL1 | Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] |
| 6 | RC_RES_SEL0_OR_FRES | Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] |
| 5 | RC_INV | Optionally inverts the clock selection for the associated UDB component block. See Table 1-824. |

1.3.1205 B[0..3]_P[0..7]_U[0..1]_CFG27 (continued)

| | | |
|-----|-----------------|--|
| 4 | RC_EN_INV | Optionally inverts the clock enable selection for the associated UDB component blocks. See Table 1-821. |
| 3:2 | RC_EN_MODE[1:0] | Selects the operating mode for the clock to the associated UDB component block. See Table 1-822. |
| 1:0 | RC_EN_SEL[1:0] | Selects channel route for enable control to the associated UDB component block See Table 1-823. |

Table 1-821. Bit field encoding: RC_EN_INV_ENUM

| Value | Name | Description |
|-------|----------|--------------|
| 1'b0 | TRUE | Non-inverted |
| 1'b1 | INVERTED | Inverted |

Table 1-822. Bit field encoding: RC_EN_MODE_ENUM

| Value | Name | Description |
|-------|---------|-----------------|
| 2'b00 | OFF | Always off |
| 2'b01 | ON | Always on |
| 2'b10 | POSEDGE | Positive edge |
| 2'b11 | LEVEL | Level sensitive |

Table 1-823. Bit field encoding: RC_EN_SEL_ENUM

| Value | Name | Description |
|-------|--------|-------------|
| 2'b00 | RC_IN0 | rc_in[0] |
| 2'b01 | RC_IN1 | rc_in[1] |
| 2'b10 | RC_IN2 | rc_in[2] |
| 2'b11 | RC_IN3 | rc_in[3] |

Table 1-824. Bit field encoding: RC_INV_ENUM

| Value | Name | Description |
|-------|----------|--------------|
| 1'b0 | TRUE | Non-inverted |
| 1'b1 | INVERTED | Inverted |

1.3.1206 B[0..3]_P[0..7]_U[0..1]_CFG28 CFG28

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG28: 0x4001005C | B0_P0_U1_CFG28: 0x400100DC |
| B0_P1_U0_CFG28: 0x4001025C | B0_P1_U1_CFG28: 0x400102DC |
| B0_P2_U0_CFG28: 0x4001045C | B0_P2_U1_CFG28: 0x400104DC |
| B0_P3_U0_CFG28: 0x4001065C | B0_P3_U1_CFG28: 0x400106DC |
| B0_P4_U0_CFG28: 0x4001085C | B0_P4_U1_CFG28: 0x400108DC |
| B0_P5_U0_CFG28: 0x40010A5C | B0_P5_U1_CFG28: 0x40010ADC |
| B0_P6_U0_CFG28: 0x40010C5C | B0_P6_U1_CFG28: 0x40010CDC |
| B0_P7_U0_CFG28: 0x40010E5C | B0_P7_U1_CFG28: 0x40010EDC |
| B1_P2_U0_CFG28: 0x4001145C | B1_P2_U1_CFG28: 0x400114DC |
| B1_P3_U0_CFG28: 0x4001165C | B1_P3_U1_CFG28: 0x400116DC |
| B1_P4_U0_CFG28: 0x4001185C | B1_P4_U1_CFG28: 0x400118DC |
| B1_P5_U0_CFG28: 0x40011A5C | B1_P5_U1_CFG28: 0x40011ADC |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|-------------|---|---|---|
| SW Access:Reset | R/W:0000 | | | | R/W:0000 | | | |
| HW Access | R | | | | R | | | |
| Name | PLD1_CK_SEL | | | | PLD0_CK_SEL | | | |

Clock Selection for PLD1 and PLD0

Register Segment: 2

| Bits | Name | Description |
|------|------------------|---|
| 7:4 | PLD1_CK_SEL[3:0] | Clock selection registers See Table 1-825. |
| 3:0 | PLD0_CK_SEL[3:0] | Clock selection registers See Table 1-825. |

Table 1-825. Bit field encoding: RC_CK_SEL_ENUM

| Value | Name | Description |
|---------|---------|-------------|
| 4'b0000 | GCLK0 | gclk[0] |
| 4'b0001 | GCLK1 | gclk[1] |
| 4'b0010 | GCLK2 | gclk[2] |
| 4'b0011 | GCLK3 | gclk[3] |
| 4'b0100 | GCLK4 | gclk[4] |
| 4'b0101 | GCLK5 | gclk[5] |
| 4'b0110 | GCLK6 | gclk[6] |
| 4'b0111 | GCLK7 | gclk[7] |
| 4'b1000 | EXT_CLK | ext_clk |

1.3.1206 B[0..3]_P[0..7]_U[0..1]_CFG28 (continued)

Table 1-825. Bit field encoding: RC_CK_SEL_ENUM

| | | |
|---------|--------|--------|
| 4'b1001 | SYSCLK | sysclk |
|---------|--------|--------|

1.3.1207 B[0..3]_P[0..7]_U[0..1]_CFG29 CFG29

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG29: 0x4001005D | B0_P0_U1_CFG29: 0x400100DD |
| B0_P1_U0_CFG29: 0x4001025D | B0_P1_U1_CFG29: 0x400102DD |
| B0_P2_U0_CFG29: 0x4001045D | B0_P2_U1_CFG29: 0x400104DD |
| B0_P3_U0_CFG29: 0x4001065D | B0_P3_U1_CFG29: 0x400106DD |
| B0_P4_U0_CFG29: 0x4001085D | B0_P4_U1_CFG29: 0x400108DD |
| B0_P5_U0_CFG29: 0x40010A5D | B0_P5_U1_CFG29: 0x40010ADD |
| B0_P6_U0_CFG29: 0x40010C5D | B0_P6_U1_CFG29: 0x40010CDD |
| B0_P7_U0_CFG29: 0x40010E5D | B0_P7_U1_CFG29: 0x40010EDD |
| B1_P2_U0_CFG29: 0x4001145D | B1_P2_U1_CFG29: 0x400114DD |
| B1_P3_U0_CFG29: 0x4001165D | B1_P3_U1_CFG29: 0x400116DD |
| B1_P4_U0_CFG29: 0x4001185D | B1_P4_U1_CFG29: 0x400118DD |
| B1_P5_U0_CFG29: 0x40011A5D | B1_P5_U1_CFG29: 0x40011ADD |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|-----------|---|---|---|
| SW Access:Reset | R/W:0000 | | | | R/W:0000 | | | |
| HW Access | R | | | | R | | | |
| Name | SC_CK_SEL | | | | DP_CK_SEL | | | |

Clock Selection for Datapath, Status and Control

Register Segment: 2

| Bits | Name | Description |
|------|----------------|---|
| 7:4 | SC_CK_SEL[3:0] | Clock selection registers See Table 1-826. |
| 3:0 | DP_CK_SEL[3:0] | Clock selection registers See Table 1-826. |

Table 1-826. Bit field encoding: RC_CK_SEL_ENUM

| Value | Name | Description |
|---------|---------|-------------|
| 4'b0000 | GCLK0 | gclk[0] |
| 4'b0001 | GCLK1 | gclk[1] |
| 4'b0010 | GCLK2 | gclk[2] |
| 4'b0011 | GCLK3 | gclk[3] |
| 4'b0100 | GCLK4 | gclk[4] |
| 4'b0101 | GCLK5 | gclk[5] |
| 4'b0110 | GCLK6 | gclk[6] |
| 4'b0111 | GCLK7 | gclk[7] |
| 4'b1000 | EXT_CLK | ext_clk |

1.3.1207 B[0..3]_P[0..7]_U[0..1]_CFG29 (continued)

Table 1-826. Bit field encoding: RC_CK_SEL_ENUM

| | | |
|---------|--------|--------|
| 4'b1001 | SYSCLK | sysclk |
|---------|--------|--------|

1.3.1208 B[0..3]_P[0..7]_U[0..1]_CFG30

CFG30

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG30: 0x4001005E | B0_P0_U1_CFG30: 0x400100DE |
| B0_P1_U0_CFG30: 0x4001025E | B0_P1_U1_CFG30: 0x400102DE |
| B0_P2_U0_CFG30: 0x4001045E | B0_P2_U1_CFG30: 0x400104DE |
| B0_P3_U0_CFG30: 0x4001065E | B0_P3_U1_CFG30: 0x400106DE |
| B0_P4_U0_CFG30: 0x4001085E | B0_P4_U1_CFG30: 0x400108DE |
| B0_P5_U0_CFG30: 0x40010A5E | B0_P5_U1_CFG30: 0x40010ADE |
| B0_P6_U0_CFG30: 0x40010C5E | B0_P6_U1_CFG30: 0x40010CDE |
| B0_P7_U0_CFG30: 0x40010E5E | B0_P7_U1_CFG30: 0x40010EDE |
| B1_P2_U0_CFG30: 0x4001145E | B1_P2_U1_CFG30: 0x400114DE |
| B1_P3_U0_CFG30: 0x4001165E | B1_P3_U1_CFG30: 0x400116DE |
| B1_P4_U0_CFG30: 0x4001185E | B1_P4_U1_CFG30: 0x400118DE |
| B1_P5_U0_CFG30: 0x40011A5E | B1_P5_U1_CFG30: 0x40011ADE |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|----------------|------|---------|-------------------|---------|---------|---|
| SW Access:Reset | R/W:0 | R/W:0 | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:00 | |
| HW Access | R | R | NA | R | R | R | R | |
| Name | SC_RES_P OL | DP_RES_P OL | | GUDB_WR | EN_RES_C NTCTL | RES_POL | RES_SEL | |

Reset control

Register Segment: 2

| Bits | Name | Description |
|------|------------|--|
| 7 | SC_RES_POL | Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. See Table 1-832. |
| 6 | DP_RES_POL | Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. See Table 1-827. |
| 4 | GUDB_WR | Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. See Table 1-829. |

1.3.1208 B[0..3]_P[0..7]_U[0..1]_CFG30 (continued)

| | | |
|-----|---------------|--|
| 3 | EN_RES_CNTCTL | <p>This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control register modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also.</p> <p>See Table 1-828.</p> |
| 2 | RES_POL | <p>The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused.</p> <p>See Table 1-830.</p> |
| 1:0 | RES_SEL[1:0] | <p>The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used.</p> <p>See Table 1-831.</p> |

Table 1-827. Bit field encoding: RC_DP_RES_POL_ENUM

| Value | Name | Description |
|-------|----------|--|
| 1'b0 | TRUE | Routed reset to the Datapath block is true polarity. |
| 1'b1 | INVERTED | Routed reset to the Datapath block is inverted polarity. |

Table 1-828. Bit field encoding: RC_EN_RES_CNTCTL_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Routed reset is not applied to counter/control register |
| 1'b1 | ENABLE | Routed reset is applied to the counter/control register |

Table 1-829. Bit field encoding: RC_GUDB_WR_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Global UDB configuration/working register write is disabled |
| 1'b1 | ENABLE | Global UDB configuration/working register write is enabled |

Table 1-830. Bit field encoding: RC_RES_POL_ENUM

| Value | Name | Description |
|-------|----------|---|
| 1'b0 | NEGATED | Polarity of the routed reset is true. |
| 1'b1 | ASSERTED | Polarity of the routed reset is inverted. |

Table 1-831. Bit field encoding: RC_RES_SEL_ENUM

| Value | Name | Description |
|-------|--------|-------------|
| 2'b00 | RC_IN0 | rc_in[0] |
| 2'b01 | RC_IN1 | rc_in[1] |
| 2'b10 | RC_IN2 | rc_in[2] |
| 2'b11 | RC_IN3 | rc_in[3] |

Table 1-832. Bit field encoding: RC_SC_RES_POL_ENUM

| Value | Name | Description |
|-------|----------|--|
| 1'b0 | TRUE | Routed reset to the Status and Control block is true polarity. |
| 1'b1 | INVERTED | Routed reset to the Status and Control block is inverted polarity. |

1.3.1209 B[0..3]_P[0..7]_U[0..1]_CFG31

CFG31

Reset: System reset for retention flops [reset_all_retention]

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_CFG31: 0x4001005F | B0_P0_U1_CFG31: 0x400100DF |
| B0_P1_U0_CFG31: 0x4001025F | B0_P1_U1_CFG31: 0x400102DF |
| B0_P2_U0_CFG31: 0x4001045F | B0_P2_U1_CFG31: 0x400104DF |
| B0_P3_U0_CFG31: 0x4001065F | B0_P3_U1_CFG31: 0x400106DF |
| B0_P4_U0_CFG31: 0x4001085F | B0_P4_U1_CFG31: 0x400108DF |
| B0_P5_U0_CFG31: 0x40010A5F | B0_P5_U1_CFG31: 0x40010ADF |
| B0_P6_U0_CFG31: 0x40010C5F | B0_P6_U1_CFG31: 0x40010CDF |
| B0_P7_U0_CFG31: 0x40010E5F | B0_P7_U1_CFG31: 0x40010EDF |
| B1_P2_U0_CFG31: 0x4001145F | B1_P2_U1_CFG31: 0x400114DF |
| B1_P3_U0_CFG31: 0x4001165F | B1_P3_U1_CFG31: 0x400116DF |
| B1_P4_U0_CFG31: 0x4001185F | B1_P4_U1_CFG31: 0x400118DF |
| B1_P5_U0_CFG31: 0x40011A5F | B1_P5_U1_CFG31: 0x40011ADF |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|--------------|------------|---|-----------|--------------|----------|---------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:00 | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | | R | R | R | R |
| Name | PLD1_RES_POL | PLD0_RES_POL | EXT_CK_SEL | | EN_RES_DP | EN_RES_S_TAT | EXT_SYNC | ALT_RES |

Reset control

Register Segment: 2

| Bits | Name | Description |
|------|-----------------|--|
| 7 | PLD1_RES_POL | Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. See Table 1-839. |
| 6 | PLD0_RES_POL | The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available in the PLD block for both PLDs, therefore this bit controls the reset polarity to both PLD0 and PLD1. When ALT RES is '0' this bit is not used. See Table 1-838. |
| 5:4 | EXT_CK_SEL[1:0] | External clock selection See Table 1-836. |
| 3 | EN_RES_DP | Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. See Table 1-834. |

1.3.1209 B[0..3]_P[0..7]_U[0..1]_CFG31 (continued)

| | | |
|---|-------------|---|
| 2 | EN_RES_STAT | Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. See Table 1-835. |
| 1 | EXT_SYNC | Enable synchronization of selected external clock See Table 1-837. |
| 0 | ALT_RES | This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs.; See Table 1-833. |

Table 1-833. Bit field encoding: RC_ALT_RES_ENUM

| Value | Name | Description |
|-------|------------|---|
| 1'b0 | COMPATIBLE | All UDB blocks share a common routed reset. |
| 1'b1 | ALTERNAT | Each UDB component block can select and control it's individual routed reset. |

Table 1-834. Bit field encoding: RC_EN_RES_DP_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | Routed reset to the Datapath block is gated off. |
| 1'b1 | ENABLE | Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26 |

Table 1-835. Bit field encoding: RC_EN_RES_STAT_ENUM

| Value | Name | Description |
|-------|----------|---|
| 1'b0 | NEGATED | Status register routed reset is gated off |
| 1'b1 | ASSERTED | Status register routed reset is on |

Table 1-836. Bit field encoding: RC_EXT_CK_SEL_ENUM

| Value | Name | Description |
|-------|--------|-------------|
| 2'b00 | RC_IN0 | rc_in[0] |
| 2'b01 | RC_IN1 | rc_in[1] |
| 2'b10 | RC_IN2 | rc_in[2] |
| 2'b11 | RC_IN3 | rc_in[3] |

Table 1-837. Bit field encoding: RC_EXT_SYNC_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Selected external clock input is not synchronized |
| 1'b1 | ENABLE | Selected external clock input is synchronized |

Table 1-838. Bit field encoding: RC_PLD0_RES_POL_ENUM

| Value | Name | Description |
|-------|----------|---|
| 1'b0 | TRUE | Routed reset to the PLD0/PLD1 block is true polarity. |
| 1'b1 | INVERTED | Routed reset to the PLD0/PLD1 block is inverted polarity. |

Table 1-839. Bit field encoding: RC_PLD1_RES_POL_ENUM

| Value | Name | Description |
|-------|----------|-------------|
| 1'b0 | TRUE | NU |
| 1'b1 | INVERTED | NU |

1.3.1210 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7]

DCFG

Reset: N/A

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P0_U0_DCFG0: 0x40010060 | B0_P0_U0_DCFG1: 0x40010062 |
| B0_P0_U0_DCFG2: 0x40010064 | B0_P0_U0_DCFG3: 0x40010066 |
| B0_P0_U0_DCFG4: 0x40010068 | B0_P0_U0_DCFG5: 0x4001006A |
| B0_P0_U0_DCFG6: 0x4001006C | B0_P0_U0_DCFG7: 0x4001006E |
| B0_P0_U1_DCFG0: 0x400100E0 | B0_P0_U1_DCFG1: 0x400100E2 |
| B0_P0_U1_DCFG2: 0x400100E4 | B0_P0_U1_DCFG3: 0x400100E6 |
| B0_P0_U1_DCFG4: 0x400100E8 | B0_P0_U1_DCFG5: 0x400100EA |
| B0_P0_U1_DCFG6: 0x400100EC | B0_P0_U1_DCFG7: 0x400100EE |
| B0_P1_U0_DCFG0: 0x40010260 | B0_P1_U0_DCFG1: 0x40010262 |
| B0_P1_U0_DCFG2: 0x40010264 | B0_P1_U0_DCFG3: 0x40010266 |
| B0_P1_U0_DCFG4: 0x40010268 | B0_P1_U0_DCFG5: 0x4001026A |
| B0_P1_U0_DCFG6: 0x4001026C | B0_P1_U0_DCFG7: 0x4001026E |
| B0_P1_U1_DCFG0: 0x400102E0 | B0_P1_U1_DCFG1: 0x400102E2 |
| B0_P1_U1_DCFG2: 0x400102E4 | B0_P1_U1_DCFG3: 0x400102E6 |
| B0_P1_U1_DCFG4: 0x400102E8 | B0_P1_U1_DCFG5: 0x400102EA |
| B0_P1_U1_DCFG6: 0x400102EC | B0_P1_U1_DCFG7: 0x400102EE |
| B0_P2_U0_DCFG0: 0x40010460 | B0_P2_U0_DCFG1: 0x40010462 |
| B0_P2_U0_DCFG2: 0x40010464 | B0_P2_U0_DCFG3: 0x40010466 |
| B0_P2_U0_DCFG4: 0x40010468 | B0_P2_U0_DCFG5: 0x4001046A |
| B0_P2_U0_DCFG6: 0x4001046C | B0_P2_U0_DCFG7: 0x4001046E |
| B0_P2_U1_DCFG0: 0x400104E0 | B0_P2_U1_DCFG1: 0x400104E2 |
| B0_P2_U1_DCFG2: 0x400104E4 | B0_P2_U1_DCFG3: 0x400104E6 |
| B0_P2_U1_DCFG4: 0x400104E8 | B0_P2_U1_DCFG5: 0x400104EA |
| B0_P2_U1_DCFG6: 0x400104EC | B0_P2_U1_DCFG7: 0x400104EE |
| B0_P3_U0_DCFG0: 0x40010660 | B0_P3_U0_DCFG1: 0x40010662 |
| B0_P3_U0_DCFG2: 0x40010664 | B0_P3_U0_DCFG3: 0x40010666 |
| B0_P3_U0_DCFG4: 0x40010668 | B0_P3_U0_DCFG5: 0x4001066A |
| B0_P3_U0_DCFG6: 0x4001066C | B0_P3_U0_DCFG7: 0x4001066E |
| B0_P3_U1_DCFG0: 0x400106E0 | B0_P3_U1_DCFG1: 0x400106E2 |
| B0_P3_U1_DCFG2: 0x400106E4 | B0_P3_U1_DCFG3: 0x400106E6 |
| B0_P3_U1_DCFG4: 0x400106E8 | B0_P3_U1_DCFG5: 0x400106EA |
| B0_P3_U1_DCFG6: 0x400106EC | B0_P3_U1_DCFG7: 0x400106EE |

1.3.1210 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] (continued)

Register : Address

| | |
|----------------------------|----------------------------|
| B0_P4_U0_DCFG0: 0x40010860 | B0_P4_U0_DCFG1: 0x40010862 |
| B0_P4_U0_DCFG2: 0x40010864 | B0_P4_U0_DCFG3: 0x40010866 |
| B0_P4_U0_DCFG4: 0x40010868 | B0_P4_U0_DCFG5: 0x4001086A |
| B0_P4_U0_DCFG6: 0x4001086C | B0_P4_U0_DCFG7: 0x4001086E |
| B0_P4_U1_DCFG0: 0x400108E0 | B0_P4_U1_DCFG1: 0x400108E2 |
| B0_P4_U1_DCFG2: 0x400108E4 | B0_P4_U1_DCFG3: 0x400108E6 |
| B0_P4_U1_DCFG4: 0x400108E8 | B0_P4_U1_DCFG5: 0x400108EA |
| B0_P4_U1_DCFG6: 0x400108EC | B0_P4_U1_DCFG7: 0x400108EE |
| B0_P5_U0_DCFG0: 0x40010A60 | B0_P5_U0_DCFG1: 0x40010A62 |
| B0_P5_U0_DCFG2: 0x40010A64 | B0_P5_U0_DCFG3: 0x40010A66 |
| B0_P5_U0_DCFG4: 0x40010A68 | B0_P5_U0_DCFG5: 0x40010A6A |
| B0_P5_U0_DCFG6: 0x40010A6C | B0_P5_U0_DCFG7: 0x40010A6E |
| B0_P5_U1_DCFG0: 0x40010AE0 | B0_P5_U1_DCFG1: 0x40010AE2 |
| B0_P5_U1_DCFG2: 0x40010AE4 | B0_P5_U1_DCFG3: 0x40010AE6 |
| B0_P5_U1_DCFG4: 0x40010AE8 | B0_P5_U1_DCFG5: 0x40010AEA |
| B0_P5_U1_DCFG6: 0x40010AEC | B0_P5_U1_DCFG7: 0x40010AEE |
| B0_P6_U0_DCFG0: 0x40010C60 | B0_P6_U0_DCFG1: 0x40010C62 |
| B0_P6_U0_DCFG2: 0x40010C64 | B0_P6_U0_DCFG3: 0x40010C66 |
| B0_P6_U0_DCFG4: 0x40010C68 | B0_P6_U0_DCFG5: 0x40010C6A |
| B0_P6_U0_DCFG6: 0x40010C6C | B0_P6_U0_DCFG7: 0x40010C6E |
| B0_P6_U1_DCFG0: 0x40010CE0 | B0_P6_U1_DCFG1: 0x40010CE2 |
| B0_P6_U1_DCFG2: 0x40010CE4 | B0_P6_U1_DCFG3: 0x40010CE6 |
| B0_P6_U1_DCFG4: 0x40010CE8 | B0_P6_U1_DCFG5: 0x40010CEA |
| B0_P6_U1_DCFG6: 0x40010CEC | B0_P6_U1_DCFG7: 0x40010CEE |
| B0_P7_U0_DCFG0: 0x40010E60 | B0_P7_U0_DCFG1: 0x40010E62 |
| B0_P7_U0_DCFG2: 0x40010E64 | B0_P7_U0_DCFG3: 0x40010E66 |
| B0_P7_U0_DCFG4: 0x40010E68 | B0_P7_U0_DCFG5: 0x40010E6A |
| B0_P7_U0_DCFG6: 0x40010E6C | B0_P7_U0_DCFG7: 0x40010E6E |
| B0_P7_U1_DCFG0: 0x40010EE0 | B0_P7_U1_DCFG1: 0x40010EE2 |
| B0_P7_U1_DCFG2: 0x40010EE4 | B0_P7_U1_DCFG3: 0x40010EE6 |
| B0_P7_U1_DCFG4: 0x40010EE8 | B0_P7_U1_DCFG5: 0x40010EEA |
| B0_P7_U1_DCFG6: 0x40010EEC | B0_P7_U1_DCFG7: 0x40010EEE |
| B1_P2_U0_DCFG0: 0x40011460 | B1_P2_U0_DCFG1: 0x40011462 |
| B1_P2_U0_DCFG2: 0x40011464 | B1_P2_U0_DCFG3: 0x40011466 |
| B1_P2_U0_DCFG4: 0x40011468 | B1_P2_U0_DCFG5: 0x4001146A |
| B1_P2_U0_DCFG6: 0x4001146C | B1_P2_U0_DCFG7: 0x4001146E |

1.3.1210 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] (continued)

Register : Address

| | |
|----------------------------|----------------------------|
| B1_P2_U1_DCFG0: 0x400114E0 | B1_P2_U1_DCFG1: 0x400114E2 |
| B1_P2_U1_DCFG2: 0x400114E4 | B1_P2_U1_DCFG3: 0x400114E6 |
| B1_P2_U1_DCFG4: 0x400114E8 | B1_P2_U1_DCFG5: 0x400114EA |
| B1_P2_U1_DCFG6: 0x400114EC | B1_P2_U1_DCFG7: 0x400114EE |
| B1_P3_U0_DCFG0: 0x40011660 | B1_P3_U0_DCFG1: 0x40011662 |
| B1_P3_U0_DCFG2: 0x40011664 | B1_P3_U0_DCFG3: 0x40011666 |
| B1_P3_U0_DCFG4: 0x40011668 | B1_P3_U0_DCFG5: 0x4001166A |
| B1_P3_U0_DCFG6: 0x4001166C | B1_P3_U0_DCFG7: 0x4001166E |
| B1_P3_U1_DCFG0: 0x400116E0 | B1_P3_U1_DCFG1: 0x400116E2 |
| B1_P3_U1_DCFG2: 0x400116E4 | B1_P3_U1_DCFG3: 0x400116E6 |
| B1_P3_U1_DCFG4: 0x400116E8 | B1_P3_U1_DCFG5: 0x400116EA |
| B1_P3_U1_DCFG6: 0x400116EC | B1_P3_U1_DCFG7: 0x400116EE |
| B1_P4_U0_DCFG0: 0x40011860 | B1_P4_U0_DCFG1: 0x40011862 |
| B1_P4_U0_DCFG2: 0x40011864 | B1_P4_U0_DCFG3: 0x40011866 |
| B1_P4_U0_DCFG4: 0x40011868 | B1_P4_U0_DCFG5: 0x4001186A |
| B1_P4_U0_DCFG6: 0x4001186C | B1_P4_U0_DCFG7: 0x4001186E |
| B1_P4_U1_DCFG0: 0x400118E0 | B1_P4_U1_DCFG1: 0x400118E2 |
| B1_P4_U1_DCFG2: 0x400118E4 | B1_P4_U1_DCFG3: 0x400118E6 |
| B1_P4_U1_DCFG4: 0x400118E8 | B1_P4_U1_DCFG5: 0x400118EA |
| B1_P4_U1_DCFG6: 0x400118EC | B1_P4_U1_DCFG7: 0x400118EE |
| B1_P5_U0_DCFG0: 0x40011A60 | B1_P5_U0_DCFG1: 0x40011A62 |
| B1_P5_U0_DCFG2: 0x40011A64 | B1_P5_U0_DCFG3: 0x40011A66 |
| B1_P5_U0_DCFG4: 0x40011A68 | B1_P5_U0_DCFG5: 0x40011A6A |
| B1_P5_U0_DCFG6: 0x40011A6C | B1_P5_U0_DCFG7: 0x40011A6E |
| B1_P5_U1_DCFG0: 0x40011AE0 | B1_P5_U1_DCFG1: 0x40011AE2 |
| B1_P5_U1_DCFG2: 0x40011AE4 | B1_P5_U1_DCFG3: 0x40011AE6 |
| B1_P5_U1_DCFG4: 0x40011AE8 | B1_P5_U1_DCFG5: 0x40011AEA |
| B1_P5_U1_DCFG6: 0x40011AEC | B1_P5_U1_DCFG7: 0x40011AEE |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|-----------|---|--------|--------|--------|---------|
| SW Access:Reset | R/W:UU | | R/W:UU | | R/W:U | R/W:U | R/W:U | R/W:U |
| HW Access | R | | R | | R | R | R | R |
| Name | A0_WR_SRC | | A1_WR_SRC | | CFB_EN | CI_SEL | SI_SEL | CMP_SEL |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|---------|----|----|-------|--------|----|--------|---|
| SW Access:Reset | R/W:UUU | | | R/W:U | R/W:UU | | R/W:UU | |
| HW Access | R | | | R | R | | R | |

1.3.1210 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] (continued)

| Name | FUNC | SRC_A | SRC_B | SHIFT |
|------|------|-------|-------|-------|
|------|------|-------|-------|-------|

Dynamic Configuration RAM

Register Segment: 2

| Bits | Name | Description |
|-------|----------------|---|
| 15:13 | FUNC[2:0] | Dynamic ALU function selection See Table 1-845. |
| 12 | SRC_A | Dynamic ALU source A selection See Table 1-848. |
| 11:10 | SRC_B[1:0] | Dynamic ALU source B selection See Table 1-849. |
| 9:8 | SHIFT[1:0] | Dynamic shift selection See Table 1-846. |
| 7:6 | A0_WR_SRC[1:0] | Dynamic A0 write source selection See Table 1-840. |
| 5:4 | A1_WR_SRC[1:0] | Dynamic A1 write source selection See Table 1-841. |
| 3 | CFB_EN | Dynamic CRC feedback selection See Table 1-842. |
| 2 | CI_SEL | Dynamic carry in selection See Table 1-843. |
| 1 | SI_SEL | Dynamic shift in selection See Table 1-847. |
| 0 | CMP_SEL | Dynamic compare selection See Table 1-844. |

Table 1-840. Bit field encoding: A0_WR_SRC_ENUM

| Value | Name | Description |
|-------|---------|--------------------------|
| 2'b00 | NOWRITE | no value written to A0 |
| 2'b01 | ALU | ALU output written to A0 |
| 2'b10 | D0 | D0 value written to A0 |
| 2'b11 | F0 | F0 value written to A0 |

Table 1-841. Bit field encoding: A1_WR_SRC_ENUM

| Value | Name | Description |
|-------|---------|--------------------------|
| 2'b00 | NOWRITE | no value written to A1 |
| 2'b01 | ALU | ALU output written to A1 |
| 2'b10 | D1 | D1 value written to A1 |
| 2'b11 | F1 | F1 value written to A1 |

Table 1-842. Bit field encoding: CFB_EN_ENUM

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1210 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] (continued)

Table 1-842. Bit field encoding: CFB_EN_ENUM

| | | |
|------|---------|-----------------------|
| 1'b0 | DISABLE | CRC feedback disabled |
| 1'b1 | ENABLE | CRC feedback enabled |

Table 1-843. Bit field encoding: CI_SEL_ENUM

| Value | Name | Description |
|-------|-------|-----------------|
| 1'b0 | CFG_A | Configuration A |
| 1'b1 | CFG_B | Configuration B |

Table 1-844. Bit field encoding: CMP_SEL_ENUM

| Value | Name | Description |
|-------|-------|-----------------|
| 1'b0 | CFG_A | Configuration A |
| 1'b1 | CFG_B | Configuration B |

Table 1-845. Bit field encoding: FUNC_ENUM

| Value | Name | Description |
|--------|-------|--------------------|
| 3'b000 | PASS | Pass |
| 3'b001 | INC_A | Increment source A |
| 3'b010 | DEC_A | Decrement source A |
| 3'b011 | ADD | Add |
| 3'b100 | SUB | Subtract |
| 3'b101 | XOR | Bitwise XOR |
| 3'b110 | AND | Bitwise AND |
| 3'b111 | OR | Bitwise OR |

Table 1-846. Bit field encoding: SHIFT_ENUM

| Value | Name | Description |
|-------|---------|-------------|
| 2'b00 | NOSHIFT | No shift |
| 2'b01 | LEFT | Left shift |
| 2'b10 | RIGHT | Right shift |
| 2'b11 | SWAP | Nibble swap |

Table 1-847. Bit field encoding: SI_SEL_ENUM

| Value | Name | Description |
|-------|-------|-----------------|
| 1'b0 | CFG_A | Configuration A |
| 1'b1 | CFG_B | Configuration B |

Table 1-848. Bit field encoding: SRC_A_ENUM

| Value | Name | Description |
|-------|------|--------------------|
| 1'b0 | A0 | ALU source A is A0 |
| 1'b1 | A1 | ALU source A is A1 |

Table 1-849. Bit field encoding: SRC_B_ENUM

| Value | Name | Description |
|-------|------|--------------------|
| 2'b00 | D0 | ALU source B is D0 |
| 2'b01 | D1 | ALU source B is D1 |
| 2'b10 | A0 | ALU source B is A0 |
| 2'b11 | A1 | ALU source B is A1 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127]

HC

Reset: N/A

Register : Address

| | |
|------------------------------|------------------------------|
| B0_P0_ROUTE_HC0: 0x40010100 | B0_P0_ROUTE_HC1: 0x40010101 |
| B0_P0_ROUTE_HC2: 0x40010102 | B0_P0_ROUTE_HC3: 0x40010103 |
| B0_P0_ROUTE_HC4: 0x40010104 | B0_P0_ROUTE_HC5: 0x40010105 |
| B0_P0_ROUTE_HC6: 0x40010106 | B0_P0_ROUTE_HC7: 0x40010107 |
| B0_P0_ROUTE_HC8: 0x40010108 | B0_P0_ROUTE_HC9: 0x40010109 |
| B0_P0_ROUTE_HC10: 0x4001010A | B0_P0_ROUTE_HC11: 0x4001010B |
| B0_P0_ROUTE_HC12: 0x4001010C | B0_P0_ROUTE_HC13: 0x4001010D |
| B0_P0_ROUTE_HC14: 0x4001010E | B0_P0_ROUTE_HC15: 0x4001010F |
| B0_P0_ROUTE_HC16: 0x40010110 | B0_P0_ROUTE_HC17: 0x40010111 |
| B0_P0_ROUTE_HC18: 0x40010112 | B0_P0_ROUTE_HC19: 0x40010113 |
| B0_P0_ROUTE_HC20: 0x40010114 | B0_P0_ROUTE_HC21: 0x40010115 |
| B0_P0_ROUTE_HC22: 0x40010116 | B0_P0_ROUTE_HC23: 0x40010117 |
| B0_P0_ROUTE_HC24: 0x40010118 | B0_P0_ROUTE_HC25: 0x40010119 |
| B0_P0_ROUTE_HC26: 0x4001011A | B0_P0_ROUTE_HC27: 0x4001011B |
| B0_P0_ROUTE_HC28: 0x4001011C | B0_P0_ROUTE_HC29: 0x4001011D |
| B0_P0_ROUTE_HC30: 0x4001011E | B0_P0_ROUTE_HC31: 0x4001011F |
| B0_P0_ROUTE_HC32: 0x40010120 | B0_P0_ROUTE_HC33: 0x40010121 |
| B0_P0_ROUTE_HC34: 0x40010122 | B0_P0_ROUTE_HC35: 0x40010123 |
| B0_P0_ROUTE_HC36: 0x40010124 | B0_P0_ROUTE_HC37: 0x40010125 |
| B0_P0_ROUTE_HC38: 0x40010126 | B0_P0_ROUTE_HC39: 0x40010127 |
| B0_P0_ROUTE_HC40: 0x40010128 | B0_P0_ROUTE_HC41: 0x40010129 |
| B0_P0_ROUTE_HC42: 0x4001012A | B0_P0_ROUTE_HC43: 0x4001012B |
| B0_P0_ROUTE_HC44: 0x4001012C | B0_P0_ROUTE_HC45: 0x4001012D |
| B0_P0_ROUTE_HC46: 0x4001012E | B0_P0_ROUTE_HC47: 0x4001012F |
| B0_P0_ROUTE_HC48: 0x40010130 | B0_P0_ROUTE_HC49: 0x40010131 |
| B0_P0_ROUTE_HC50: 0x40010132 | B0_P0_ROUTE_HC51: 0x40010133 |
| B0_P0_ROUTE_HC52: 0x40010134 | B0_P0_ROUTE_HC53: 0x40010135 |
| B0_P0_ROUTE_HC54: 0x40010136 | B0_P0_ROUTE_HC55: 0x40010137 |
| B0_P0_ROUTE_HC56: 0x40010138 | B0_P0_ROUTE_HC57: 0x40010139 |
| B0_P0_ROUTE_HC58: 0x4001013A | B0_P0_ROUTE_HC59: 0x4001013B |
| B0_P0_ROUTE_HC60: 0x4001013C | B0_P0_ROUTE_HC61: 0x4001013D |
| B0_P0_ROUTE_HC62: 0x4001013E | B0_P0_ROUTE_HC63: 0x4001013F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B0_P0_ROUTE_HC64: 0x40010140 | B0_P0_ROUTE_HC65: 0x40010141 |
| B0_P0_ROUTE_HC66: 0x40010142 | B0_P0_ROUTE_HC67: 0x40010143 |
| B0_P0_ROUTE_HC68: 0x40010144 | B0_P0_ROUTE_HC69: 0x40010145 |
| B0_P0_ROUTE_HC70: 0x40010146 | B0_P0_ROUTE_HC71: 0x40010147 |
| B0_P0_ROUTE_HC72: 0x40010148 | B0_P0_ROUTE_HC73: 0x40010149 |
| B0_P0_ROUTE_HC74: 0x4001014A | B0_P0_ROUTE_HC75: 0x4001014B |
| B0_P0_ROUTE_HC76: 0x4001014C | B0_P0_ROUTE_HC77: 0x4001014D |
| B0_P0_ROUTE_HC78: 0x4001014E | B0_P0_ROUTE_HC79: 0x4001014F |
| B0_P0_ROUTE_HC80: 0x40010150 | B0_P0_ROUTE_HC81: 0x40010151 |
| B0_P0_ROUTE_HC82: 0x40010152 | B0_P0_ROUTE_HC83: 0x40010153 |
| B0_P0_ROUTE_HC84: 0x40010154 | B0_P0_ROUTE_HC85: 0x40010155 |
| B0_P0_ROUTE_HC86: 0x40010156 | B0_P0_ROUTE_HC87: 0x40010157 |
| B0_P0_ROUTE_HC88: 0x40010158 | B0_P0_ROUTE_HC89: 0x40010159 |
| B0_P0_ROUTE_HC90: 0x4001015A | B0_P0_ROUTE_HC91: 0x4001015B |
| B0_P0_ROUTE_HC92: 0x4001015C | B0_P0_ROUTE_HC93: 0x4001015D |
| B0_P0_ROUTE_HC94: 0x4001015E | B0_P0_ROUTE_HC95: 0x4001015F |
| B0_P0_ROUTE_HC96: 0x40010160 | B0_P0_ROUTE_HC97: 0x40010161 |
| B0_P0_ROUTE_HC98: 0x40010162 | B0_P0_ROUTE_HC99: 0x40010163 |
| B0_P0_ROUTE_HC100: 0x40010164 | B0_P0_ROUTE_HC101: 0x40010165 |
| B0_P0_ROUTE_HC102: 0x40010166 | B0_P0_ROUTE_HC103: 0x40010167 |
| B0_P0_ROUTE_HC104: 0x40010168 | B0_P0_ROUTE_HC105: 0x40010169 |
| B0_P0_ROUTE_HC106: 0x4001016A | B0_P0_ROUTE_HC107: 0x4001016B |
| B0_P0_ROUTE_HC108: 0x4001016C | B0_P0_ROUTE_HC109: 0x4001016D |
| B0_P0_ROUTE_HC110: 0x4001016E | B0_P0_ROUTE_HC111: 0x4001016F |
| B0_P0_ROUTE_HC112: 0x40010170 | B0_P0_ROUTE_HC113: 0x40010171 |
| B0_P0_ROUTE_HC114: 0x40010172 | B0_P0_ROUTE_HC115: 0x40010173 |
| B0_P0_ROUTE_HC116: 0x40010174 | B0_P0_ROUTE_HC117: 0x40010175 |
| B0_P0_ROUTE_HC118: 0x40010176 | B0_P0_ROUTE_HC119: 0x40010177 |
| B0_P0_ROUTE_HC120: 0x40010178 | B0_P0_ROUTE_HC121: 0x40010179 |
| B0_P0_ROUTE_HC122: 0x4001017A | B0_P0_ROUTE_HC123: 0x4001017B |
| B0_P0_ROUTE_HC124: 0x4001017C | B0_P0_ROUTE_HC125: 0x4001017D |
| B0_P0_ROUTE_HC126: 0x4001017E | B0_P0_ROUTE_HC127: 0x4001017F |
| B0_P1_ROUTE_HC0: 0x40010300 | B0_P1_ROUTE_HC1: 0x40010301 |
| B0_P1_ROUTE_HC2: 0x40010302 | B0_P1_ROUTE_HC3: 0x40010303 |
| B0_P1_ROUTE_HC4: 0x40010304 | B0_P1_ROUTE_HC5: 0x40010305 |
| B0_P1_ROUTE_HC6: 0x40010306 | B0_P1_ROUTE_HC7: 0x40010307 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|------------------------------|------------------------------|
| B0_P1_ROUTE_HC8: 0x40010308 | B0_P1_ROUTE_HC9: 0x40010309 |
| B0_P1_ROUTE_HC10: 0x4001030A | B0_P1_ROUTE_HC11: 0x4001030B |
| B0_P1_ROUTE_HC12: 0x4001030C | B0_P1_ROUTE_HC13: 0x4001030D |
| B0_P1_ROUTE_HC14: 0x4001030E | B0_P1_ROUTE_HC15: 0x4001030F |
| B0_P1_ROUTE_HC16: 0x40010310 | B0_P1_ROUTE_HC17: 0x40010311 |
| B0_P1_ROUTE_HC18: 0x40010312 | B0_P1_ROUTE_HC19: 0x40010313 |
| B0_P1_ROUTE_HC20: 0x40010314 | B0_P1_ROUTE_HC21: 0x40010315 |
| B0_P1_ROUTE_HC22: 0x40010316 | B0_P1_ROUTE_HC23: 0x40010317 |
| B0_P1_ROUTE_HC24: 0x40010318 | B0_P1_ROUTE_HC25: 0x40010319 |
| B0_P1_ROUTE_HC26: 0x4001031A | B0_P1_ROUTE_HC27: 0x4001031B |
| B0_P1_ROUTE_HC28: 0x4001031C | B0_P1_ROUTE_HC29: 0x4001031D |
| B0_P1_ROUTE_HC30: 0x4001031E | B0_P1_ROUTE_HC31: 0x4001031F |
| B0_P1_ROUTE_HC32: 0x40010320 | B0_P1_ROUTE_HC33: 0x40010321 |
| B0_P1_ROUTE_HC34: 0x40010322 | B0_P1_ROUTE_HC35: 0x40010323 |
| B0_P1_ROUTE_HC36: 0x40010324 | B0_P1_ROUTE_HC37: 0x40010325 |
| B0_P1_ROUTE_HC38: 0x40010326 | B0_P1_ROUTE_HC39: 0x40010327 |
| B0_P1_ROUTE_HC40: 0x40010328 | B0_P1_ROUTE_HC41: 0x40010329 |
| B0_P1_ROUTE_HC42: 0x4001032A | B0_P1_ROUTE_HC43: 0x4001032B |
| B0_P1_ROUTE_HC44: 0x4001032C | B0_P1_ROUTE_HC45: 0x4001032D |
| B0_P1_ROUTE_HC46: 0x4001032E | B0_P1_ROUTE_HC47: 0x4001032F |
| B0_P1_ROUTE_HC48: 0x40010330 | B0_P1_ROUTE_HC49: 0x40010331 |
| B0_P1_ROUTE_HC50: 0x40010332 | B0_P1_ROUTE_HC51: 0x40010333 |
| B0_P1_ROUTE_HC52: 0x40010334 | B0_P1_ROUTE_HC53: 0x40010335 |
| B0_P1_ROUTE_HC54: 0x40010336 | B0_P1_ROUTE_HC55: 0x40010337 |
| B0_P1_ROUTE_HC56: 0x40010338 | B0_P1_ROUTE_HC57: 0x40010339 |
| B0_P1_ROUTE_HC58: 0x4001033A | B0_P1_ROUTE_HC59: 0x4001033B |
| B0_P1_ROUTE_HC60: 0x4001033C | B0_P1_ROUTE_HC61: 0x4001033D |
| B0_P1_ROUTE_HC62: 0x4001033E | B0_P1_ROUTE_HC63: 0x4001033F |
| B0_P1_ROUTE_HC64: 0x40010340 | B0_P1_ROUTE_HC65: 0x40010341 |
| B0_P1_ROUTE_HC66: 0x40010342 | B0_P1_ROUTE_HC67: 0x40010343 |
| B0_P1_ROUTE_HC68: 0x40010344 | B0_P1_ROUTE_HC69: 0x40010345 |
| B0_P1_ROUTE_HC70: 0x40010346 | B0_P1_ROUTE_HC71: 0x40010347 |
| B0_P1_ROUTE_HC72: 0x40010348 | B0_P1_ROUTE_HC73: 0x40010349 |
| B0_P1_ROUTE_HC74: 0x4001034A | B0_P1_ROUTE_HC75: 0x4001034B |
| B0_P1_ROUTE_HC76: 0x4001034C | B0_P1_ROUTE_HC77: 0x4001034D |
| B0_P1_ROUTE_HC78: 0x4001034E | B0_P1_ROUTE_HC79: 0x4001034F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B0_P1_ROUTE_HC80: 0x40010350 | B0_P1_ROUTE_HC81: 0x40010351 |
| B0_P1_ROUTE_HC82: 0x40010352 | B0_P1_ROUTE_HC83: 0x40010353 |
| B0_P1_ROUTE_HC84: 0x40010354 | B0_P1_ROUTE_HC85: 0x40010355 |
| B0_P1_ROUTE_HC86: 0x40010356 | B0_P1_ROUTE_HC87: 0x40010357 |
| B0_P1_ROUTE_HC88: 0x40010358 | B0_P1_ROUTE_HC89: 0x40010359 |
| B0_P1_ROUTE_HC90: 0x4001035A | B0_P1_ROUTE_HC91: 0x4001035B |
| B0_P1_ROUTE_HC92: 0x4001035C | B0_P1_ROUTE_HC93: 0x4001035D |
| B0_P1_ROUTE_HC94: 0x4001035E | B0_P1_ROUTE_HC95: 0x4001035F |
| B0_P1_ROUTE_HC96: 0x40010360 | B0_P1_ROUTE_HC97: 0x40010361 |
| B0_P1_ROUTE_HC98: 0x40010362 | B0_P1_ROUTE_HC99: 0x40010363 |
| B0_P1_ROUTE_HC100: 0x40010364 | B0_P1_ROUTE_HC101: 0x40010365 |
| B0_P1_ROUTE_HC102: 0x40010366 | B0_P1_ROUTE_HC103: 0x40010367 |
| B0_P1_ROUTE_HC104: 0x40010368 | B0_P1_ROUTE_HC105: 0x40010369 |
| B0_P1_ROUTE_HC106: 0x4001036A | B0_P1_ROUTE_HC107: 0x4001036B |
| B0_P1_ROUTE_HC108: 0x4001036C | B0_P1_ROUTE_HC109: 0x4001036D |
| B0_P1_ROUTE_HC110: 0x4001036E | B0_P1_ROUTE_HC111: 0x4001036F |
| B0_P1_ROUTE_HC112: 0x40010370 | B0_P1_ROUTE_HC113: 0x40010371 |
| B0_P1_ROUTE_HC114: 0x40010372 | B0_P1_ROUTE_HC115: 0x40010373 |
| B0_P1_ROUTE_HC116: 0x40010374 | B0_P1_ROUTE_HC117: 0x40010375 |
| B0_P1_ROUTE_HC118: 0x40010376 | B0_P1_ROUTE_HC119: 0x40010377 |
| B0_P1_ROUTE_HC120: 0x40010378 | B0_P1_ROUTE_HC121: 0x40010379 |
| B0_P1_ROUTE_HC122: 0x4001037A | B0_P1_ROUTE_HC123: 0x4001037B |
| B0_P1_ROUTE_HC124: 0x4001037C | B0_P1_ROUTE_HC125: 0x4001037D |
| B0_P1_ROUTE_HC126: 0x4001037E | B0_P1_ROUTE_HC127: 0x4001037F |
| B0_P2_ROUTE_HC0: 0x40010500 | B0_P2_ROUTE_HC1: 0x40010501 |
| B0_P2_ROUTE_HC2: 0x40010502 | B0_P2_ROUTE_HC3: 0x40010503 |
| B0_P2_ROUTE_HC4: 0x40010504 | B0_P2_ROUTE_HC5: 0x40010505 |
| B0_P2_ROUTE_HC6: 0x40010506 | B0_P2_ROUTE_HC7: 0x40010507 |
| B0_P2_ROUTE_HC8: 0x40010508 | B0_P2_ROUTE_HC9: 0x40010509 |
| B0_P2_ROUTE_HC10: 0x4001050A | B0_P2_ROUTE_HC11: 0x4001050B |
| B0_P2_ROUTE_HC12: 0x4001050C | B0_P2_ROUTE_HC13: 0x4001050D |
| B0_P2_ROUTE_HC14: 0x4001050E | B0_P2_ROUTE_HC15: 0x4001050F |
| B0_P2_ROUTE_HC16: 0x40010510 | B0_P2_ROUTE_HC17: 0x40010511 |
| B0_P2_ROUTE_HC18: 0x40010512 | B0_P2_ROUTE_HC19: 0x40010513 |
| B0_P2_ROUTE_HC20: 0x40010514 | B0_P2_ROUTE_HC21: 0x40010515 |
| B0_P2_ROUTE_HC22: 0x40010516 | B0_P2_ROUTE_HC23: 0x40010517 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|------------------------------|------------------------------|
| B0_P2_ROUTE_HC24: 0x40010518 | B0_P2_ROUTE_HC25: 0x40010519 |
| B0_P2_ROUTE_HC26: 0x4001051A | B0_P2_ROUTE_HC27: 0x4001051B |
| B0_P2_ROUTE_HC28: 0x4001051C | B0_P2_ROUTE_HC29: 0x4001051D |
| B0_P2_ROUTE_HC30: 0x4001051E | B0_P2_ROUTE_HC31: 0x4001051F |
| B0_P2_ROUTE_HC32: 0x40010520 | B0_P2_ROUTE_HC33: 0x40010521 |
| B0_P2_ROUTE_HC34: 0x40010522 | B0_P2_ROUTE_HC35: 0x40010523 |
| B0_P2_ROUTE_HC36: 0x40010524 | B0_P2_ROUTE_HC37: 0x40010525 |
| B0_P2_ROUTE_HC38: 0x40010526 | B0_P2_ROUTE_HC39: 0x40010527 |
| B0_P2_ROUTE_HC40: 0x40010528 | B0_P2_ROUTE_HC41: 0x40010529 |
| B0_P2_ROUTE_HC42: 0x4001052A | B0_P2_ROUTE_HC43: 0x4001052B |
| B0_P2_ROUTE_HC44: 0x4001052C | B0_P2_ROUTE_HC45: 0x4001052D |
| B0_P2_ROUTE_HC46: 0x4001052E | B0_P2_ROUTE_HC47: 0x4001052F |
| B0_P2_ROUTE_HC48: 0x40010530 | B0_P2_ROUTE_HC49: 0x40010531 |
| B0_P2_ROUTE_HC50: 0x40010532 | B0_P2_ROUTE_HC51: 0x40010533 |
| B0_P2_ROUTE_HC52: 0x40010534 | B0_P2_ROUTE_HC53: 0x40010535 |
| B0_P2_ROUTE_HC54: 0x40010536 | B0_P2_ROUTE_HC55: 0x40010537 |
| B0_P2_ROUTE_HC56: 0x40010538 | B0_P2_ROUTE_HC57: 0x40010539 |
| B0_P2_ROUTE_HC58: 0x4001053A | B0_P2_ROUTE_HC59: 0x4001053B |
| B0_P2_ROUTE_HC60: 0x4001053C | B0_P2_ROUTE_HC61: 0x4001053D |
| B0_P2_ROUTE_HC62: 0x4001053E | B0_P2_ROUTE_HC63: 0x4001053F |
| B0_P2_ROUTE_HC64: 0x40010540 | B0_P2_ROUTE_HC65: 0x40010541 |
| B0_P2_ROUTE_HC66: 0x40010542 | B0_P2_ROUTE_HC67: 0x40010543 |
| B0_P2_ROUTE_HC68: 0x40010544 | B0_P2_ROUTE_HC69: 0x40010545 |
| B0_P2_ROUTE_HC70: 0x40010546 | B0_P2_ROUTE_HC71: 0x40010547 |
| B0_P2_ROUTE_HC72: 0x40010548 | B0_P2_ROUTE_HC73: 0x40010549 |
| B0_P2_ROUTE_HC74: 0x4001054A | B0_P2_ROUTE_HC75: 0x4001054B |
| B0_P2_ROUTE_HC76: 0x4001054C | B0_P2_ROUTE_HC77: 0x4001054D |
| B0_P2_ROUTE_HC78: 0x4001054E | B0_P2_ROUTE_HC79: 0x4001054F |
| B0_P2_ROUTE_HC80: 0x40010550 | B0_P2_ROUTE_HC81: 0x40010551 |
| B0_P2_ROUTE_HC82: 0x40010552 | B0_P2_ROUTE_HC83: 0x40010553 |
| B0_P2_ROUTE_HC84: 0x40010554 | B0_P2_ROUTE_HC85: 0x40010555 |
| B0_P2_ROUTE_HC86: 0x40010556 | B0_P2_ROUTE_HC87: 0x40010557 |
| B0_P2_ROUTE_HC88: 0x40010558 | B0_P2_ROUTE_HC89: 0x40010559 |
| B0_P2_ROUTE_HC90: 0x4001055A | B0_P2_ROUTE_HC91: 0x4001055B |
| B0_P2_ROUTE_HC92: 0x4001055C | B0_P2_ROUTE_HC93: 0x4001055D |
| B0_P2_ROUTE_HC94: 0x4001055E | B0_P2_ROUTE_HC95: 0x4001055F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
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| B0_P2_ROUTE_HC96: 0x40010560 | B0_P2_ROUTE_HC97: 0x40010561 |
| B0_P2_ROUTE_HC98: 0x40010562 | B0_P2_ROUTE_HC99: 0x40010563 |
| B0_P2_ROUTE_HC100: 0x40010564 | B0_P2_ROUTE_HC101: 0x40010565 |
| B0_P2_ROUTE_HC102: 0x40010566 | B0_P2_ROUTE_HC103: 0x40010567 |
| B0_P2_ROUTE_HC104: 0x40010568 | B0_P2_ROUTE_HC105: 0x40010569 |
| B0_P2_ROUTE_HC106: 0x4001056A | B0_P2_ROUTE_HC107: 0x4001056B |
| B0_P2_ROUTE_HC108: 0x4001056C | B0_P2_ROUTE_HC109: 0x4001056D |
| B0_P2_ROUTE_HC110: 0x4001056E | B0_P2_ROUTE_HC111: 0x4001056F |
| B0_P2_ROUTE_HC112: 0x40010570 | B0_P2_ROUTE_HC113: 0x40010571 |
| B0_P2_ROUTE_HC114: 0x40010572 | B0_P2_ROUTE_HC115: 0x40010573 |
| B0_P2_ROUTE_HC116: 0x40010574 | B0_P2_ROUTE_HC117: 0x40010575 |
| B0_P2_ROUTE_HC118: 0x40010576 | B0_P2_ROUTE_HC119: 0x40010577 |
| B0_P2_ROUTE_HC120: 0x40010578 | B0_P2_ROUTE_HC121: 0x40010579 |
| B0_P2_ROUTE_HC122: 0x4001057A | B0_P2_ROUTE_HC123: 0x4001057B |
| B0_P2_ROUTE_HC124: 0x4001057C | B0_P2_ROUTE_HC125: 0x4001057D |
| B0_P2_ROUTE_HC126: 0x4001057E | B0_P2_ROUTE_HC127: 0x4001057F |
| B0_P3_ROUTE_HC0: 0x40010700 | B0_P3_ROUTE_HC1: 0x40010701 |
| B0_P3_ROUTE_HC2: 0x40010702 | B0_P3_ROUTE_HC3: 0x40010703 |
| B0_P3_ROUTE_HC4: 0x40010704 | B0_P3_ROUTE_HC5: 0x40010705 |
| B0_P3_ROUTE_HC6: 0x40010706 | B0_P3_ROUTE_HC7: 0x40010707 |
| B0_P3_ROUTE_HC8: 0x40010708 | B0_P3_ROUTE_HC9: 0x40010709 |
| B0_P3_ROUTE_HC10: 0x4001070A | B0_P3_ROUTE_HC11: 0x4001070B |
| B0_P3_ROUTE_HC12: 0x4001070C | B0_P3_ROUTE_HC13: 0x4001070D |
| B0_P3_ROUTE_HC14: 0x4001070E | B0_P3_ROUTE_HC15: 0x4001070F |
| B0_P3_ROUTE_HC16: 0x40010710 | B0_P3_ROUTE_HC17: 0x40010711 |
| B0_P3_ROUTE_HC18: 0x40010712 | B0_P3_ROUTE_HC19: 0x40010713 |
| B0_P3_ROUTE_HC20: 0x40010714 | B0_P3_ROUTE_HC21: 0x40010715 |
| B0_P3_ROUTE_HC22: 0x40010716 | B0_P3_ROUTE_HC23: 0x40010717 |
| B0_P3_ROUTE_HC24: 0x40010718 | B0_P3_ROUTE_HC25: 0x40010719 |
| B0_P3_ROUTE_HC26: 0x4001071A | B0_P3_ROUTE_HC27: 0x4001071B |
| B0_P3_ROUTE_HC28: 0x4001071C | B0_P3_ROUTE_HC29: 0x4001071D |
| B0_P3_ROUTE_HC30: 0x4001071E | B0_P3_ROUTE_HC31: 0x4001071F |
| B0_P3_ROUTE_HC32: 0x40010720 | B0_P3_ROUTE_HC33: 0x40010721 |
| B0_P3_ROUTE_HC34: 0x40010722 | B0_P3_ROUTE_HC35: 0x40010723 |
| B0_P3_ROUTE_HC36: 0x40010724 | B0_P3_ROUTE_HC37: 0x40010725 |
| B0_P3_ROUTE_HC38: 0x40010726 | B0_P3_ROUTE_HC39: 0x40010727 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

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| B0_P3_ROUTE_HC40: 0x40010728 | B0_P3_ROUTE_HC41: 0x40010729 |
| B0_P3_ROUTE_HC42: 0x4001072A | B0_P3_ROUTE_HC43: 0x4001072B |
| B0_P3_ROUTE_HC44: 0x4001072C | B0_P3_ROUTE_HC45: 0x4001072D |
| B0_P3_ROUTE_HC46: 0x4001072E | B0_P3_ROUTE_HC47: 0x4001072F |
| B0_P3_ROUTE_HC48: 0x40010730 | B0_P3_ROUTE_HC49: 0x40010731 |
| B0_P3_ROUTE_HC50: 0x40010732 | B0_P3_ROUTE_HC51: 0x40010733 |
| B0_P3_ROUTE_HC52: 0x40010734 | B0_P3_ROUTE_HC53: 0x40010735 |
| B0_P3_ROUTE_HC54: 0x40010736 | B0_P3_ROUTE_HC55: 0x40010737 |
| B0_P3_ROUTE_HC56: 0x40010738 | B0_P3_ROUTE_HC57: 0x40010739 |
| B0_P3_ROUTE_HC58: 0x4001073A | B0_P3_ROUTE_HC59: 0x4001073B |
| B0_P3_ROUTE_HC60: 0x4001073C | B0_P3_ROUTE_HC61: 0x4001073D |
| B0_P3_ROUTE_HC62: 0x4001073E | B0_P3_ROUTE_HC63: 0x4001073F |
| B0_P3_ROUTE_HC64: 0x40010740 | B0_P3_ROUTE_HC65: 0x40010741 |
| B0_P3_ROUTE_HC66: 0x40010742 | B0_P3_ROUTE_HC67: 0x40010743 |
| B0_P3_ROUTE_HC68: 0x40010744 | B0_P3_ROUTE_HC69: 0x40010745 |
| B0_P3_ROUTE_HC70: 0x40010746 | B0_P3_ROUTE_HC71: 0x40010747 |
| B0_P3_ROUTE_HC72: 0x40010748 | B0_P3_ROUTE_HC73: 0x40010749 |
| B0_P3_ROUTE_HC74: 0x4001074A | B0_P3_ROUTE_HC75: 0x4001074B |
| B0_P3_ROUTE_HC76: 0x4001074C | B0_P3_ROUTE_HC77: 0x4001074D |
| B0_P3_ROUTE_HC78: 0x4001074E | B0_P3_ROUTE_HC79: 0x4001074F |
| B0_P3_ROUTE_HC80: 0x40010750 | B0_P3_ROUTE_HC81: 0x40010751 |
| B0_P3_ROUTE_HC82: 0x40010752 | B0_P3_ROUTE_HC83: 0x40010753 |
| B0_P3_ROUTE_HC84: 0x40010754 | B0_P3_ROUTE_HC85: 0x40010755 |
| B0_P3_ROUTE_HC86: 0x40010756 | B0_P3_ROUTE_HC87: 0x40010757 |
| B0_P3_ROUTE_HC88: 0x40010758 | B0_P3_ROUTE_HC89: 0x40010759 |
| B0_P3_ROUTE_HC90: 0x4001075A | B0_P3_ROUTE_HC91: 0x4001075B |
| B0_P3_ROUTE_HC92: 0x4001075C | B0_P3_ROUTE_HC93: 0x4001075D |
| B0_P3_ROUTE_HC94: 0x4001075E | B0_P3_ROUTE_HC95: 0x4001075F |
| B0_P3_ROUTE_HC96: 0x40010760 | B0_P3_ROUTE_HC97: 0x40010761 |
| B0_P3_ROUTE_HC98: 0x40010762 | B0_P3_ROUTE_HC99: 0x40010763 |
| B0_P3_ROUTE_HC100: 0x40010764 | B0_P3_ROUTE_HC101: 0x40010765 |
| B0_P3_ROUTE_HC102: 0x40010766 | B0_P3_ROUTE_HC103: 0x40010767 |
| B0_P3_ROUTE_HC104: 0x40010768 | B0_P3_ROUTE_HC105: 0x40010769 |
| B0_P3_ROUTE_HC106: 0x4001076A | B0_P3_ROUTE_HC107: 0x4001076B |
| B0_P3_ROUTE_HC108: 0x4001076C | B0_P3_ROUTE_HC109: 0x4001076D |
| B0_P3_ROUTE_HC110: 0x4001076E | B0_P3_ROUTE_HC111: 0x4001076F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B0_P3_ROUTE_HC112: 0x40010770 | B0_P3_ROUTE_HC113: 0x40010771 |
| B0_P3_ROUTE_HC114: 0x40010772 | B0_P3_ROUTE_HC115: 0x40010773 |
| B0_P3_ROUTE_HC116: 0x40010774 | B0_P3_ROUTE_HC117: 0x40010775 |
| B0_P3_ROUTE_HC118: 0x40010776 | B0_P3_ROUTE_HC119: 0x40010777 |
| B0_P3_ROUTE_HC120: 0x40010778 | B0_P3_ROUTE_HC121: 0x40010779 |
| B0_P3_ROUTE_HC122: 0x4001077A | B0_P3_ROUTE_HC123: 0x4001077B |
| B0_P3_ROUTE_HC124: 0x4001077C | B0_P3_ROUTE_HC125: 0x4001077D |
| B0_P3_ROUTE_HC126: 0x4001077E | B0_P3_ROUTE_HC127: 0x4001077F |
| B0_P4_ROUTE_HC0: 0x40010900 | B0_P4_ROUTE_HC1: 0x40010901 |
| B0_P4_ROUTE_HC2: 0x40010902 | B0_P4_ROUTE_HC3: 0x40010903 |
| B0_P4_ROUTE_HC4: 0x40010904 | B0_P4_ROUTE_HC5: 0x40010905 |
| B0_P4_ROUTE_HC6: 0x40010906 | B0_P4_ROUTE_HC7: 0x40010907 |
| B0_P4_ROUTE_HC8: 0x40010908 | B0_P4_ROUTE_HC9: 0x40010909 |
| B0_P4_ROUTE_HC10: 0x4001090A | B0_P4_ROUTE_HC11: 0x4001090B |
| B0_P4_ROUTE_HC12: 0x4001090C | B0_P4_ROUTE_HC13: 0x4001090D |
| B0_P4_ROUTE_HC14: 0x4001090E | B0_P4_ROUTE_HC15: 0x4001090F |
| B0_P4_ROUTE_HC16: 0x40010910 | B0_P4_ROUTE_HC17: 0x40010911 |
| B0_P4_ROUTE_HC18: 0x40010912 | B0_P4_ROUTE_HC19: 0x40010913 |
| B0_P4_ROUTE_HC20: 0x40010914 | B0_P4_ROUTE_HC21: 0x40010915 |
| B0_P4_ROUTE_HC22: 0x40010916 | B0_P4_ROUTE_HC23: 0x40010917 |
| B0_P4_ROUTE_HC24: 0x40010918 | B0_P4_ROUTE_HC25: 0x40010919 |
| B0_P4_ROUTE_HC26: 0x4001091A | B0_P4_ROUTE_HC27: 0x4001091B |
| B0_P4_ROUTE_HC28: 0x4001091C | B0_P4_ROUTE_HC29: 0x4001091D |
| B0_P4_ROUTE_HC30: 0x4001091E | B0_P4_ROUTE_HC31: 0x4001091F |
| B0_P4_ROUTE_HC32: 0x40010920 | B0_P4_ROUTE_HC33: 0x40010921 |
| B0_P4_ROUTE_HC34: 0x40010922 | B0_P4_ROUTE_HC35: 0x40010923 |
| B0_P4_ROUTE_HC36: 0x40010924 | B0_P4_ROUTE_HC37: 0x40010925 |
| B0_P4_ROUTE_HC38: 0x40010926 | B0_P4_ROUTE_HC39: 0x40010927 |
| B0_P4_ROUTE_HC40: 0x40010928 | B0_P4_ROUTE_HC41: 0x40010929 |
| B0_P4_ROUTE_HC42: 0x4001092A | B0_P4_ROUTE_HC43: 0x4001092B |
| B0_P4_ROUTE_HC44: 0x4001092C | B0_P4_ROUTE_HC45: 0x4001092D |
| B0_P4_ROUTE_HC46: 0x4001092E | B0_P4_ROUTE_HC47: 0x4001092F |
| B0_P4_ROUTE_HC48: 0x40010930 | B0_P4_ROUTE_HC49: 0x40010931 |
| B0_P4_ROUTE_HC50: 0x40010932 | B0_P4_ROUTE_HC51: 0x40010933 |
| B0_P4_ROUTE_HC52: 0x40010934 | B0_P4_ROUTE_HC53: 0x40010935 |
| B0_P4_ROUTE_HC54: 0x40010936 | B0_P4_ROUTE_HC55: 0x40010937 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B0_P4_ROUTE_HC56: 0x40010938 | B0_P4_ROUTE_HC57: 0x40010939 |
| B0_P4_ROUTE_HC58: 0x4001093A | B0_P4_ROUTE_HC59: 0x4001093B |
| B0_P4_ROUTE_HC60: 0x4001093C | B0_P4_ROUTE_HC61: 0x4001093D |
| B0_P4_ROUTE_HC62: 0x4001093E | B0_P4_ROUTE_HC63: 0x4001093F |
| B0_P4_ROUTE_HC64: 0x40010940 | B0_P4_ROUTE_HC65: 0x40010941 |
| B0_P4_ROUTE_HC66: 0x40010942 | B0_P4_ROUTE_HC67: 0x40010943 |
| B0_P4_ROUTE_HC68: 0x40010944 | B0_P4_ROUTE_HC69: 0x40010945 |
| B0_P4_ROUTE_HC70: 0x40010946 | B0_P4_ROUTE_HC71: 0x40010947 |
| B0_P4_ROUTE_HC72: 0x40010948 | B0_P4_ROUTE_HC73: 0x40010949 |
| B0_P4_ROUTE_HC74: 0x4001094A | B0_P4_ROUTE_HC75: 0x4001094B |
| B0_P4_ROUTE_HC76: 0x4001094C | B0_P4_ROUTE_HC77: 0x4001094D |
| B0_P4_ROUTE_HC78: 0x4001094E | B0_P4_ROUTE_HC79: 0x4001094F |
| B0_P4_ROUTE_HC80: 0x40010950 | B0_P4_ROUTE_HC81: 0x40010951 |
| B0_P4_ROUTE_HC82: 0x40010952 | B0_P4_ROUTE_HC83: 0x40010953 |
| B0_P4_ROUTE_HC84: 0x40010954 | B0_P4_ROUTE_HC85: 0x40010955 |
| B0_P4_ROUTE_HC86: 0x40010956 | B0_P4_ROUTE_HC87: 0x40010957 |
| B0_P4_ROUTE_HC88: 0x40010958 | B0_P4_ROUTE_HC89: 0x40010959 |
| B0_P4_ROUTE_HC90: 0x4001095A | B0_P4_ROUTE_HC91: 0x4001095B |
| B0_P4_ROUTE_HC92: 0x4001095C | B0_P4_ROUTE_HC93: 0x4001095D |
| B0_P4_ROUTE_HC94: 0x4001095E | B0_P4_ROUTE_HC95: 0x4001095F |
| B0_P4_ROUTE_HC96: 0x40010960 | B0_P4_ROUTE_HC97: 0x40010961 |
| B0_P4_ROUTE_HC98: 0x40010962 | B0_P4_ROUTE_HC99: 0x40010963 |
| B0_P4_ROUTE_HC100: 0x40010964 | B0_P4_ROUTE_HC101: 0x40010965 |
| B0_P4_ROUTE_HC102: 0x40010966 | B0_P4_ROUTE_HC103: 0x40010967 |
| B0_P4_ROUTE_HC104: 0x40010968 | B0_P4_ROUTE_HC105: 0x40010969 |
| B0_P4_ROUTE_HC106: 0x4001096A | B0_P4_ROUTE_HC107: 0x4001096B |
| B0_P4_ROUTE_HC108: 0x4001096C | B0_P4_ROUTE_HC109: 0x4001096D |
| B0_P4_ROUTE_HC110: 0x4001096E | B0_P4_ROUTE_HC111: 0x4001096F |
| B0_P4_ROUTE_HC112: 0x40010970 | B0_P4_ROUTE_HC113: 0x40010971 |
| B0_P4_ROUTE_HC114: 0x40010972 | B0_P4_ROUTE_HC115: 0x40010973 |
| B0_P4_ROUTE_HC116: 0x40010974 | B0_P4_ROUTE_HC117: 0x40010975 |
| B0_P4_ROUTE_HC118: 0x40010976 | B0_P4_ROUTE_HC119: 0x40010977 |
| B0_P4_ROUTE_HC120: 0x40010978 | B0_P4_ROUTE_HC121: 0x40010979 |
| B0_P4_ROUTE_HC122: 0x4001097A | B0_P4_ROUTE_HC123: 0x4001097B |
| B0_P4_ROUTE_HC124: 0x4001097C | B0_P4_ROUTE_HC125: 0x4001097D |
| B0_P4_ROUTE_HC126: 0x4001097E | B0_P4_ROUTE_HC127: 0x4001097F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

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|------------------------------|------------------------------|
| B0_P5_ROUTE_HC0: 0x40010B00 | B0_P5_ROUTE_HC1: 0x40010B01 |
| B0_P5_ROUTE_HC2: 0x40010B02 | B0_P5_ROUTE_HC3: 0x40010B03 |
| B0_P5_ROUTE_HC4: 0x40010B04 | B0_P5_ROUTE_HC5: 0x40010B05 |
| B0_P5_ROUTE_HC6: 0x40010B06 | B0_P5_ROUTE_HC7: 0x40010B07 |
| B0_P5_ROUTE_HC8: 0x40010B08 | B0_P5_ROUTE_HC9: 0x40010B09 |
| B0_P5_ROUTE_HC10: 0x40010B0A | B0_P5_ROUTE_HC11: 0x40010B0B |
| B0_P5_ROUTE_HC12: 0x40010B0C | B0_P5_ROUTE_HC13: 0x40010B0D |
| B0_P5_ROUTE_HC14: 0x40010B0E | B0_P5_ROUTE_HC15: 0x40010B0F |
| B0_P5_ROUTE_HC16: 0x40010B10 | B0_P5_ROUTE_HC17: 0x40010B11 |
| B0_P5_ROUTE_HC18: 0x40010B12 | B0_P5_ROUTE_HC19: 0x40010B13 |
| B0_P5_ROUTE_HC20: 0x40010B14 | B0_P5_ROUTE_HC21: 0x40010B15 |
| B0_P5_ROUTE_HC22: 0x40010B16 | B0_P5_ROUTE_HC23: 0x40010B17 |
| B0_P5_ROUTE_HC24: 0x40010B18 | B0_P5_ROUTE_HC25: 0x40010B19 |
| B0_P5_ROUTE_HC26: 0x40010B1A | B0_P5_ROUTE_HC27: 0x40010B1B |
| B0_P5_ROUTE_HC28: 0x40010B1C | B0_P5_ROUTE_HC29: 0x40010B1D |
| B0_P5_ROUTE_HC30: 0x40010B1E | B0_P5_ROUTE_HC31: 0x40010B1F |
| B0_P5_ROUTE_HC32: 0x40010B20 | B0_P5_ROUTE_HC33: 0x40010B21 |
| B0_P5_ROUTE_HC34: 0x40010B22 | B0_P5_ROUTE_HC35: 0x40010B23 |
| B0_P5_ROUTE_HC36: 0x40010B24 | B0_P5_ROUTE_HC37: 0x40010B25 |
| B0_P5_ROUTE_HC38: 0x40010B26 | B0_P5_ROUTE_HC39: 0x40010B27 |
| B0_P5_ROUTE_HC40: 0x40010B28 | B0_P5_ROUTE_HC41: 0x40010B29 |
| B0_P5_ROUTE_HC42: 0x40010B2A | B0_P5_ROUTE_HC43: 0x40010B2B |
| B0_P5_ROUTE_HC44: 0x40010B2C | B0_P5_ROUTE_HC45: 0x40010B2D |
| B0_P5_ROUTE_HC46: 0x40010B2E | B0_P5_ROUTE_HC47: 0x40010B2F |
| B0_P5_ROUTE_HC48: 0x40010B30 | B0_P5_ROUTE_HC49: 0x40010B31 |
| B0_P5_ROUTE_HC50: 0x40010B32 | B0_P5_ROUTE_HC51: 0x40010B33 |
| B0_P5_ROUTE_HC52: 0x40010B34 | B0_P5_ROUTE_HC53: 0x40010B35 |
| B0_P5_ROUTE_HC54: 0x40010B36 | B0_P5_ROUTE_HC55: 0x40010B37 |
| B0_P5_ROUTE_HC56: 0x40010B38 | B0_P5_ROUTE_HC57: 0x40010B39 |
| B0_P5_ROUTE_HC58: 0x40010B3A | B0_P5_ROUTE_HC59: 0x40010B3B |
| B0_P5_ROUTE_HC60: 0x40010B3C | B0_P5_ROUTE_HC61: 0x40010B3D |
| B0_P5_ROUTE_HC62: 0x40010B3E | B0_P5_ROUTE_HC63: 0x40010B3F |
| B0_P5_ROUTE_HC64: 0x40010B40 | B0_P5_ROUTE_HC65: 0x40010B41 |
| B0_P5_ROUTE_HC66: 0x40010B42 | B0_P5_ROUTE_HC67: 0x40010B43 |
| B0_P5_ROUTE_HC68: 0x40010B44 | B0_P5_ROUTE_HC69: 0x40010B45 |
| B0_P5_ROUTE_HC70: 0x40010B46 | B0_P5_ROUTE_HC71: 0x40010B47 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

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| B0_P5_ROUTE_HC72: 0x40010B48 | B0_P5_ROUTE_HC73: 0x40010B49 |
| B0_P5_ROUTE_HC74: 0x40010B4A | B0_P5_ROUTE_HC75: 0x40010B4B |
| B0_P5_ROUTE_HC76: 0x40010B4C | B0_P5_ROUTE_HC77: 0x40010B4D |
| B0_P5_ROUTE_HC78: 0x40010B4E | B0_P5_ROUTE_HC79: 0x40010B4F |
| B0_P5_ROUTE_HC80: 0x40010B50 | B0_P5_ROUTE_HC81: 0x40010B51 |
| B0_P5_ROUTE_HC82: 0x40010B52 | B0_P5_ROUTE_HC83: 0x40010B53 |
| B0_P5_ROUTE_HC84: 0x40010B54 | B0_P5_ROUTE_HC85: 0x40010B55 |
| B0_P5_ROUTE_HC86: 0x40010B56 | B0_P5_ROUTE_HC87: 0x40010B57 |
| B0_P5_ROUTE_HC88: 0x40010B58 | B0_P5_ROUTE_HC89: 0x40010B59 |
| B0_P5_ROUTE_HC90: 0x40010B5A | B0_P5_ROUTE_HC91: 0x40010B5B |
| B0_P5_ROUTE_HC92: 0x40010B5C | B0_P5_ROUTE_HC93: 0x40010B5D |
| B0_P5_ROUTE_HC94: 0x40010B5E | B0_P5_ROUTE_HC95: 0x40010B5F |
| B0_P5_ROUTE_HC96: 0x40010B60 | B0_P5_ROUTE_HC97: 0x40010B61 |
| B0_P5_ROUTE_HC98: 0x40010B62 | B0_P5_ROUTE_HC99: 0x40010B63 |
| B0_P5_ROUTE_HC100: 0x40010B64 | B0_P5_ROUTE_HC101: 0x40010B65 |
| B0_P5_ROUTE_HC102: 0x40010B66 | B0_P5_ROUTE_HC103: 0x40010B67 |
| B0_P5_ROUTE_HC104: 0x40010B68 | B0_P5_ROUTE_HC105: 0x40010B69 |
| B0_P5_ROUTE_HC106: 0x40010B6A | B0_P5_ROUTE_HC107: 0x40010B6B |
| B0_P5_ROUTE_HC108: 0x40010B6C | B0_P5_ROUTE_HC109: 0x40010B6D |
| B0_P5_ROUTE_HC110: 0x40010B6E | B0_P5_ROUTE_HC111: 0x40010B6F |
| B0_P5_ROUTE_HC112: 0x40010B70 | B0_P5_ROUTE_HC113: 0x40010B71 |
| B0_P5_ROUTE_HC114: 0x40010B72 | B0_P5_ROUTE_HC115: 0x40010B73 |
| B0_P5_ROUTE_HC116: 0x40010B74 | B0_P5_ROUTE_HC117: 0x40010B75 |
| B0_P5_ROUTE_HC118: 0x40010B76 | B0_P5_ROUTE_HC119: 0x40010B77 |
| B0_P5_ROUTE_HC120: 0x40010B78 | B0_P5_ROUTE_HC121: 0x40010B79 |
| B0_P5_ROUTE_HC122: 0x40010B7A | B0_P5_ROUTE_HC123: 0x40010B7B |
| B0_P5_ROUTE_HC124: 0x40010B7C | B0_P5_ROUTE_HC125: 0x40010B7D |
| B0_P5_ROUTE_HC126: 0x40010B7E | B0_P5_ROUTE_HC127: 0x40010B7F |
| B0_P6_ROUTE_HC0: 0x40010D00 | B0_P6_ROUTE_HC1: 0x40010D01 |
| B0_P6_ROUTE_HC2: 0x40010D02 | B0_P6_ROUTE_HC3: 0x40010D03 |
| B0_P6_ROUTE_HC4: 0x40010D04 | B0_P6_ROUTE_HC5: 0x40010D05 |
| B0_P6_ROUTE_HC6: 0x40010D06 | B0_P6_ROUTE_HC7: 0x40010D07 |
| B0_P6_ROUTE_HC8: 0x40010D08 | B0_P6_ROUTE_HC9: 0x40010D09 |
| B0_P6_ROUTE_HC10: 0x40010D0A | B0_P6_ROUTE_HC11: 0x40010D0B |
| B0_P6_ROUTE_HC12: 0x40010D0C | B0_P6_ROUTE_HC13: 0x40010D0D |
| B0_P6_ROUTE_HC14: 0x40010D0E | B0_P6_ROUTE_HC15: 0x40010D0F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

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|------------------------------|------------------------------|
| B0_P6_ROUTE_HC16: 0x40010D10 | B0_P6_ROUTE_HC17: 0x40010D11 |
| B0_P6_ROUTE_HC18: 0x40010D12 | B0_P6_ROUTE_HC19: 0x40010D13 |
| B0_P6_ROUTE_HC20: 0x40010D14 | B0_P6_ROUTE_HC21: 0x40010D15 |
| B0_P6_ROUTE_HC22: 0x40010D16 | B0_P6_ROUTE_HC23: 0x40010D17 |
| B0_P6_ROUTE_HC24: 0x40010D18 | B0_P6_ROUTE_HC25: 0x40010D19 |
| B0_P6_ROUTE_HC26: 0x40010D1A | B0_P6_ROUTE_HC27: 0x40010D1B |
| B0_P6_ROUTE_HC28: 0x40010D1C | B0_P6_ROUTE_HC29: 0x40010D1D |
| B0_P6_ROUTE_HC30: 0x40010D1E | B0_P6_ROUTE_HC31: 0x40010D1F |
| B0_P6_ROUTE_HC32: 0x40010D20 | B0_P6_ROUTE_HC33: 0x40010D21 |
| B0_P6_ROUTE_HC34: 0x40010D22 | B0_P6_ROUTE_HC35: 0x40010D23 |
| B0_P6_ROUTE_HC36: 0x40010D24 | B0_P6_ROUTE_HC37: 0x40010D25 |
| B0_P6_ROUTE_HC38: 0x40010D26 | B0_P6_ROUTE_HC39: 0x40010D27 |
| B0_P6_ROUTE_HC40: 0x40010D28 | B0_P6_ROUTE_HC41: 0x40010D29 |
| B0_P6_ROUTE_HC42: 0x40010D2A | B0_P6_ROUTE_HC43: 0x40010D2B |
| B0_P6_ROUTE_HC44: 0x40010D2C | B0_P6_ROUTE_HC45: 0x40010D2D |
| B0_P6_ROUTE_HC46: 0x40010D2E | B0_P6_ROUTE_HC47: 0x40010D2F |
| B0_P6_ROUTE_HC48: 0x40010D30 | B0_P6_ROUTE_HC49: 0x40010D31 |
| B0_P6_ROUTE_HC50: 0x40010D32 | B0_P6_ROUTE_HC51: 0x40010D33 |
| B0_P6_ROUTE_HC52: 0x40010D34 | B0_P6_ROUTE_HC53: 0x40010D35 |
| B0_P6_ROUTE_HC54: 0x40010D36 | B0_P6_ROUTE_HC55: 0x40010D37 |
| B0_P6_ROUTE_HC56: 0x40010D38 | B0_P6_ROUTE_HC57: 0x40010D39 |
| B0_P6_ROUTE_HC58: 0x40010D3A | B0_P6_ROUTE_HC59: 0x40010D3B |
| B0_P6_ROUTE_HC60: 0x40010D3C | B0_P6_ROUTE_HC61: 0x40010D3D |
| B0_P6_ROUTE_HC62: 0x40010D3E | B0_P6_ROUTE_HC63: 0x40010D3F |
| B0_P6_ROUTE_HC64: 0x40010D40 | B0_P6_ROUTE_HC65: 0x40010D41 |
| B0_P6_ROUTE_HC66: 0x40010D42 | B0_P6_ROUTE_HC67: 0x40010D43 |
| B0_P6_ROUTE_HC68: 0x40010D44 | B0_P6_ROUTE_HC69: 0x40010D45 |
| B0_P6_ROUTE_HC70: 0x40010D46 | B0_P6_ROUTE_HC71: 0x40010D47 |
| B0_P6_ROUTE_HC72: 0x40010D48 | B0_P6_ROUTE_HC73: 0x40010D49 |
| B0_P6_ROUTE_HC74: 0x40010D4A | B0_P6_ROUTE_HC75: 0x40010D4B |
| B0_P6_ROUTE_HC76: 0x40010D4C | B0_P6_ROUTE_HC77: 0x40010D4D |
| B0_P6_ROUTE_HC78: 0x40010D4E | B0_P6_ROUTE_HC79: 0x40010D4F |
| B0_P6_ROUTE_HC80: 0x40010D50 | B0_P6_ROUTE_HC81: 0x40010D51 |
| B0_P6_ROUTE_HC82: 0x40010D52 | B0_P6_ROUTE_HC83: 0x40010D53 |
| B0_P6_ROUTE_HC84: 0x40010D54 | B0_P6_ROUTE_HC85: 0x40010D55 |
| B0_P6_ROUTE_HC86: 0x40010D56 | B0_P6_ROUTE_HC87: 0x40010D57 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B0_P6_ROUTE_HC88: 0x40010D58 | B0_P6_ROUTE_HC89: 0x40010D59 |
| B0_P6_ROUTE_HC90: 0x40010D5A | B0_P6_ROUTE_HC91: 0x40010D5B |
| B0_P6_ROUTE_HC92: 0x40010D5C | B0_P6_ROUTE_HC93: 0x40010D5D |
| B0_P6_ROUTE_HC94: 0x40010D5E | B0_P6_ROUTE_HC95: 0x40010D5F |
| B0_P6_ROUTE_HC96: 0x40010D60 | B0_P6_ROUTE_HC97: 0x40010D61 |
| B0_P6_ROUTE_HC98: 0x40010D62 | B0_P6_ROUTE_HC99: 0x40010D63 |
| B0_P6_ROUTE_HC100: 0x40010D64 | B0_P6_ROUTE_HC101: 0x40010D65 |
| B0_P6_ROUTE_HC102: 0x40010D66 | B0_P6_ROUTE_HC103: 0x40010D67 |
| B0_P6_ROUTE_HC104: 0x40010D68 | B0_P6_ROUTE_HC105: 0x40010D69 |
| B0_P6_ROUTE_HC106: 0x40010D6A | B0_P6_ROUTE_HC107: 0x40010D6B |
| B0_P6_ROUTE_HC108: 0x40010D6C | B0_P6_ROUTE_HC109: 0x40010D6D |
| B0_P6_ROUTE_HC110: 0x40010D6E | B0_P6_ROUTE_HC111: 0x40010D6F |
| B0_P6_ROUTE_HC112: 0x40010D70 | B0_P6_ROUTE_HC113: 0x40010D71 |
| B0_P6_ROUTE_HC114: 0x40010D72 | B0_P6_ROUTE_HC115: 0x40010D73 |
| B0_P6_ROUTE_HC116: 0x40010D74 | B0_P6_ROUTE_HC117: 0x40010D75 |
| B0_P6_ROUTE_HC118: 0x40010D76 | B0_P6_ROUTE_HC119: 0x40010D77 |
| B0_P6_ROUTE_HC120: 0x40010D78 | B0_P6_ROUTE_HC121: 0x40010D79 |
| B0_P6_ROUTE_HC122: 0x40010D7A | B0_P6_ROUTE_HC123: 0x40010D7B |
| B0_P6_ROUTE_HC124: 0x40010D7C | B0_P6_ROUTE_HC125: 0x40010D7D |
| B0_P6_ROUTE_HC126: 0x40010D7E | B0_P6_ROUTE_HC127: 0x40010D7F |
| B0_P7_ROUTE_HC0: 0x40010F00 | B0_P7_ROUTE_HC1: 0x40010F01 |
| B0_P7_ROUTE_HC2: 0x40010F02 | B0_P7_ROUTE_HC3: 0x40010F03 |
| B0_P7_ROUTE_HC4: 0x40010F04 | B0_P7_ROUTE_HC5: 0x40010F05 |
| B0_P7_ROUTE_HC6: 0x40010F06 | B0_P7_ROUTE_HC7: 0x40010F07 |
| B0_P7_ROUTE_HC8: 0x40010F08 | B0_P7_ROUTE_HC9: 0x40010F09 |
| B0_P7_ROUTE_HC10: 0x40010F0A | B0_P7_ROUTE_HC11: 0x40010F0B |
| B0_P7_ROUTE_HC12: 0x40010F0C | B0_P7_ROUTE_HC13: 0x40010F0D |
| B0_P7_ROUTE_HC14: 0x40010F0E | B0_P7_ROUTE_HC15: 0x40010F0F |
| B0_P7_ROUTE_HC16: 0x40010F10 | B0_P7_ROUTE_HC17: 0x40010F11 |
| B0_P7_ROUTE_HC18: 0x40010F12 | B0_P7_ROUTE_HC19: 0x40010F13 |
| B0_P7_ROUTE_HC20: 0x40010F14 | B0_P7_ROUTE_HC21: 0x40010F15 |
| B0_P7_ROUTE_HC22: 0x40010F16 | B0_P7_ROUTE_HC23: 0x40010F17 |
| B0_P7_ROUTE_HC24: 0x40010F18 | B0_P7_ROUTE_HC25: 0x40010F19 |
| B0_P7_ROUTE_HC26: 0x40010F1A | B0_P7_ROUTE_HC27: 0x40010F1B |
| B0_P7_ROUTE_HC28: 0x40010F1C | B0_P7_ROUTE_HC29: 0x40010F1D |
| B0_P7_ROUTE_HC30: 0x40010F1E | B0_P7_ROUTE_HC31: 0x40010F1F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B0_P7_ROUTE_HC32: 0x40010F20 | B0_P7_ROUTE_HC33: 0x40010F21 |
| B0_P7_ROUTE_HC34: 0x40010F22 | B0_P7_ROUTE_HC35: 0x40010F23 |
| B0_P7_ROUTE_HC36: 0x40010F24 | B0_P7_ROUTE_HC37: 0x40010F25 |
| B0_P7_ROUTE_HC38: 0x40010F26 | B0_P7_ROUTE_HC39: 0x40010F27 |
| B0_P7_ROUTE_HC40: 0x40010F28 | B0_P7_ROUTE_HC41: 0x40010F29 |
| B0_P7_ROUTE_HC42: 0x40010F2A | B0_P7_ROUTE_HC43: 0x40010F2B |
| B0_P7_ROUTE_HC44: 0x40010F2C | B0_P7_ROUTE_HC45: 0x40010F2D |
| B0_P7_ROUTE_HC46: 0x40010F2E | B0_P7_ROUTE_HC47: 0x40010F2F |
| B0_P7_ROUTE_HC48: 0x40010F30 | B0_P7_ROUTE_HC49: 0x40010F31 |
| B0_P7_ROUTE_HC50: 0x40010F32 | B0_P7_ROUTE_HC51: 0x40010F33 |
| B0_P7_ROUTE_HC52: 0x40010F34 | B0_P7_ROUTE_HC53: 0x40010F35 |
| B0_P7_ROUTE_HC54: 0x40010F36 | B0_P7_ROUTE_HC55: 0x40010F37 |
| B0_P7_ROUTE_HC56: 0x40010F38 | B0_P7_ROUTE_HC57: 0x40010F39 |
| B0_P7_ROUTE_HC58: 0x40010F3A | B0_P7_ROUTE_HC59: 0x40010F3B |
| B0_P7_ROUTE_HC60: 0x40010F3C | B0_P7_ROUTE_HC61: 0x40010F3D |
| B0_P7_ROUTE_HC62: 0x40010F3E | B0_P7_ROUTE_HC63: 0x40010F3F |
| B0_P7_ROUTE_HC64: 0x40010F40 | B0_P7_ROUTE_HC65: 0x40010F41 |
| B0_P7_ROUTE_HC66: 0x40010F42 | B0_P7_ROUTE_HC67: 0x40010F43 |
| B0_P7_ROUTE_HC68: 0x40010F44 | B0_P7_ROUTE_HC69: 0x40010F45 |
| B0_P7_ROUTE_HC70: 0x40010F46 | B0_P7_ROUTE_HC71: 0x40010F47 |
| B0_P7_ROUTE_HC72: 0x40010F48 | B0_P7_ROUTE_HC73: 0x40010F49 |
| B0_P7_ROUTE_HC74: 0x40010F4A | B0_P7_ROUTE_HC75: 0x40010F4B |
| B0_P7_ROUTE_HC76: 0x40010F4C | B0_P7_ROUTE_HC77: 0x40010F4D |
| B0_P7_ROUTE_HC78: 0x40010F4E | B0_P7_ROUTE_HC79: 0x40010F4F |
| B0_P7_ROUTE_HC80: 0x40010F50 | B0_P7_ROUTE_HC81: 0x40010F51 |
| B0_P7_ROUTE_HC82: 0x40010F52 | B0_P7_ROUTE_HC83: 0x40010F53 |
| B0_P7_ROUTE_HC84: 0x40010F54 | B0_P7_ROUTE_HC85: 0x40010F55 |
| B0_P7_ROUTE_HC86: 0x40010F56 | B0_P7_ROUTE_HC87: 0x40010F57 |
| B0_P7_ROUTE_HC88: 0x40010F58 | B0_P7_ROUTE_HC89: 0x40010F59 |
| B0_P7_ROUTE_HC90: 0x40010F5A | B0_P7_ROUTE_HC91: 0x40010F5B |
| B0_P7_ROUTE_HC92: 0x40010F5C | B0_P7_ROUTE_HC93: 0x40010F5D |
| B0_P7_ROUTE_HC94: 0x40010F5E | B0_P7_ROUTE_HC95: 0x40010F5F |
| B0_P7_ROUTE_HC96: 0x40010F60 | B0_P7_ROUTE_HC97: 0x40010F61 |
| B0_P7_ROUTE_HC98: 0x40010F62 | B0_P7_ROUTE_HC99: 0x40010F63 |
| B0_P7_ROUTE_HC100: 0x40010F64 | B0_P7_ROUTE_HC101: 0x40010F65 |
| B0_P7_ROUTE_HC102: 0x40010F66 | B0_P7_ROUTE_HC103: 0x40010F67 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B0_P7_ROUTE_HC104: 0x40010F68 | B0_P7_ROUTE_HC105: 0x40010F69 |
| B0_P7_ROUTE_HC106: 0x40010F6A | B0_P7_ROUTE_HC107: 0x40010F6B |
| B0_P7_ROUTE_HC108: 0x40010F6C | B0_P7_ROUTE_HC109: 0x40010F6D |
| B0_P7_ROUTE_HC110: 0x40010F6E | B0_P7_ROUTE_HC111: 0x40010F6F |
| B0_P7_ROUTE_HC112: 0x40010F70 | B0_P7_ROUTE_HC113: 0x40010F71 |
| B0_P7_ROUTE_HC114: 0x40010F72 | B0_P7_ROUTE_HC115: 0x40010F73 |
| B0_P7_ROUTE_HC116: 0x40010F74 | B0_P7_ROUTE_HC117: 0x40010F75 |
| B0_P7_ROUTE_HC118: 0x40010F76 | B0_P7_ROUTE_HC119: 0x40010F77 |
| B0_P7_ROUTE_HC120: 0x40010F78 | B0_P7_ROUTE_HC121: 0x40010F79 |
| B0_P7_ROUTE_HC122: 0x40010F7A | B0_P7_ROUTE_HC123: 0x40010F7B |
| B0_P7_ROUTE_HC124: 0x40010F7C | B0_P7_ROUTE_HC125: 0x40010F7D |
| B0_P7_ROUTE_HC126: 0x40010F7E | B0_P7_ROUTE_HC127: 0x40010F7F |
| B1_P2_ROUTE_HC0: 0x40011500 | B1_P2_ROUTE_HC1: 0x40011501 |
| B1_P2_ROUTE_HC2: 0x40011502 | B1_P2_ROUTE_HC3: 0x40011503 |
| B1_P2_ROUTE_HC4: 0x40011504 | B1_P2_ROUTE_HC5: 0x40011505 |
| B1_P2_ROUTE_HC6: 0x40011506 | B1_P2_ROUTE_HC7: 0x40011507 |
| B1_P2_ROUTE_HC8: 0x40011508 | B1_P2_ROUTE_HC9: 0x40011509 |
| B1_P2_ROUTE_HC10: 0x4001150A | B1_P2_ROUTE_HC11: 0x4001150B |
| B1_P2_ROUTE_HC12: 0x4001150C | B1_P2_ROUTE_HC13: 0x4001150D |
| B1_P2_ROUTE_HC14: 0x4001150E | B1_P2_ROUTE_HC15: 0x4001150F |
| B1_P2_ROUTE_HC16: 0x40011510 | B1_P2_ROUTE_HC17: 0x40011511 |
| B1_P2_ROUTE_HC18: 0x40011512 | B1_P2_ROUTE_HC19: 0x40011513 |
| B1_P2_ROUTE_HC20: 0x40011514 | B1_P2_ROUTE_HC21: 0x40011515 |
| B1_P2_ROUTE_HC22: 0x40011516 | B1_P2_ROUTE_HC23: 0x40011517 |
| B1_P2_ROUTE_HC24: 0x40011518 | B1_P2_ROUTE_HC25: 0x40011519 |
| B1_P2_ROUTE_HC26: 0x4001151A | B1_P2_ROUTE_HC27: 0x4001151B |
| B1_P2_ROUTE_HC28: 0x4001151C | B1_P2_ROUTE_HC29: 0x4001151D |
| B1_P2_ROUTE_HC30: 0x4001151E | B1_P2_ROUTE_HC31: 0x4001151F |
| B1_P2_ROUTE_HC32: 0x40011520 | B1_P2_ROUTE_HC33: 0x40011521 |
| B1_P2_ROUTE_HC34: 0x40011522 | B1_P2_ROUTE_HC35: 0x40011523 |
| B1_P2_ROUTE_HC36: 0x40011524 | B1_P2_ROUTE_HC37: 0x40011525 |
| B1_P2_ROUTE_HC38: 0x40011526 | B1_P2_ROUTE_HC39: 0x40011527 |
| B1_P2_ROUTE_HC40: 0x40011528 | B1_P2_ROUTE_HC41: 0x40011529 |
| B1_P2_ROUTE_HC42: 0x4001152A | B1_P2_ROUTE_HC43: 0x4001152B |
| B1_P2_ROUTE_HC44: 0x4001152C | B1_P2_ROUTE_HC45: 0x4001152D |
| B1_P2_ROUTE_HC46: 0x4001152E | B1_P2_ROUTE_HC47: 0x4001152F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B1_P2_ROUTE_HC48: 0x40011530 | B1_P2_ROUTE_HC49: 0x40011531 |
| B1_P2_ROUTE_HC50: 0x40011532 | B1_P2_ROUTE_HC51: 0x40011533 |
| B1_P2_ROUTE_HC52: 0x40011534 | B1_P2_ROUTE_HC53: 0x40011535 |
| B1_P2_ROUTE_HC54: 0x40011536 | B1_P2_ROUTE_HC55: 0x40011537 |
| B1_P2_ROUTE_HC56: 0x40011538 | B1_P2_ROUTE_HC57: 0x40011539 |
| B1_P2_ROUTE_HC58: 0x4001153A | B1_P2_ROUTE_HC59: 0x4001153B |
| B1_P2_ROUTE_HC60: 0x4001153C | B1_P2_ROUTE_HC61: 0x4001153D |
| B1_P2_ROUTE_HC62: 0x4001153E | B1_P2_ROUTE_HC63: 0x4001153F |
| B1_P2_ROUTE_HC64: 0x40011540 | B1_P2_ROUTE_HC65: 0x40011541 |
| B1_P2_ROUTE_HC66: 0x40011542 | B1_P2_ROUTE_HC67: 0x40011543 |
| B1_P2_ROUTE_HC68: 0x40011544 | B1_P2_ROUTE_HC69: 0x40011545 |
| B1_P2_ROUTE_HC70: 0x40011546 | B1_P2_ROUTE_HC71: 0x40011547 |
| B1_P2_ROUTE_HC72: 0x40011548 | B1_P2_ROUTE_HC73: 0x40011549 |
| B1_P2_ROUTE_HC74: 0x4001154A | B1_P2_ROUTE_HC75: 0x4001154B |
| B1_P2_ROUTE_HC76: 0x4001154C | B1_P2_ROUTE_HC77: 0x4001154D |
| B1_P2_ROUTE_HC78: 0x4001154E | B1_P2_ROUTE_HC79: 0x4001154F |
| B1_P2_ROUTE_HC80: 0x40011550 | B1_P2_ROUTE_HC81: 0x40011551 |
| B1_P2_ROUTE_HC82: 0x40011552 | B1_P2_ROUTE_HC83: 0x40011553 |
| B1_P2_ROUTE_HC84: 0x40011554 | B1_P2_ROUTE_HC85: 0x40011555 |
| B1_P2_ROUTE_HC86: 0x40011556 | B1_P2_ROUTE_HC87: 0x40011557 |
| B1_P2_ROUTE_HC88: 0x40011558 | B1_P2_ROUTE_HC89: 0x40011559 |
| B1_P2_ROUTE_HC90: 0x4001155A | B1_P2_ROUTE_HC91: 0x4001155B |
| B1_P2_ROUTE_HC92: 0x4001155C | B1_P2_ROUTE_HC93: 0x4001155D |
| B1_P2_ROUTE_HC94: 0x4001155E | B1_P2_ROUTE_HC95: 0x4001155F |
| B1_P2_ROUTE_HC96: 0x40011560 | B1_P2_ROUTE_HC97: 0x40011561 |
| B1_P2_ROUTE_HC98: 0x40011562 | B1_P2_ROUTE_HC99: 0x40011563 |
| B1_P2_ROUTE_HC100: 0x40011564 | B1_P2_ROUTE_HC101: 0x40011565 |
| B1_P2_ROUTE_HC102: 0x40011566 | B1_P2_ROUTE_HC103: 0x40011567 |
| B1_P2_ROUTE_HC104: 0x40011568 | B1_P2_ROUTE_HC105: 0x40011569 |
| B1_P2_ROUTE_HC106: 0x4001156A | B1_P2_ROUTE_HC107: 0x4001156B |
| B1_P2_ROUTE_HC108: 0x4001156C | B1_P2_ROUTE_HC109: 0x4001156D |
| B1_P2_ROUTE_HC110: 0x4001156E | B1_P2_ROUTE_HC111: 0x4001156F |
| B1_P2_ROUTE_HC112: 0x40011570 | B1_P2_ROUTE_HC113: 0x40011571 |
| B1_P2_ROUTE_HC114: 0x40011572 | B1_P2_ROUTE_HC115: 0x40011573 |
| B1_P2_ROUTE_HC116: 0x40011574 | B1_P2_ROUTE_HC117: 0x40011575 |
| B1_P2_ROUTE_HC118: 0x40011576 | B1_P2_ROUTE_HC119: 0x40011577 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B1_P2_ROUTE_HC120: 0x40011578 | B1_P2_ROUTE_HC121: 0x40011579 |
| B1_P2_ROUTE_HC122: 0x4001157A | B1_P2_ROUTE_HC123: 0x4001157B |
| B1_P2_ROUTE_HC124: 0x4001157C | B1_P2_ROUTE_HC125: 0x4001157D |
| B1_P2_ROUTE_HC126: 0x4001157E | B1_P2_ROUTE_HC127: 0x4001157F |
| B1_P3_ROUTE_HC0: 0x40011700 | B1_P3_ROUTE_HC1: 0x40011701 |
| B1_P3_ROUTE_HC2: 0x40011702 | B1_P3_ROUTE_HC3: 0x40011703 |
| B1_P3_ROUTE_HC4: 0x40011704 | B1_P3_ROUTE_HC5: 0x40011705 |
| B1_P3_ROUTE_HC6: 0x40011706 | B1_P3_ROUTE_HC7: 0x40011707 |
| B1_P3_ROUTE_HC8: 0x40011708 | B1_P3_ROUTE_HC9: 0x40011709 |
| B1_P3_ROUTE_HC10: 0x4001170A | B1_P3_ROUTE_HC11: 0x4001170B |
| B1_P3_ROUTE_HC12: 0x4001170C | B1_P3_ROUTE_HC13: 0x4001170D |
| B1_P3_ROUTE_HC14: 0x4001170E | B1_P3_ROUTE_HC15: 0x4001170F |
| B1_P3_ROUTE_HC16: 0x40011710 | B1_P3_ROUTE_HC17: 0x40011711 |
| B1_P3_ROUTE_HC18: 0x40011712 | B1_P3_ROUTE_HC19: 0x40011713 |
| B1_P3_ROUTE_HC20: 0x40011714 | B1_P3_ROUTE_HC21: 0x40011715 |
| B1_P3_ROUTE_HC22: 0x40011716 | B1_P3_ROUTE_HC23: 0x40011717 |
| B1_P3_ROUTE_HC24: 0x40011718 | B1_P3_ROUTE_HC25: 0x40011719 |
| B1_P3_ROUTE_HC26: 0x4001171A | B1_P3_ROUTE_HC27: 0x4001171B |
| B1_P3_ROUTE_HC28: 0x4001171C | B1_P3_ROUTE_HC29: 0x4001171D |
| B1_P3_ROUTE_HC30: 0x4001171E | B1_P3_ROUTE_HC31: 0x4001171F |
| B1_P3_ROUTE_HC32: 0x40011720 | B1_P3_ROUTE_HC33: 0x40011721 |
| B1_P3_ROUTE_HC34: 0x40011722 | B1_P3_ROUTE_HC35: 0x40011723 |
| B1_P3_ROUTE_HC36: 0x40011724 | B1_P3_ROUTE_HC37: 0x40011725 |
| B1_P3_ROUTE_HC38: 0x40011726 | B1_P3_ROUTE_HC39: 0x40011727 |
| B1_P3_ROUTE_HC40: 0x40011728 | B1_P3_ROUTE_HC41: 0x40011729 |
| B1_P3_ROUTE_HC42: 0x4001172A | B1_P3_ROUTE_HC43: 0x4001172B |
| B1_P3_ROUTE_HC44: 0x4001172C | B1_P3_ROUTE_HC45: 0x4001172D |
| B1_P3_ROUTE_HC46: 0x4001172E | B1_P3_ROUTE_HC47: 0x4001172F |
| B1_P3_ROUTE_HC48: 0x40011730 | B1_P3_ROUTE_HC49: 0x40011731 |
| B1_P3_ROUTE_HC50: 0x40011732 | B1_P3_ROUTE_HC51: 0x40011733 |
| B1_P3_ROUTE_HC52: 0x40011734 | B1_P3_ROUTE_HC53: 0x40011735 |
| B1_P3_ROUTE_HC54: 0x40011736 | B1_P3_ROUTE_HC55: 0x40011737 |
| B1_P3_ROUTE_HC56: 0x40011738 | B1_P3_ROUTE_HC57: 0x40011739 |
| B1_P3_ROUTE_HC58: 0x4001173A | B1_P3_ROUTE_HC59: 0x4001173B |
| B1_P3_ROUTE_HC60: 0x4001173C | B1_P3_ROUTE_HC61: 0x4001173D |
| B1_P3_ROUTE_HC62: 0x4001173E | B1_P3_ROUTE_HC63: 0x4001173F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B1_P3_ROUTE_HC64: 0x40011740 | B1_P3_ROUTE_HC65: 0x40011741 |
| B1_P3_ROUTE_HC66: 0x40011742 | B1_P3_ROUTE_HC67: 0x40011743 |
| B1_P3_ROUTE_HC68: 0x40011744 | B1_P3_ROUTE_HC69: 0x40011745 |
| B1_P3_ROUTE_HC70: 0x40011746 | B1_P3_ROUTE_HC71: 0x40011747 |
| B1_P3_ROUTE_HC72: 0x40011748 | B1_P3_ROUTE_HC73: 0x40011749 |
| B1_P3_ROUTE_HC74: 0x4001174A | B1_P3_ROUTE_HC75: 0x4001174B |
| B1_P3_ROUTE_HC76: 0x4001174C | B1_P3_ROUTE_HC77: 0x4001174D |
| B1_P3_ROUTE_HC78: 0x4001174E | B1_P3_ROUTE_HC79: 0x4001174F |
| B1_P3_ROUTE_HC80: 0x40011750 | B1_P3_ROUTE_HC81: 0x40011751 |
| B1_P3_ROUTE_HC82: 0x40011752 | B1_P3_ROUTE_HC83: 0x40011753 |
| B1_P3_ROUTE_HC84: 0x40011754 | B1_P3_ROUTE_HC85: 0x40011755 |
| B1_P3_ROUTE_HC86: 0x40011756 | B1_P3_ROUTE_HC87: 0x40011757 |
| B1_P3_ROUTE_HC88: 0x40011758 | B1_P3_ROUTE_HC89: 0x40011759 |
| B1_P3_ROUTE_HC90: 0x4001175A | B1_P3_ROUTE_HC91: 0x4001175B |
| B1_P3_ROUTE_HC92: 0x4001175C | B1_P3_ROUTE_HC93: 0x4001175D |
| B1_P3_ROUTE_HC94: 0x4001175E | B1_P3_ROUTE_HC95: 0x4001175F |
| B1_P3_ROUTE_HC96: 0x40011760 | B1_P3_ROUTE_HC97: 0x40011761 |
| B1_P3_ROUTE_HC98: 0x40011762 | B1_P3_ROUTE_HC99: 0x40011763 |
| B1_P3_ROUTE_HC100: 0x40011764 | B1_P3_ROUTE_HC101: 0x40011765 |
| B1_P3_ROUTE_HC102: 0x40011766 | B1_P3_ROUTE_HC103: 0x40011767 |
| B1_P3_ROUTE_HC104: 0x40011768 | B1_P3_ROUTE_HC105: 0x40011769 |
| B1_P3_ROUTE_HC106: 0x4001176A | B1_P3_ROUTE_HC107: 0x4001176B |
| B1_P3_ROUTE_HC108: 0x4001176C | B1_P3_ROUTE_HC109: 0x4001176D |
| B1_P3_ROUTE_HC110: 0x4001176E | B1_P3_ROUTE_HC111: 0x4001176F |
| B1_P3_ROUTE_HC112: 0x40011770 | B1_P3_ROUTE_HC113: 0x40011771 |
| B1_P3_ROUTE_HC114: 0x40011772 | B1_P3_ROUTE_HC115: 0x40011773 |
| B1_P3_ROUTE_HC116: 0x40011774 | B1_P3_ROUTE_HC117: 0x40011775 |
| B1_P3_ROUTE_HC118: 0x40011776 | B1_P3_ROUTE_HC119: 0x40011777 |
| B1_P3_ROUTE_HC120: 0x40011778 | B1_P3_ROUTE_HC121: 0x40011779 |
| B1_P3_ROUTE_HC122: 0x4001177A | B1_P3_ROUTE_HC123: 0x4001177B |
| B1_P3_ROUTE_HC124: 0x4001177C | B1_P3_ROUTE_HC125: 0x4001177D |
| B1_P3_ROUTE_HC126: 0x4001177E | B1_P3_ROUTE_HC127: 0x4001177F |
| B1_P4_ROUTE_HC0: 0x40011900 | B1_P4_ROUTE_HC1: 0x40011901 |
| B1_P4_ROUTE_HC2: 0x40011902 | B1_P4_ROUTE_HC3: 0x40011903 |
| B1_P4_ROUTE_HC4: 0x40011904 | B1_P4_ROUTE_HC5: 0x40011905 |
| B1_P4_ROUTE_HC6: 0x40011906 | B1_P4_ROUTE_HC7: 0x40011907 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|------------------------------|------------------------------|
| B1_P4_ROUTE_HC8: 0x40011908 | B1_P4_ROUTE_HC9: 0x40011909 |
| B1_P4_ROUTE_HC10: 0x4001190A | B1_P4_ROUTE_HC11: 0x4001190B |
| B1_P4_ROUTE_HC12: 0x4001190C | B1_P4_ROUTE_HC13: 0x4001190D |
| B1_P4_ROUTE_HC14: 0x4001190E | B1_P4_ROUTE_HC15: 0x4001190F |
| B1_P4_ROUTE_HC16: 0x40011910 | B1_P4_ROUTE_HC17: 0x40011911 |
| B1_P4_ROUTE_HC18: 0x40011912 | B1_P4_ROUTE_HC19: 0x40011913 |
| B1_P4_ROUTE_HC20: 0x40011914 | B1_P4_ROUTE_HC21: 0x40011915 |
| B1_P4_ROUTE_HC22: 0x40011916 | B1_P4_ROUTE_HC23: 0x40011917 |
| B1_P4_ROUTE_HC24: 0x40011918 | B1_P4_ROUTE_HC25: 0x40011919 |
| B1_P4_ROUTE_HC26: 0x4001191A | B1_P4_ROUTE_HC27: 0x4001191B |
| B1_P4_ROUTE_HC28: 0x4001191C | B1_P4_ROUTE_HC29: 0x4001191D |
| B1_P4_ROUTE_HC30: 0x4001191E | B1_P4_ROUTE_HC31: 0x4001191F |
| B1_P4_ROUTE_HC32: 0x40011920 | B1_P4_ROUTE_HC33: 0x40011921 |
| B1_P4_ROUTE_HC34: 0x40011922 | B1_P4_ROUTE_HC35: 0x40011923 |
| B1_P4_ROUTE_HC36: 0x40011924 | B1_P4_ROUTE_HC37: 0x40011925 |
| B1_P4_ROUTE_HC38: 0x40011926 | B1_P4_ROUTE_HC39: 0x40011927 |
| B1_P4_ROUTE_HC40: 0x40011928 | B1_P4_ROUTE_HC41: 0x40011929 |
| B1_P4_ROUTE_HC42: 0x4001192A | B1_P4_ROUTE_HC43: 0x4001192B |
| B1_P4_ROUTE_HC44: 0x4001192C | B1_P4_ROUTE_HC45: 0x4001192D |
| B1_P4_ROUTE_HC46: 0x4001192E | B1_P4_ROUTE_HC47: 0x4001192F |
| B1_P4_ROUTE_HC48: 0x40011930 | B1_P4_ROUTE_HC49: 0x40011931 |
| B1_P4_ROUTE_HC50: 0x40011932 | B1_P4_ROUTE_HC51: 0x40011933 |
| B1_P4_ROUTE_HC52: 0x40011934 | B1_P4_ROUTE_HC53: 0x40011935 |
| B1_P4_ROUTE_HC54: 0x40011936 | B1_P4_ROUTE_HC55: 0x40011937 |
| B1_P4_ROUTE_HC56: 0x40011938 | B1_P4_ROUTE_HC57: 0x40011939 |
| B1_P4_ROUTE_HC58: 0x4001193A | B1_P4_ROUTE_HC59: 0x4001193B |
| B1_P4_ROUTE_HC60: 0x4001193C | B1_P4_ROUTE_HC61: 0x4001193D |
| B1_P4_ROUTE_HC62: 0x4001193E | B1_P4_ROUTE_HC63: 0x4001193F |
| B1_P4_ROUTE_HC64: 0x40011940 | B1_P4_ROUTE_HC65: 0x40011941 |
| B1_P4_ROUTE_HC66: 0x40011942 | B1_P4_ROUTE_HC67: 0x40011943 |
| B1_P4_ROUTE_HC68: 0x40011944 | B1_P4_ROUTE_HC69: 0x40011945 |
| B1_P4_ROUTE_HC70: 0x40011946 | B1_P4_ROUTE_HC71: 0x40011947 |
| B1_P4_ROUTE_HC72: 0x40011948 | B1_P4_ROUTE_HC73: 0x40011949 |
| B1_P4_ROUTE_HC74: 0x4001194A | B1_P4_ROUTE_HC75: 0x4001194B |
| B1_P4_ROUTE_HC76: 0x4001194C | B1_P4_ROUTE_HC77: 0x4001194D |
| B1_P4_ROUTE_HC78: 0x4001194E | B1_P4_ROUTE_HC79: 0x4001194F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B1_P4_ROUTE_HC80: 0x40011950 | B1_P4_ROUTE_HC81: 0x40011951 |
| B1_P4_ROUTE_HC82: 0x40011952 | B1_P4_ROUTE_HC83: 0x40011953 |
| B1_P4_ROUTE_HC84: 0x40011954 | B1_P4_ROUTE_HC85: 0x40011955 |
| B1_P4_ROUTE_HC86: 0x40011956 | B1_P4_ROUTE_HC87: 0x40011957 |
| B1_P4_ROUTE_HC88: 0x40011958 | B1_P4_ROUTE_HC89: 0x40011959 |
| B1_P4_ROUTE_HC90: 0x4001195A | B1_P4_ROUTE_HC91: 0x4001195B |
| B1_P4_ROUTE_HC92: 0x4001195C | B1_P4_ROUTE_HC93: 0x4001195D |
| B1_P4_ROUTE_HC94: 0x4001195E | B1_P4_ROUTE_HC95: 0x4001195F |
| B1_P4_ROUTE_HC96: 0x40011960 | B1_P4_ROUTE_HC97: 0x40011961 |
| B1_P4_ROUTE_HC98: 0x40011962 | B1_P4_ROUTE_HC99: 0x40011963 |
| B1_P4_ROUTE_HC100: 0x40011964 | B1_P4_ROUTE_HC101: 0x40011965 |
| B1_P4_ROUTE_HC102: 0x40011966 | B1_P4_ROUTE_HC103: 0x40011967 |
| B1_P4_ROUTE_HC104: 0x40011968 | B1_P4_ROUTE_HC105: 0x40011969 |
| B1_P4_ROUTE_HC106: 0x4001196A | B1_P4_ROUTE_HC107: 0x4001196B |
| B1_P4_ROUTE_HC108: 0x4001196C | B1_P4_ROUTE_HC109: 0x4001196D |
| B1_P4_ROUTE_HC110: 0x4001196E | B1_P4_ROUTE_HC111: 0x4001196F |
| B1_P4_ROUTE_HC112: 0x40011970 | B1_P4_ROUTE_HC113: 0x40011971 |
| B1_P4_ROUTE_HC114: 0x40011972 | B1_P4_ROUTE_HC115: 0x40011973 |
| B1_P4_ROUTE_HC116: 0x40011974 | B1_P4_ROUTE_HC117: 0x40011975 |
| B1_P4_ROUTE_HC118: 0x40011976 | B1_P4_ROUTE_HC119: 0x40011977 |
| B1_P4_ROUTE_HC120: 0x40011978 | B1_P4_ROUTE_HC121: 0x40011979 |
| B1_P4_ROUTE_HC122: 0x4001197A | B1_P4_ROUTE_HC123: 0x4001197B |
| B1_P4_ROUTE_HC124: 0x4001197C | B1_P4_ROUTE_HC125: 0x4001197D |
| B1_P4_ROUTE_HC126: 0x4001197E | B1_P4_ROUTE_HC127: 0x4001197F |
| B1_P5_ROUTE_HC0: 0x40011B00 | B1_P5_ROUTE_HC1: 0x40011B01 |
| B1_P5_ROUTE_HC2: 0x40011B02 | B1_P5_ROUTE_HC3: 0x40011B03 |
| B1_P5_ROUTE_HC4: 0x40011B04 | B1_P5_ROUTE_HC5: 0x40011B05 |
| B1_P5_ROUTE_HC6: 0x40011B06 | B1_P5_ROUTE_HC7: 0x40011B07 |
| B1_P5_ROUTE_HC8: 0x40011B08 | B1_P5_ROUTE_HC9: 0x40011B09 |
| B1_P5_ROUTE_HC10: 0x40011B0A | B1_P5_ROUTE_HC11: 0x40011B0B |
| B1_P5_ROUTE_HC12: 0x40011B0C | B1_P5_ROUTE_HC13: 0x40011B0D |
| B1_P5_ROUTE_HC14: 0x40011B0E | B1_P5_ROUTE_HC15: 0x40011B0F |
| B1_P5_ROUTE_HC16: 0x40011B10 | B1_P5_ROUTE_HC17: 0x40011B11 |
| B1_P5_ROUTE_HC18: 0x40011B12 | B1_P5_ROUTE_HC19: 0x40011B13 |
| B1_P5_ROUTE_HC20: 0x40011B14 | B1_P5_ROUTE_HC21: 0x40011B15 |
| B1_P5_ROUTE_HC22: 0x40011B16 | B1_P5_ROUTE_HC23: 0x40011B17 |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|------------------------------|------------------------------|
| B1_P5_ROUTE_HC24: 0x40011B18 | B1_P5_ROUTE_HC25: 0x40011B19 |
| B1_P5_ROUTE_HC26: 0x40011B1A | B1_P5_ROUTE_HC27: 0x40011B1B |
| B1_P5_ROUTE_HC28: 0x40011B1C | B1_P5_ROUTE_HC29: 0x40011B1D |
| B1_P5_ROUTE_HC30: 0x40011B1E | B1_P5_ROUTE_HC31: 0x40011B1F |
| B1_P5_ROUTE_HC32: 0x40011B20 | B1_P5_ROUTE_HC33: 0x40011B21 |
| B1_P5_ROUTE_HC34: 0x40011B22 | B1_P5_ROUTE_HC35: 0x40011B23 |
| B1_P5_ROUTE_HC36: 0x40011B24 | B1_P5_ROUTE_HC37: 0x40011B25 |
| B1_P5_ROUTE_HC38: 0x40011B26 | B1_P5_ROUTE_HC39: 0x40011B27 |
| B1_P5_ROUTE_HC40: 0x40011B28 | B1_P5_ROUTE_HC41: 0x40011B29 |
| B1_P5_ROUTE_HC42: 0x40011B2A | B1_P5_ROUTE_HC43: 0x40011B2B |
| B1_P5_ROUTE_HC44: 0x40011B2C | B1_P5_ROUTE_HC45: 0x40011B2D |
| B1_P5_ROUTE_HC46: 0x40011B2E | B1_P5_ROUTE_HC47: 0x40011B2F |
| B1_P5_ROUTE_HC48: 0x40011B30 | B1_P5_ROUTE_HC49: 0x40011B31 |
| B1_P5_ROUTE_HC50: 0x40011B32 | B1_P5_ROUTE_HC51: 0x40011B33 |
| B1_P5_ROUTE_HC52: 0x40011B34 | B1_P5_ROUTE_HC53: 0x40011B35 |
| B1_P5_ROUTE_HC54: 0x40011B36 | B1_P5_ROUTE_HC55: 0x40011B37 |
| B1_P5_ROUTE_HC56: 0x40011B38 | B1_P5_ROUTE_HC57: 0x40011B39 |
| B1_P5_ROUTE_HC58: 0x40011B3A | B1_P5_ROUTE_HC59: 0x40011B3B |
| B1_P5_ROUTE_HC60: 0x40011B3C | B1_P5_ROUTE_HC61: 0x40011B3D |
| B1_P5_ROUTE_HC62: 0x40011B3E | B1_P5_ROUTE_HC63: 0x40011B3F |
| B1_P5_ROUTE_HC64: 0x40011B40 | B1_P5_ROUTE_HC65: 0x40011B41 |
| B1_P5_ROUTE_HC66: 0x40011B42 | B1_P5_ROUTE_HC67: 0x40011B43 |
| B1_P5_ROUTE_HC68: 0x40011B44 | B1_P5_ROUTE_HC69: 0x40011B45 |
| B1_P5_ROUTE_HC70: 0x40011B46 | B1_P5_ROUTE_HC71: 0x40011B47 |
| B1_P5_ROUTE_HC72: 0x40011B48 | B1_P5_ROUTE_HC73: 0x40011B49 |
| B1_P5_ROUTE_HC74: 0x40011B4A | B1_P5_ROUTE_HC75: 0x40011B4B |
| B1_P5_ROUTE_HC76: 0x40011B4C | B1_P5_ROUTE_HC77: 0x40011B4D |
| B1_P5_ROUTE_HC78: 0x40011B4E | B1_P5_ROUTE_HC79: 0x40011B4F |
| B1_P5_ROUTE_HC80: 0x40011B50 | B1_P5_ROUTE_HC81: 0x40011B51 |
| B1_P5_ROUTE_HC82: 0x40011B52 | B1_P5_ROUTE_HC83: 0x40011B53 |
| B1_P5_ROUTE_HC84: 0x40011B54 | B1_P5_ROUTE_HC85: 0x40011B55 |
| B1_P5_ROUTE_HC86: 0x40011B56 | B1_P5_ROUTE_HC87: 0x40011B57 |
| B1_P5_ROUTE_HC88: 0x40011B58 | B1_P5_ROUTE_HC89: 0x40011B59 |
| B1_P5_ROUTE_HC90: 0x40011B5A | B1_P5_ROUTE_HC91: 0x40011B5B |
| B1_P5_ROUTE_HC92: 0x40011B5C | B1_P5_ROUTE_HC93: 0x40011B5D |
| B1_P5_ROUTE_HC94: 0x40011B5E | B1_P5_ROUTE_HC95: 0x40011B5F |

1.3.1211 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

| | |
|-------------------------------|-------------------------------|
| B1_P5_ROUTE_HC96: 0x40011B60 | B1_P5_ROUTE_HC97: 0x40011B61 |
| B1_P5_ROUTE_HC98: 0x40011B62 | B1_P5_ROUTE_HC99: 0x40011B63 |
| B1_P5_ROUTE_HC100: 0x40011B64 | B1_P5_ROUTE_HC101: 0x40011B65 |
| B1_P5_ROUTE_HC102: 0x40011B66 | B1_P5_ROUTE_HC103: 0x40011B67 |
| B1_P5_ROUTE_HC104: 0x40011B68 | B1_P5_ROUTE_HC105: 0x40011B69 |
| B1_P5_ROUTE_HC106: 0x40011B6A | B1_P5_ROUTE_HC107: 0x40011B6B |
| B1_P5_ROUTE_HC108: 0x40011B6C | B1_P5_ROUTE_HC109: 0x40011B6D |
| B1_P5_ROUTE_HC110: 0x40011B6E | B1_P5_ROUTE_HC111: 0x40011B6F |
| B1_P5_ROUTE_HC112: 0x40011B70 | B1_P5_ROUTE_HC113: 0x40011B71 |
| B1_P5_ROUTE_HC114: 0x40011B72 | B1_P5_ROUTE_HC115: 0x40011B73 |
| B1_P5_ROUTE_HC116: 0x40011B74 | B1_P5_ROUTE_HC117: 0x40011B75 |
| B1_P5_ROUTE_HC118: 0x40011B76 | B1_P5_ROUTE_HC119: 0x40011B77 |
| B1_P5_ROUTE_HC120: 0x40011B78 | B1_P5_ROUTE_HC121: 0x40011B79 |
| B1_P5_ROUTE_HC122: 0x40011B7A | B1_P5_ROUTE_HC123: 0x40011B7B |
| B1_P5_ROUTE_HC124: 0x40011B7C | B1_P5_ROUTE_HC125: 0x40011B7D |
| B1_P5_ROUTE_HC126: 0x40011B7E | B1_P5_ROUTE_HC127: 0x40011B7F |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | hc_byte | | | | | | | |

UDB Channel HC Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|--------------|-------------------------------------|
| 7:0 | hc_byte[7:0] | RAM configuration bytes for channel |

1.3.1212 B[0..3]_P[0..7]_ROUTE_HV_L[0..15]

HV_L

Reset: N/A

Register : Address

B0_P0_ROUTE_HV_L0: 0x40010180
B0_P0_ROUTE_HV_L1: 0x40010181
B0_P0_ROUTE_HV_L2: 0x40010182
B0_P0_ROUTE_HV_L3: 0x40010183
B0_P0_ROUTE_HV_L4: 0x40010184
B0_P0_ROUTE_HV_L5: 0x40010185
B0_P0_ROUTE_HV_L6: 0x40010186
B0_P0_ROUTE_HV_L7: 0x40010187
B0_P0_ROUTE_HV_L8: 0x40010188
B0_P0_ROUTE_HV_L9: 0x40010189
B0_P0_ROUTE_HV_L10: 0x4001018A
B0_P0_ROUTE_HV_L11: 0x4001018B
B0_P0_ROUTE_HV_L12: 0x4001018C
B0_P0_ROUTE_HV_L13: 0x4001018D
B0_P0_ROUTE_HV_L14: 0x4001018E
B0_P0_ROUTE_HV_L15: 0x4001018F
B0_P1_ROUTE_HV_L0: 0x40010380
B0_P1_ROUTE_HV_L1: 0x40010381
B0_P1_ROUTE_HV_L2: 0x40010382
B0_P1_ROUTE_HV_L3: 0x40010383
B0_P1_ROUTE_HV_L4: 0x40010384
B0_P1_ROUTE_HV_L5: 0x40010385
B0_P1_ROUTE_HV_L6: 0x40010386
B0_P1_ROUTE_HV_L7: 0x40010387
B0_P1_ROUTE_HV_L8: 0x40010388
B0_P1_ROUTE_HV_L9: 0x40010389
B0_P1_ROUTE_HV_L10: 0x4001038A
B0_P1_ROUTE_HV_L11: 0x4001038B
B0_P1_ROUTE_HV_L12: 0x4001038C
B0_P1_ROUTE_HV_L13: 0x4001038D
B0_P1_ROUTE_HV_L14: 0x4001038E
B0_P1_ROUTE_HV_L15: 0x4001038F

1.3.1212 B[0..3]_P[0..7]_ROUTE_HV_L[0..15] (continued)

Register : Address

B0_P2_ROUTE_HV_L0: 0x40010580
 B0_P2_ROUTE_HV_L1: 0x40010581
 B0_P2_ROUTE_HV_L2: 0x40010582
 B0_P2_ROUTE_HV_L3: 0x40010583
 B0_P2_ROUTE_HV_L4: 0x40010584
 B0_P2_ROUTE_HV_L5: 0x40010585
 B0_P2_ROUTE_HV_L6: 0x40010586
 B0_P2_ROUTE_HV_L7: 0x40010587
 B0_P2_ROUTE_HV_L8: 0x40010588
 B0_P2_ROUTE_HV_L9: 0x40010589
 B0_P2_ROUTE_HV_L10: 0x4001058A
 B0_P2_ROUTE_HV_L11: 0x4001058B
 B0_P2_ROUTE_HV_L12: 0x4001058C
 B0_P2_ROUTE_HV_L13: 0x4001058D
 B0_P2_ROUTE_HV_L14: 0x4001058E
 B0_P2_ROUTE_HV_L15: 0x4001058F
 B0_P3_ROUTE_HV_L0: 0x40010780
 B0_P3_ROUTE_HV_L1: 0x40010781
 B0_P3_ROUTE_HV_L2: 0x40010782
 B0_P3_ROUTE_HV_L3: 0x40010783
 B0_P3_ROUTE_HV_L4: 0x40010784
 B0_P3_ROUTE_HV_L5: 0x40010785
 B0_P3_ROUTE_HV_L6: 0x40010786
 B0_P3_ROUTE_HV_L7: 0x40010787
 B0_P3_ROUTE_HV_L8: 0x40010788
 B0_P3_ROUTE_HV_L9: 0x40010789
 B0_P3_ROUTE_HV_L10: 0x4001078A
 B0_P3_ROUTE_HV_L11: 0x4001078B
 B0_P3_ROUTE_HV_L12: 0x4001078C
 B0_P3_ROUTE_HV_L13: 0x4001078D
 B0_P3_ROUTE_HV_L14: 0x4001078E
 B0_P3_ROUTE_HV_L15: 0x4001078F
 B0_P4_ROUTE_HV_L0: 0x40010980
 B0_P4_ROUTE_HV_L1: 0x40010981
 B0_P4_ROUTE_HV_L2: 0x40010982
 B0_P4_ROUTE_HV_L3: 0x40010983

1.3.1212 B[0..3]_P[0..7]_ROUTE_HV_L[0..15] (continued)

Register : Address

B0_P4_ROUTE_HV_L4: 0x40010984
B0_P4_ROUTE_HV_L5: 0x40010985
B0_P4_ROUTE_HV_L6: 0x40010986
B0_P4_ROUTE_HV_L7: 0x40010987
B0_P4_ROUTE_HV_L8: 0x40010988
B0_P4_ROUTE_HV_L9: 0x40010989
B0_P4_ROUTE_HV_L10: 0x4001098A
B0_P4_ROUTE_HV_L11: 0x4001098B
B0_P4_ROUTE_HV_L12: 0x4001098C
B0_P4_ROUTE_HV_L13: 0x4001098D
B0_P4_ROUTE_HV_L14: 0x4001098E
B0_P4_ROUTE_HV_L15: 0x4001098F
B0_P5_ROUTE_HV_L0: 0x40010B80
B0_P5_ROUTE_HV_L1: 0x40010B81
B0_P5_ROUTE_HV_L2: 0x40010B82
B0_P5_ROUTE_HV_L3: 0x40010B83
B0_P5_ROUTE_HV_L4: 0x40010B84
B0_P5_ROUTE_HV_L5: 0x40010B85
B0_P5_ROUTE_HV_L6: 0x40010B86
B0_P5_ROUTE_HV_L7: 0x40010B87
B0_P5_ROUTE_HV_L8: 0x40010B88
B0_P5_ROUTE_HV_L9: 0x40010B89
B0_P5_ROUTE_HV_L10: 0x40010B8A
B0_P5_ROUTE_HV_L11: 0x40010B8B
B0_P5_ROUTE_HV_L12: 0x40010B8C
B0_P5_ROUTE_HV_L13: 0x40010B8D
B0_P5_ROUTE_HV_L14: 0x40010B8E
B0_P5_ROUTE_HV_L15: 0x40010B8F
B0_P6_ROUTE_HV_L0: 0x40010D80
B0_P6_ROUTE_HV_L1: 0x40010D81
B0_P6_ROUTE_HV_L2: 0x40010D82
B0_P6_ROUTE_HV_L3: 0x40010D83
B0_P6_ROUTE_HV_L4: 0x40010D84
B0_P6_ROUTE_HV_L5: 0x40010D85
B0_P6_ROUTE_HV_L6: 0x40010D86
B0_P6_ROUTE_HV_L7: 0x40010D87

1.3.1212 B[0..3]_P[0..7]_ROUTE_HV_L[0..15] (continued)

Register : Address

B0_P6_ROUTE_HV_L8: 0x40010D88
 B0_P6_ROUTE_HV_L9: 0x40010D89
 B0_P6_ROUTE_HV_L10: 0x40010D8A
 B0_P6_ROUTE_HV_L11: 0x40010D8B
 B0_P6_ROUTE_HV_L12: 0x40010D8C
 B0_P6_ROUTE_HV_L13: 0x40010D8D
 B0_P6_ROUTE_HV_L14: 0x40010D8E
 B0_P6_ROUTE_HV_L15: 0x40010D8F
 B0_P7_ROUTE_HV_L0: 0x40010F80
 B0_P7_ROUTE_HV_L1: 0x40010F81
 B0_P7_ROUTE_HV_L2: 0x40010F82
 B0_P7_ROUTE_HV_L3: 0x40010F83
 B0_P7_ROUTE_HV_L4: 0x40010F84
 B0_P7_ROUTE_HV_L5: 0x40010F85
 B0_P7_ROUTE_HV_L6: 0x40010F86
 B0_P7_ROUTE_HV_L7: 0x40010F87
 B0_P7_ROUTE_HV_L8: 0x40010F88
 B0_P7_ROUTE_HV_L9: 0x40010F89
 B0_P7_ROUTE_HV_L10: 0x40010F8A
 B0_P7_ROUTE_HV_L11: 0x40010F8B
 B0_P7_ROUTE_HV_L12: 0x40010F8C
 B0_P7_ROUTE_HV_L13: 0x40010F8D
 B0_P7_ROUTE_HV_L14: 0x40010F8E
 B0_P7_ROUTE_HV_L15: 0x40010F8F
 B1_P2_ROUTE_HV_L0: 0x40011580
 B1_P2_ROUTE_HV_L1: 0x40011581
 B1_P2_ROUTE_HV_L2: 0x40011582
 B1_P2_ROUTE_HV_L3: 0x40011583
 B1_P2_ROUTE_HV_L4: 0x40011584
 B1_P2_ROUTE_HV_L5: 0x40011585
 B1_P2_ROUTE_HV_L6: 0x40011586
 B1_P2_ROUTE_HV_L7: 0x40011587
 B1_P2_ROUTE_HV_L8: 0x40011588
 B1_P2_ROUTE_HV_L9: 0x40011589
 B1_P2_ROUTE_HV_L10: 0x4001158A
 B1_P2_ROUTE_HV_L11: 0x4001158B

1.3.1212 B[0..3]_P[0..7]_ROUTE_HV_L[0..15] (continued)

Register : Address

B1_P2_ROUTE_HV_L12: 0x4001158C
B1_P2_ROUTE_HV_L13: 0x4001158D
B1_P2_ROUTE_HV_L14: 0x4001158E
B1_P2_ROUTE_HV_L15: 0x4001158F
B1_P3_ROUTE_HV_L0: 0x40011780
B1_P3_ROUTE_HV_L1: 0x40011781
B1_P3_ROUTE_HV_L2: 0x40011782
B1_P3_ROUTE_HV_L3: 0x40011783
B1_P3_ROUTE_HV_L4: 0x40011784
B1_P3_ROUTE_HV_L5: 0x40011785
B1_P3_ROUTE_HV_L6: 0x40011786
B1_P3_ROUTE_HV_L7: 0x40011787
B1_P3_ROUTE_HV_L8: 0x40011788
B1_P3_ROUTE_HV_L9: 0x40011789
B1_P3_ROUTE_HV_L10: 0x4001178A
B1_P3_ROUTE_HV_L11: 0x4001178B
B1_P3_ROUTE_HV_L12: 0x4001178C
B1_P3_ROUTE_HV_L13: 0x4001178D
B1_P3_ROUTE_HV_L14: 0x4001178E
B1_P3_ROUTE_HV_L15: 0x4001178F
B1_P4_ROUTE_HV_L0: 0x40011980
B1_P4_ROUTE_HV_L1: 0x40011981
B1_P4_ROUTE_HV_L2: 0x40011982
B1_P4_ROUTE_HV_L3: 0x40011983
B1_P4_ROUTE_HV_L4: 0x40011984
B1_P4_ROUTE_HV_L5: 0x40011985
B1_P4_ROUTE_HV_L6: 0x40011986
B1_P4_ROUTE_HV_L7: 0x40011987
B1_P4_ROUTE_HV_L8: 0x40011988
B1_P4_ROUTE_HV_L9: 0x40011989
B1_P4_ROUTE_HV_L10: 0x4001198A
B1_P4_ROUTE_HV_L11: 0x4001198B
B1_P4_ROUTE_HV_L12: 0x4001198C
B1_P4_ROUTE_HV_L13: 0x4001198D
B1_P4_ROUTE_HV_L14: 0x4001198E
B1_P4_ROUTE_HV_L15: 0x4001198F

1.3.1212 B[0..3]_P[0..7]_ROUTE_HV_L[0..15] (continued)

Register : Address

B1_P5_ROUTE_HV_L0: 0x40011B80

B1_P5_ROUTE_HV_L1: 0x40011B81

B1_P5_ROUTE_HV_L2: 0x40011B82

B1_P5_ROUTE_HV_L3: 0x40011B83

B1_P5_ROUTE_HV_L4: 0x40011B84

B1_P5_ROUTE_HV_L5: 0x40011B85

B1_P5_ROUTE_HV_L6: 0x40011B86

B1_P5_ROUTE_HV_L7: 0x40011B87

B1_P5_ROUTE_HV_L8: 0x40011B88

B1_P5_ROUTE_HV_L9: 0x40011B89

B1_P5_ROUTE_HV_L10: 0x40011B8A

B1_P5_ROUTE_HV_L11: 0x40011B8B

B1_P5_ROUTE_HV_L12: 0x40011B8C

B1_P5_ROUTE_HV_L13: 0x40011B8D

B1_P5_ROUTE_HV_L14: 0x40011B8E

B1_P5_ROUTE_HV_L15: 0x40011B8F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | hv_byte | | | | | | | |

UDB Channel HV Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|--------------|-------------------------------------|
| 7:0 | hv_byte[7:0] | RAM configuration bytes for channel |

1.3.1213 B[0..3]_P[0..7]_ROUTE_HS[0..23]

HS

Reset: N/A

Register : Address

| | |
|------------------------------|------------------------------|
| B0_P0_ROUTE_HS0: 0x40010190 | B0_P0_ROUTE_HS1: 0x40010191 |
| B0_P0_ROUTE_HS2: 0x40010192 | B0_P0_ROUTE_HS3: 0x40010193 |
| B0_P0_ROUTE_HS4: 0x40010194 | B0_P0_ROUTE_HS5: 0x40010195 |
| B0_P0_ROUTE_HS6: 0x40010196 | B0_P0_ROUTE_HS7: 0x40010197 |
| B0_P0_ROUTE_HS8: 0x40010198 | B0_P0_ROUTE_HS9: 0x40010199 |
| B0_P0_ROUTE_HS10: 0x4001019A | B0_P0_ROUTE_HS11: 0x4001019B |
| B0_P0_ROUTE_HS12: 0x4001019C | B0_P0_ROUTE_HS13: 0x4001019D |
| B0_P0_ROUTE_HS14: 0x4001019E | B0_P0_ROUTE_HS15: 0x4001019F |
| B0_P0_ROUTE_HS16: 0x400101A0 | B0_P0_ROUTE_HS17: 0x400101A1 |
| B0_P0_ROUTE_HS18: 0x400101A2 | B0_P0_ROUTE_HS19: 0x400101A3 |
| B0_P0_ROUTE_HS20: 0x400101A4 | B0_P0_ROUTE_HS21: 0x400101A5 |
| B0_P0_ROUTE_HS22: 0x400101A6 | B0_P0_ROUTE_HS23: 0x400101A7 |
| B0_P1_ROUTE_HS0: 0x40010390 | B0_P1_ROUTE_HS1: 0x40010391 |
| B0_P1_ROUTE_HS2: 0x40010392 | B0_P1_ROUTE_HS3: 0x40010393 |
| B0_P1_ROUTE_HS4: 0x40010394 | B0_P1_ROUTE_HS5: 0x40010395 |
| B0_P1_ROUTE_HS6: 0x40010396 | B0_P1_ROUTE_HS7: 0x40010397 |
| B0_P1_ROUTE_HS8: 0x40010398 | B0_P1_ROUTE_HS9: 0x40010399 |
| B0_P1_ROUTE_HS10: 0x4001039A | B0_P1_ROUTE_HS11: 0x4001039B |
| B0_P1_ROUTE_HS12: 0x4001039C | B0_P1_ROUTE_HS13: 0x4001039D |
| B0_P1_ROUTE_HS14: 0x4001039E | B0_P1_ROUTE_HS15: 0x4001039F |
| B0_P1_ROUTE_HS16: 0x400103A0 | B0_P1_ROUTE_HS17: 0x400103A1 |
| B0_P1_ROUTE_HS18: 0x400103A2 | B0_P1_ROUTE_HS19: 0x400103A3 |
| B0_P1_ROUTE_HS20: 0x400103A4 | B0_P1_ROUTE_HS21: 0x400103A5 |
| B0_P1_ROUTE_HS22: 0x400103A6 | B0_P1_ROUTE_HS23: 0x400103A7 |
| B0_P2_ROUTE_HS0: 0x40010590 | B0_P2_ROUTE_HS1: 0x40010591 |
| B0_P2_ROUTE_HS2: 0x40010592 | B0_P2_ROUTE_HS3: 0x40010593 |
| B0_P2_ROUTE_HS4: 0x40010594 | B0_P2_ROUTE_HS5: 0x40010595 |
| B0_P2_ROUTE_HS6: 0x40010596 | B0_P2_ROUTE_HS7: 0x40010597 |
| B0_P2_ROUTE_HS8: 0x40010598 | B0_P2_ROUTE_HS9: 0x40010599 |
| B0_P2_ROUTE_HS10: 0x4001059A | B0_P2_ROUTE_HS11: 0x4001059B |
| B0_P2_ROUTE_HS12: 0x4001059C | B0_P2_ROUTE_HS13: 0x4001059D |
| B0_P2_ROUTE_HS14: 0x4001059E | B0_P2_ROUTE_HS15: 0x4001059F |

1.3.1213 B[0..3]_P[0..7]_ROUTE_HS[0..23] (continued)

Register : Address

| | |
|------------------------------|------------------------------|
| B0_P2_ROUTE_HS16: 0x400105A0 | B0_P2_ROUTE_HS17: 0x400105A1 |
| B0_P2_ROUTE_HS18: 0x400105A2 | B0_P2_ROUTE_HS19: 0x400105A3 |
| B0_P2_ROUTE_HS20: 0x400105A4 | B0_P2_ROUTE_HS21: 0x400105A5 |
| B0_P2_ROUTE_HS22: 0x400105A6 | B0_P2_ROUTE_HS23: 0x400105A7 |
| B0_P3_ROUTE_HS0: 0x40010790 | B0_P3_ROUTE_HS1: 0x40010791 |
| B0_P3_ROUTE_HS2: 0x40010792 | B0_P3_ROUTE_HS3: 0x40010793 |
| B0_P3_ROUTE_HS4: 0x40010794 | B0_P3_ROUTE_HS5: 0x40010795 |
| B0_P3_ROUTE_HS6: 0x40010796 | B0_P3_ROUTE_HS7: 0x40010797 |
| B0_P3_ROUTE_HS8: 0x40010798 | B0_P3_ROUTE_HS9: 0x40010799 |
| B0_P3_ROUTE_HS10: 0x4001079A | B0_P3_ROUTE_HS11: 0x4001079B |
| B0_P3_ROUTE_HS12: 0x4001079C | B0_P3_ROUTE_HS13: 0x4001079D |
| B0_P3_ROUTE_HS14: 0x4001079E | B0_P3_ROUTE_HS15: 0x4001079F |
| B0_P3_ROUTE_HS16: 0x400107A0 | B0_P3_ROUTE_HS17: 0x400107A1 |
| B0_P3_ROUTE_HS18: 0x400107A2 | B0_P3_ROUTE_HS19: 0x400107A3 |
| B0_P3_ROUTE_HS20: 0x400107A4 | B0_P3_ROUTE_HS21: 0x400107A5 |
| B0_P3_ROUTE_HS22: 0x400107A6 | B0_P3_ROUTE_HS23: 0x400107A7 |
| B0_P4_ROUTE_HS0: 0x40010990 | B0_P4_ROUTE_HS1: 0x40010991 |
| B0_P4_ROUTE_HS2: 0x40010992 | B0_P4_ROUTE_HS3: 0x40010993 |
| B0_P4_ROUTE_HS4: 0x40010994 | B0_P4_ROUTE_HS5: 0x40010995 |
| B0_P4_ROUTE_HS6: 0x40010996 | B0_P4_ROUTE_HS7: 0x40010997 |
| B0_P4_ROUTE_HS8: 0x40010998 | B0_P4_ROUTE_HS9: 0x40010999 |
| B0_P4_ROUTE_HS10: 0x4001099A | B0_P4_ROUTE_HS11: 0x4001099B |
| B0_P4_ROUTE_HS12: 0x4001099C | B0_P4_ROUTE_HS13: 0x4001099D |
| B0_P4_ROUTE_HS14: 0x4001099E | B0_P4_ROUTE_HS15: 0x4001099F |
| B0_P4_ROUTE_HS16: 0x400109A0 | B0_P4_ROUTE_HS17: 0x400109A1 |
| B0_P4_ROUTE_HS18: 0x400109A2 | B0_P4_ROUTE_HS19: 0x400109A3 |
| B0_P4_ROUTE_HS20: 0x400109A4 | B0_P4_ROUTE_HS21: 0x400109A5 |
| B0_P4_ROUTE_HS22: 0x400109A6 | B0_P4_ROUTE_HS23: 0x400109A7 |
| B0_P5_ROUTE_HS0: 0x40010B90 | B0_P5_ROUTE_HS1: 0x40010B91 |
| B0_P5_ROUTE_HS2: 0x40010B92 | B0_P5_ROUTE_HS3: 0x40010B93 |
| B0_P5_ROUTE_HS4: 0x40010B94 | B0_P5_ROUTE_HS5: 0x40010B95 |
| B0_P5_ROUTE_HS6: 0x40010B96 | B0_P5_ROUTE_HS7: 0x40010B97 |
| B0_P5_ROUTE_HS8: 0x40010B98 | B0_P5_ROUTE_HS9: 0x40010B99 |
| B0_P5_ROUTE_HS10: 0x40010B9A | B0_P5_ROUTE_HS11: 0x40010B9B |
| B0_P5_ROUTE_HS12: 0x40010B9C | B0_P5_ROUTE_HS13: 0x40010B9D |
| B0_P5_ROUTE_HS14: 0x40010B9E | B0_P5_ROUTE_HS15: 0x40010B9F |

1.3.1213 B[0..3]_P[0..7]_ROUTE_HS[0..23] (continued)

Register : Address

| | |
|------------------------------|------------------------------|
| B0_P5_ROUTE_HS16: 0x40010BA0 | B0_P5_ROUTE_HS17: 0x40010BA1 |
| B0_P5_ROUTE_HS18: 0x40010BA2 | B0_P5_ROUTE_HS19: 0x40010BA3 |
| B0_P5_ROUTE_HS20: 0x40010BA4 | B0_P5_ROUTE_HS21: 0x40010BA5 |
| B0_P5_ROUTE_HS22: 0x40010BA6 | B0_P5_ROUTE_HS23: 0x40010BA7 |
| B0_P6_ROUTE_HS0: 0x40010D90 | B0_P6_ROUTE_HS1: 0x40010D91 |
| B0_P6_ROUTE_HS2: 0x40010D92 | B0_P6_ROUTE_HS3: 0x40010D93 |
| B0_P6_ROUTE_HS4: 0x40010D94 | B0_P6_ROUTE_HS5: 0x40010D95 |
| B0_P6_ROUTE_HS6: 0x40010D96 | B0_P6_ROUTE_HS7: 0x40010D97 |
| B0_P6_ROUTE_HS8: 0x40010D98 | B0_P6_ROUTE_HS9: 0x40010D99 |
| B0_P6_ROUTE_HS10: 0x40010D9A | B0_P6_ROUTE_HS11: 0x40010D9B |
| B0_P6_ROUTE_HS12: 0x40010D9C | B0_P6_ROUTE_HS13: 0x40010D9D |
| B0_P6_ROUTE_HS14: 0x40010D9E | B0_P6_ROUTE_HS15: 0x40010D9F |
| B0_P6_ROUTE_HS16: 0x40010DA0 | B0_P6_ROUTE_HS17: 0x40010DA1 |
| B0_P6_ROUTE_HS18: 0x40010DA2 | B0_P6_ROUTE_HS19: 0x40010DA3 |
| B0_P6_ROUTE_HS20: 0x40010DA4 | B0_P6_ROUTE_HS21: 0x40010DA5 |
| B0_P6_ROUTE_HS22: 0x40010DA6 | B0_P6_ROUTE_HS23: 0x40010DA7 |
| B0_P7_ROUTE_HS0: 0x40010F90 | B0_P7_ROUTE_HS1: 0x40010F91 |
| B0_P7_ROUTE_HS2: 0x40010F92 | B0_P7_ROUTE_HS3: 0x40010F93 |
| B0_P7_ROUTE_HS4: 0x40010F94 | B0_P7_ROUTE_HS5: 0x40010F95 |
| B0_P7_ROUTE_HS6: 0x40010F96 | B0_P7_ROUTE_HS7: 0x40010F97 |
| B0_P7_ROUTE_HS8: 0x40010F98 | B0_P7_ROUTE_HS9: 0x40010F99 |
| B0_P7_ROUTE_HS10: 0x40010F9A | B0_P7_ROUTE_HS11: 0x40010F9B |
| B0_P7_ROUTE_HS12: 0x40010F9C | B0_P7_ROUTE_HS13: 0x40010F9D |
| B0_P7_ROUTE_HS14: 0x40010F9E | B0_P7_ROUTE_HS15: 0x40010F9F |
| B0_P7_ROUTE_HS16: 0x40010FA0 | B0_P7_ROUTE_HS17: 0x40010FA1 |
| B0_P7_ROUTE_HS18: 0x40010FA2 | B0_P7_ROUTE_HS19: 0x40010FA3 |
| B0_P7_ROUTE_HS20: 0x40010FA4 | B0_P7_ROUTE_HS21: 0x40010FA5 |
| B0_P7_ROUTE_HS22: 0x40010FA6 | B0_P7_ROUTE_HS23: 0x40010FA7 |
| B1_P2_ROUTE_HS0: 0x40011590 | B1_P2_ROUTE_HS1: 0x40011591 |
| B1_P2_ROUTE_HS2: 0x40011592 | B1_P2_ROUTE_HS3: 0x40011593 |
| B1_P2_ROUTE_HS4: 0x40011594 | B1_P2_ROUTE_HS5: 0x40011595 |
| B1_P2_ROUTE_HS6: 0x40011596 | B1_P2_ROUTE_HS7: 0x40011597 |
| B1_P2_ROUTE_HS8: 0x40011598 | B1_P2_ROUTE_HS9: 0x40011599 |
| B1_P2_ROUTE_HS10: 0x4001159A | B1_P2_ROUTE_HS11: 0x4001159B |
| B1_P2_ROUTE_HS12: 0x4001159C | B1_P2_ROUTE_HS13: 0x4001159D |
| B1_P2_ROUTE_HS14: 0x4001159E | B1_P2_ROUTE_HS15: 0x4001159F |

1.3.1213 B[0..3]_P[0..7]_ROUTE_HS[0..23] (continued)

Register : Address

| | |
|------------------------------|------------------------------|
| B1_P2_ROUTE_HS16: 0x400115A0 | B1_P2_ROUTE_HS17: 0x400115A1 |
| B1_P2_ROUTE_HS18: 0x400115A2 | B1_P2_ROUTE_HS19: 0x400115A3 |
| B1_P2_ROUTE_HS20: 0x400115A4 | B1_P2_ROUTE_HS21: 0x400115A5 |
| B1_P2_ROUTE_HS22: 0x400115A6 | B1_P2_ROUTE_HS23: 0x400115A7 |
| B1_P3_ROUTE_HS0: 0x40011790 | B1_P3_ROUTE_HS1: 0x40011791 |
| B1_P3_ROUTE_HS2: 0x40011792 | B1_P3_ROUTE_HS3: 0x40011793 |
| B1_P3_ROUTE_HS4: 0x40011794 | B1_P3_ROUTE_HS5: 0x40011795 |
| B1_P3_ROUTE_HS6: 0x40011796 | B1_P3_ROUTE_HS7: 0x40011797 |
| B1_P3_ROUTE_HS8: 0x40011798 | B1_P3_ROUTE_HS9: 0x40011799 |
| B1_P3_ROUTE_HS10: 0x4001179A | B1_P3_ROUTE_HS11: 0x4001179B |
| B1_P3_ROUTE_HS12: 0x4001179C | B1_P3_ROUTE_HS13: 0x4001179D |
| B1_P3_ROUTE_HS14: 0x4001179E | B1_P3_ROUTE_HS15: 0x4001179F |
| B1_P3_ROUTE_HS16: 0x400117A0 | B1_P3_ROUTE_HS17: 0x400117A1 |
| B1_P3_ROUTE_HS18: 0x400117A2 | B1_P3_ROUTE_HS19: 0x400117A3 |
| B1_P3_ROUTE_HS20: 0x400117A4 | B1_P3_ROUTE_HS21: 0x400117A5 |
| B1_P3_ROUTE_HS22: 0x400117A6 | B1_P3_ROUTE_HS23: 0x400117A7 |
| B1_P4_ROUTE_HS0: 0x40011990 | B1_P4_ROUTE_HS1: 0x40011991 |
| B1_P4_ROUTE_HS2: 0x40011992 | B1_P4_ROUTE_HS3: 0x40011993 |
| B1_P4_ROUTE_HS4: 0x40011994 | B1_P4_ROUTE_HS5: 0x40011995 |
| B1_P4_ROUTE_HS6: 0x40011996 | B1_P4_ROUTE_HS7: 0x40011997 |
| B1_P4_ROUTE_HS8: 0x40011998 | B1_P4_ROUTE_HS9: 0x40011999 |
| B1_P4_ROUTE_HS10: 0x4001199A | B1_P4_ROUTE_HS11: 0x4001199B |
| B1_P4_ROUTE_HS12: 0x4001199C | B1_P4_ROUTE_HS13: 0x4001199D |
| B1_P4_ROUTE_HS14: 0x4001199E | B1_P4_ROUTE_HS15: 0x4001199F |
| B1_P4_ROUTE_HS16: 0x400119A0 | B1_P4_ROUTE_HS17: 0x400119A1 |
| B1_P4_ROUTE_HS18: 0x400119A2 | B1_P4_ROUTE_HS19: 0x400119A3 |
| B1_P4_ROUTE_HS20: 0x400119A4 | B1_P4_ROUTE_HS21: 0x400119A5 |
| B1_P4_ROUTE_HS22: 0x400119A6 | B1_P4_ROUTE_HS23: 0x400119A7 |
| B1_P5_ROUTE_HS0: 0x40011B90 | B1_P5_ROUTE_HS1: 0x40011B91 |
| B1_P5_ROUTE_HS2: 0x40011B92 | B1_P5_ROUTE_HS3: 0x40011B93 |
| B1_P5_ROUTE_HS4: 0x40011B94 | B1_P5_ROUTE_HS5: 0x40011B95 |
| B1_P5_ROUTE_HS6: 0x40011B96 | B1_P5_ROUTE_HS7: 0x40011B97 |
| B1_P5_ROUTE_HS8: 0x40011B98 | B1_P5_ROUTE_HS9: 0x40011B99 |
| B1_P5_ROUTE_HS10: 0x40011B9A | B1_P5_ROUTE_HS11: 0x40011B9B |
| B1_P5_ROUTE_HS12: 0x40011B9C | B1_P5_ROUTE_HS13: 0x40011B9D |
| B1_P5_ROUTE_HS14: 0x40011B9E | B1_P5_ROUTE_HS15: 0x40011B9F |

1.3.1213 B[0..3]_P[0..7]_ROUTE_HS[0..23] (continued)

Register : Address

| | |
|------------------------------|------------------------------|
| B1_P5_ROUTE_HS16: 0x40011BA0 | B1_P5_ROUTE_HS17: 0x40011BA1 |
| B1_P5_ROUTE_HS18: 0x40011BA2 | B1_P5_ROUTE_HS19: 0x40011BA3 |
| B1_P5_ROUTE_HS20: 0x40011BA4 | B1_P5_ROUTE_HS21: 0x40011BA5 |
| B1_P5_ROUTE_HS22: 0x40011BA6 | B1_P5_ROUTE_HS23: 0x40011BA7 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | hs_byte | | | | | | | |

UDB Channel HS Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|--------------|-------------------------------------|
| 7:0 | hs_byte[7:0] | RAM configuration bytes for channel |

1.3.1214 B[0..3]_P[0..7]_ROUTE_HV_R[0..15]

HV_R

Reset: N/A

Register : Address

B0_P0_ROUTE_HV_R0: 0x400101A8
 B0_P0_ROUTE_HV_R1: 0x400101A9
 B0_P0_ROUTE_HV_R2: 0x400101AA
 B0_P0_ROUTE_HV_R3: 0x400101AB
 B0_P0_ROUTE_HV_R4: 0x400101AC
 B0_P0_ROUTE_HV_R5: 0x400101AD
 B0_P0_ROUTE_HV_R6: 0x400101AE
 B0_P0_ROUTE_HV_R7: 0x400101AF
 B0_P0_ROUTE_HV_R8: 0x400101B0
 B0_P0_ROUTE_HV_R9: 0x400101B1
 B0_P0_ROUTE_HV_R10: 0x400101B2
 B0_P0_ROUTE_HV_R11: 0x400101B3
 B0_P0_ROUTE_HV_R12: 0x400101B4
 B0_P0_ROUTE_HV_R13: 0x400101B5
 B0_P0_ROUTE_HV_R14: 0x400101B6
 B0_P0_ROUTE_HV_R15: 0x400101B7
 B0_P1_ROUTE_HV_R0: 0x400103A8
 B0_P1_ROUTE_HV_R1: 0x400103A9
 B0_P1_ROUTE_HV_R2: 0x400103AA
 B0_P1_ROUTE_HV_R3: 0x400103AB
 B0_P1_ROUTE_HV_R4: 0x400103AC
 B0_P1_ROUTE_HV_R5: 0x400103AD
 B0_P1_ROUTE_HV_R6: 0x400103AE
 B0_P1_ROUTE_HV_R7: 0x400103AF
 B0_P1_ROUTE_HV_R8: 0x400103B0
 B0_P1_ROUTE_HV_R9: 0x400103B1
 B0_P1_ROUTE_HV_R10: 0x400103B2
 B0_P1_ROUTE_HV_R11: 0x400103B3
 B0_P1_ROUTE_HV_R12: 0x400103B4
 B0_P1_ROUTE_HV_R13: 0x400103B5
 B0_P1_ROUTE_HV_R14: 0x400103B6
 B0_P1_ROUTE_HV_R15: 0x400103B7

1.3.1214 B[0..3]_P[0..7]_ROUTE_HV_R[0..15] (continued)

Register : Address

B0_P2_ROUTE_HV_R0: 0x400105A8
B0_P2_ROUTE_HV_R1: 0x400105A9
B0_P2_ROUTE_HV_R2: 0x400105AA
B0_P2_ROUTE_HV_R3: 0x400105AB
B0_P2_ROUTE_HV_R4: 0x400105AC
B0_P2_ROUTE_HV_R5: 0x400105AD
B0_P2_ROUTE_HV_R6: 0x400105AE
B0_P2_ROUTE_HV_R7: 0x400105AF
B0_P2_ROUTE_HV_R8: 0x400105B0
B0_P2_ROUTE_HV_R9: 0x400105B1
B0_P2_ROUTE_HV_R10: 0x400105B2
B0_P2_ROUTE_HV_R11: 0x400105B3
B0_P2_ROUTE_HV_R12: 0x400105B4
B0_P2_ROUTE_HV_R13: 0x400105B5
B0_P2_ROUTE_HV_R14: 0x400105B6
B0_P2_ROUTE_HV_R15: 0x400105B7
B0_P3_ROUTE_HV_R0: 0x400107A8
B0_P3_ROUTE_HV_R1: 0x400107A9
B0_P3_ROUTE_HV_R2: 0x400107AA
B0_P3_ROUTE_HV_R3: 0x400107AB
B0_P3_ROUTE_HV_R4: 0x400107AC
B0_P3_ROUTE_HV_R5: 0x400107AD
B0_P3_ROUTE_HV_R6: 0x400107AE
B0_P3_ROUTE_HV_R7: 0x400107AF
B0_P3_ROUTE_HV_R8: 0x400107B0
B0_P3_ROUTE_HV_R9: 0x400107B1
B0_P3_ROUTE_HV_R10: 0x400107B2
B0_P3_ROUTE_HV_R11: 0x400107B3
B0_P3_ROUTE_HV_R12: 0x400107B4
B0_P3_ROUTE_HV_R13: 0x400107B5
B0_P3_ROUTE_HV_R14: 0x400107B6
B0_P3_ROUTE_HV_R15: 0x400107B7
B0_P4_ROUTE_HV_R0: 0x400109A8
B0_P4_ROUTE_HV_R1: 0x400109A9
B0_P4_ROUTE_HV_R2: 0x400109AA
B0_P4_ROUTE_HV_R3: 0x400109AB

1.3.1214 B[0..3]_P[0..7]_ROUTE_HV_R[0..15] (continued)

Register : Address

B0_P4_ROUTE_HV_R4: 0x400109AC
 B0_P4_ROUTE_HV_R5: 0x400109AD
 B0_P4_ROUTE_HV_R6: 0x400109AE
 B0_P4_ROUTE_HV_R7: 0x400109AF
 B0_P4_ROUTE_HV_R8: 0x400109B0
 B0_P4_ROUTE_HV_R9: 0x400109B1
 B0_P4_ROUTE_HV_R10: 0x400109B2
 B0_P4_ROUTE_HV_R11: 0x400109B3
 B0_P4_ROUTE_HV_R12: 0x400109B4
 B0_P4_ROUTE_HV_R13: 0x400109B5
 B0_P4_ROUTE_HV_R14: 0x400109B6
 B0_P4_ROUTE_HV_R15: 0x400109B7
 B0_P5_ROUTE_HV_R0: 0x40010BA8
 B0_P5_ROUTE_HV_R1: 0x40010BA9
 B0_P5_ROUTE_HV_R2: 0x40010BAA
 B0_P5_ROUTE_HV_R3: 0x40010BAB
 B0_P5_ROUTE_HV_R4: 0x40010BAC
 B0_P5_ROUTE_HV_R5: 0x40010BAD
 B0_P5_ROUTE_HV_R6: 0x40010BAE
 B0_P5_ROUTE_HV_R7: 0x40010BAF
 B0_P5_ROUTE_HV_R8: 0x40010BB0
 B0_P5_ROUTE_HV_R9: 0x40010BB1
 B0_P5_ROUTE_HV_R10: 0x40010BB2
 B0_P5_ROUTE_HV_R11: 0x40010BB3
 B0_P5_ROUTE_HV_R12: 0x40010BB4
 B0_P5_ROUTE_HV_R13: 0x40010BB5
 B0_P5_ROUTE_HV_R14: 0x40010BB6
 B0_P5_ROUTE_HV_R15: 0x40010BB7
 B0_P6_ROUTE_HV_R0: 0x40010DA8
 B0_P6_ROUTE_HV_R1: 0x40010DA9
 B0_P6_ROUTE_HV_R2: 0x40010DAA
 B0_P6_ROUTE_HV_R3: 0x40010DAB
 B0_P6_ROUTE_HV_R4: 0x40010DAC
 B0_P6_ROUTE_HV_R5: 0x40010DAD
 B0_P6_ROUTE_HV_R6: 0x40010DAE
 B0_P6_ROUTE_HV_R7: 0x40010DAF

1.3.1214 B[0..3]_P[0..7]_ROUTE_HV_R[0..15] (continued)

Register : Address

B0_P6_ROUTE_HV_R8: 0x40010DB0
 B0_P6_ROUTE_HV_R9: 0x40010DB1
 B0_P6_ROUTE_HV_R10: 0x40010DB2
 B0_P6_ROUTE_HV_R11: 0x40010DB3
 B0_P6_ROUTE_HV_R12: 0x40010DB4
 B0_P6_ROUTE_HV_R13: 0x40010DB5
 B0_P6_ROUTE_HV_R14: 0x40010DB6
 B0_P6_ROUTE_HV_R15: 0x40010DB7
 B0_P7_ROUTE_HV_R0: 0x40010FA8
 B0_P7_ROUTE_HV_R1: 0x40010FA9
 B0_P7_ROUTE_HV_R2: 0x40010FAA
 B0_P7_ROUTE_HV_R3: 0x40010FAB
 B0_P7_ROUTE_HV_R4: 0x40010FAC
 B0_P7_ROUTE_HV_R5: 0x40010FAD
 B0_P7_ROUTE_HV_R6: 0x40010FAE
 B0_P7_ROUTE_HV_R7: 0x40010FAF
 B0_P7_ROUTE_HV_R8: 0x40010FB0
 B0_P7_ROUTE_HV_R9: 0x40010FB1
 B0_P7_ROUTE_HV_R10: 0x40010FB2
 B0_P7_ROUTE_HV_R11: 0x40010FB3
 B0_P7_ROUTE_HV_R12: 0x40010FB4
 B0_P7_ROUTE_HV_R13: 0x40010FB5
 B0_P7_ROUTE_HV_R14: 0x40010FB6
 B0_P7_ROUTE_HV_R15: 0x40010FB7
 B1_P2_ROUTE_HV_R0: 0x400115A8
 B1_P2_ROUTE_HV_R1: 0x400115A9
 B1_P2_ROUTE_HV_R2: 0x400115AA
 B1_P2_ROUTE_HV_R3: 0x400115AB
 B1_P2_ROUTE_HV_R4: 0x400115AC
 B1_P2_ROUTE_HV_R5: 0x400115AD
 B1_P2_ROUTE_HV_R6: 0x400115AE
 B1_P2_ROUTE_HV_R7: 0x400115AF
 B1_P2_ROUTE_HV_R8: 0x400115B0
 B1_P2_ROUTE_HV_R9: 0x400115B1
 B1_P2_ROUTE_HV_R10: 0x400115B2
 B1_P2_ROUTE_HV_R11: 0x400115B3

1.3.1214 B[0..3]_P[0..7]_ROUTE_HV_R[0..15] (continued)

Register : Address

B1_P2_ROUTE_HV_R12: 0x400115B4

B1_P2_ROUTE_HV_R13: 0x400115B5

B1_P2_ROUTE_HV_R14: 0x400115B6

B1_P2_ROUTE_HV_R15: 0x400115B7

B1_P3_ROUTE_HV_R0: 0x400117A8

B1_P3_ROUTE_HV_R1: 0x400117A9

B1_P3_ROUTE_HV_R2: 0x400117AA

B1_P3_ROUTE_HV_R3: 0x400117AB

B1_P3_ROUTE_HV_R4: 0x400117AC

B1_P3_ROUTE_HV_R5: 0x400117AD

B1_P3_ROUTE_HV_R6: 0x400117AE

B1_P3_ROUTE_HV_R7: 0x400117AF

B1_P3_ROUTE_HV_R8: 0x400117B0

B1_P3_ROUTE_HV_R9: 0x400117B1

B1_P3_ROUTE_HV_R10: 0x400117B2

B1_P3_ROUTE_HV_R11: 0x400117B3

B1_P3_ROUTE_HV_R12: 0x400117B4

B1_P3_ROUTE_HV_R13: 0x400117B5

B1_P3_ROUTE_HV_R14: 0x400117B6

B1_P3_ROUTE_HV_R15: 0x400117B7

B1_P4_ROUTE_HV_R0: 0x400119A8

B1_P4_ROUTE_HV_R1: 0x400119A9

B1_P4_ROUTE_HV_R2: 0x400119AA

B1_P4_ROUTE_HV_R3: 0x400119AB

B1_P4_ROUTE_HV_R4: 0x400119AC

B1_P4_ROUTE_HV_R5: 0x400119AD

B1_P4_ROUTE_HV_R6: 0x400119AE

B1_P4_ROUTE_HV_R7: 0x400119AF

B1_P4_ROUTE_HV_R8: 0x400119B0

B1_P4_ROUTE_HV_R9: 0x400119B1

B1_P4_ROUTE_HV_R10: 0x400119B2

B1_P4_ROUTE_HV_R11: 0x400119B3

B1_P4_ROUTE_HV_R12: 0x400119B4

B1_P4_ROUTE_HV_R13: 0x400119B5

B1_P4_ROUTE_HV_R14: 0x400119B6

B1_P4_ROUTE_HV_R15: 0x400119B7

1.3.1214 B[0..3]_P[0..7]_ROUTE_HV_R[0..15] (continued)

Register : Address

- B1_P5_ROUTE_HV_R0: 0x40011BA8
- B1_P5_ROUTE_HV_R1: 0x40011BA9
- B1_P5_ROUTE_HV_R2: 0x40011BAA
- B1_P5_ROUTE_HV_R3: 0x40011BAB
- B1_P5_ROUTE_HV_R4: 0x40011BAC
- B1_P5_ROUTE_HV_R5: 0x40011BAD
- B1_P5_ROUTE_HV_R6: 0x40011BAE
- B1_P5_ROUTE_HV_R7: 0x40011BAF
- B1_P5_ROUTE_HV_R8: 0x40011BB0
- B1_P5_ROUTE_HV_R9: 0x40011BB1
- B1_P5_ROUTE_HV_R10: 0x40011BB2
- B1_P5_ROUTE_HV_R11: 0x40011BB3
- B1_P5_ROUTE_HV_R12: 0x40011BB4
- B1_P5_ROUTE_HV_R13: 0x40011BB5
- B1_P5_ROUTE_HV_R14: 0x40011BB6
- B1_P5_ROUTE_HV_R15: 0x40011BB7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | hv_byte | | | | | | | |

UDB Channel HV Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|--------------|-------------------------------------|
| 7:0 | hv_byte[7:0] | RAM configuration bytes for channel |

1.3.1215 B[0..3]_P[0..7]_ROUTE_PLD0IN0 PLD0IN0

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD0IN0: 0x400101C0

B0_P1_ROUTE_PLD0IN0: 0x400103C0

B0_P2_ROUTE_PLD0IN0: 0x400105C0

B0_P3_ROUTE_PLD0IN0: 0x400107C0

B0_P4_ROUTE_PLD0IN0: 0x400109C0

B0_P5_ROUTE_PLD0IN0: 0x40010BC0

B0_P6_ROUTE_PLD0IN0: 0x40010DC0

B0_P7_ROUTE_PLD0IN0: 0x40010FC0

B1_P2_ROUTE_PLD0IN0: 0x400115C0

B1_P3_ROUTE_PLD0IN0: 0x400117C0

B1_P4_ROUTE_PLD0IN0: 0x400119C0

B1_P5_ROUTE_PLD0IN0: 0x40011BC0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

UDB Channel PI Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration nibble for BOTTOM UDB port interface configuration |
| 3:0 | pi_top[3:0] | RAM configuration nibble for TOP UDB port interface configuration |

1.3.1216 B[0..3]_P[0..7]_ROUTE_PLD0IN1

PLD0IN1

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD0IN1: 0x400101C2
 B0_P1_ROUTE_PLD0IN1: 0x400103C2
 B0_P2_ROUTE_PLD0IN1: 0x400105C2
 B0_P3_ROUTE_PLD0IN1: 0x400107C2
 B0_P4_ROUTE_PLD0IN1: 0x400109C2
 B0_P5_ROUTE_PLD0IN1: 0x40010BC2
 B0_P6_ROUTE_PLD0IN1: 0x40010DC2
 B0_P7_ROUTE_PLD0IN1: 0x40010FC2
 B1_P2_ROUTE_PLD0IN1: 0x400115C2
 B1_P3_ROUTE_PLD0IN1: 0x400117C2
 B1_P4_ROUTE_PLD0IN1: 0x400119C2
 B1_P5_ROUTE_PLD0IN1: 0x40011BC2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

UDB Channel PI Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration nibble for BOTTOM UDB port interface configuration |
| 3:0 | pi_top[3:0] | RAM configuration nibble for TOP UDB port interface configuration |

1.3.1217 B[0..3]_P[0..7]_ROUTE_PLD0IN2 PLD0IN2

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD0IN2: 0x400101C4

B0_P1_ROUTE_PLD0IN2: 0x400103C4

B0_P2_ROUTE_PLD0IN2: 0x400105C4

B0_P3_ROUTE_PLD0IN2: 0x400107C4

B0_P4_ROUTE_PLD0IN2: 0x400109C4

B0_P5_ROUTE_PLD0IN2: 0x40010BC4

B0_P6_ROUTE_PLD0IN2: 0x40010DC4

B0_P7_ROUTE_PLD0IN2: 0x40010FC4

B1_P2_ROUTE_PLD0IN2: 0x400115C4

B1_P3_ROUTE_PLD0IN2: 0x400117C4

B1_P4_ROUTE_PLD0IN2: 0x400119C4

B1_P5_ROUTE_PLD0IN2: 0x40011BC4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

UDB Channel PI Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration nibble for BOTTOM UDB port interface configuration |
| 3:0 | pi_top[3:0] | RAM configuration nibble for TOP UDB port interface configuration |

1.3.1218 B[0..3]_P[0..7]_ROUTE_PLD1IN0

PLD1IN0

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD1IN0: 0x400101CA

B0_P1_ROUTE_PLD1IN0: 0x400103CA

B0_P2_ROUTE_PLD1IN0: 0x400105CA

B0_P3_ROUTE_PLD1IN0: 0x400107CA

B0_P4_ROUTE_PLD1IN0: 0x400109CA

B0_P5_ROUTE_PLD1IN0: 0x40010BCA

B0_P6_ROUTE_PLD1IN0: 0x40010DCA

B0_P7_ROUTE_PLD1IN0: 0x40010FCA

B1_P2_ROUTE_PLD1IN0: 0x400115CA

B1_P3_ROUTE_PLD1IN0: 0x400117CA

B1_P4_ROUTE_PLD1IN0: 0x400119CA

B1_P5_ROUTE_PLD1IN0: 0x40011BCA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

UDB Channel PI Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration nibble for BOTTOM UDB port interface configuration |
| 3:0 | pi_top[3:0] | RAM configuration nibble for TOP UDB port interface configuration |

1.3.1219 B[0..3]_P[0..7]_ROUTE_PLD1IN1 PLD1IN1

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD1IN1: 0x400101CC

B0_P1_ROUTE_PLD1IN1: 0x400103CC

B0_P2_ROUTE_PLD1IN1: 0x400105CC

B0_P3_ROUTE_PLD1IN1: 0x400107CC

B0_P4_ROUTE_PLD1IN1: 0x400109CC

B0_P5_ROUTE_PLD1IN1: 0x40010BCC

B0_P6_ROUTE_PLD1IN1: 0x40010DCC

B0_P7_ROUTE_PLD1IN1: 0x40010FCC

B1_P2_ROUTE_PLD1IN1: 0x400115CC

B1_P3_ROUTE_PLD1IN1: 0x400117CC

B1_P4_ROUTE_PLD1IN1: 0x400119CC

B1_P5_ROUTE_PLD1IN1: 0x40011BCC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

UDB Channel PI Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration nibble for BOTTOM UDB port interface configuration |
| 3:0 | pi_top[3:0] | RAM configuration nibble for TOP UDB port interface configuration |

1.3.1220 B[0..3]_P[0..7]_ROUTE_PLD1IN2

PLD1IN2

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD1IN2: 0x400101CE
 B0_P1_ROUTE_PLD1IN2: 0x400103CE
 B0_P2_ROUTE_PLD1IN2: 0x400105CE
 B0_P3_ROUTE_PLD1IN2: 0x400107CE
 B0_P4_ROUTE_PLD1IN2: 0x400109CE
 B0_P5_ROUTE_PLD1IN2: 0x40010BCE
 B0_P6_ROUTE_PLD1IN2: 0x40010DCE
 B0_P7_ROUTE_PLD1IN2: 0x40010FCE
 B1_P2_ROUTE_PLD1IN2: 0x400115CE
 B1_P3_ROUTE_PLD1IN2: 0x400117CE
 B1_P4_ROUTE_PLD1IN2: 0x400119CE
 B1_P5_ROUTE_PLD1IN2: 0x40011BCE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

UDB Channel PI Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration nibble for BOTTOM UDB port interface configuration |
| 3:0 | pi_top[3:0] | RAM configuration nibble for TOP UDB port interface configuration |

1.3.1221 B[0..3]_P[0..7]_ROUTE_DPINO DPINO

Reset: N/A

Register : Address

B0_P0_ROUTE_DPINO: 0x400101D0

B0_P1_ROUTE_DPINO: 0x400103D0

B0_P2_ROUTE_DPINO: 0x400105D0

B0_P3_ROUTE_DPINO: 0x400107D0

B0_P4_ROUTE_DPINO: 0x400109D0

B0_P5_ROUTE_DPINO: 0x40010BD0

B0_P6_ROUTE_DPINO: 0x40010DD0

B0_P7_ROUTE_DPINO: 0x40010FD0

B1_P2_ROUTE_DPINO: 0x400115D0

B1_P3_ROUTE_DPINO: 0x400117D0

B1_P4_ROUTE_DPINO: 0x400119D0

B1_P5_ROUTE_DPINO: 0x40011BD0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

UDB Channel PI Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration nibble for BOTTOM UDB port interface configuration |
| 3:0 | pi_top[3:0] | RAM configuration nibble for TOP UDB port interface configuration |

1.3.1222 B[0..3]_P[0..7]_ROUTE_DPIN1

DPIN1

Reset: N/A

Register : Address

B0_P0_ROUTE_DPIN1: 0x400101D2

B0_P1_ROUTE_DPIN1: 0x400103D2

B0_P2_ROUTE_DPIN1: 0x400105D2

B0_P3_ROUTE_DPIN1: 0x400107D2

B0_P4_ROUTE_DPIN1: 0x400109D2

B0_P5_ROUTE_DPIN1: 0x40010BD2

B0_P6_ROUTE_DPIN1: 0x40010DD2

B0_P7_ROUTE_DPIN1: 0x40010FD2

B1_P2_ROUTE_DPIN1: 0x400115D2

B1_P3_ROUTE_DPIN1: 0x400117D2

B1_P4_ROUTE_DPIN1: 0x400119D2

B1_P5_ROUTE_DPIN1: 0x40011BD2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|--------|---|--------|---|-------|---|
| SW Access:Reset | NA:00 | | R/W:UU | | R/W:UU | | NA:00 | |
| HW Access | NA | | R | | R | | NA | |
| Name | | | pi_bot | | pi_top | | | |

UDB Channel PI Tile Configuration (half populated)

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 5:4 | pi_bot[1:0] | RAM configuration bits (2) for BOTTOM UDB port interface configuration |
| 3:2 | pi_top[1:0] | RAM configuration bits (2) for TOP UDB port interface configuration |

1.3.1223 B[0..3]_P[0..7]_ROUTE_SCIN SCIN

Reset: N/A

Register : Address

B0_P0_ROUTE_SCIN: 0x400101D6

B0_P1_ROUTE_SCIN: 0x400103D6

B0_P2_ROUTE_SCIN: 0x400105D6

B0_P3_ROUTE_SCIN: 0x400107D6

B0_P4_ROUTE_SCIN: 0x400109D6

B0_P5_ROUTE_SCIN: 0x40010BD6

B0_P6_ROUTE_SCIN: 0x40010DD6

B0_P7_ROUTE_SCIN: 0x40010FD6

B1_P2_ROUTE_SCIN: 0x400115D6

B1_P3_ROUTE_SCIN: 0x400117D6

B1_P4_ROUTE_SCIN: 0x400119D6

B1_P5_ROUTE_SCIN: 0x40011BD6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

UDB Channel PI Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration nibble for BOTTOM UDB port interface configuration |
| 3:0 | pi_top[3:0] | RAM configuration nibble for TOP UDB port interface configuration |

1.3.1224 B[0..3]_P[0..7]_ROUTE_SCI0IN

SCI0IN

Reset: N/A

Register : Address

B0_P0_ROUTE_SCI0IN: 0x400101D8

B0_P1_ROUTE_SCI0IN: 0x400103D8

B0_P2_ROUTE_SCI0IN: 0x400105D8

B0_P3_ROUTE_SCI0IN: 0x400107D8

B0_P4_ROUTE_SCI0IN: 0x400109D8

B0_P5_ROUTE_SCI0IN: 0x40010BD8

B0_P6_ROUTE_SCI0IN: 0x40010DD8

B0_P7_ROUTE_SCI0IN: 0x40010FD8

B1_P2_ROUTE_SCI0IN: 0x400115D8

B1_P3_ROUTE_SCI0IN: 0x400117D8

B1_P4_ROUTE_SCI0IN: 0x400119D8

B1_P5_ROUTE_SCI0IN: 0x40011BD8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

UDB Channel PI Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration nibble for BOTTOM UDB port interface configuration |
| 3:0 | pi_top[3:0] | RAM configuration nibble for TOP UDB port interface configuration |

1.3.1225 B[0..3]_P[0..7]_ROUTE_RCIN RCIN

Reset: N/A

Register : Address

B0_P0_ROUTE_RCIN: 0x400101DE

B0_P1_ROUTE_RCIN: 0x400103DE

B0_P2_ROUTE_RCIN: 0x400105DE

B0_P3_ROUTE_RCIN: 0x400107DE

B0_P4_ROUTE_RCIN: 0x400109DE

B0_P5_ROUTE_RCIN: 0x40010BDE

B0_P6_ROUTE_RCIN: 0x40010DDE

B0_P7_ROUTE_RCIN: 0x40010FDE

B1_P2_ROUTE_RCIN: 0x400115DE

B1_P3_ROUTE_RCIN: 0x400117DE

B1_P4_ROUTE_RCIN: 0x400119DE

B1_P5_ROUTE_RCIN: 0x40011BDE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

UDB Channel PI Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration nibble for BOTTOM UDB port interface configuration |
| 3:0 | pi_top[3:0] | RAM configuration nibble for TOP UDB port interface configuration |

1.3.1226 B[0..3]_P[0..7]_ROUTE_VS0

VS0

Reset: N/A

Register : Address

| | |
|-----------------------------|-----------------------------|
| B0_P0_ROUTE_VS0: 0x400101E0 | B0_P1_ROUTE_VS0: 0x400103E0 |
| B0_P2_ROUTE_VS0: 0x400105E0 | B0_P3_ROUTE_VS0: 0x400107E0 |
| B0_P4_ROUTE_VS0: 0x400109E0 | B0_P5_ROUTE_VS0: 0x40010BE0 |
| B0_P6_ROUTE_VS0: 0x40010DE0 | B0_P7_ROUTE_VS0: 0x40010FE0 |
| B1_P2_ROUTE_VS0: 0x400115E0 | B1_P3_ROUTE_VS0: 0x400117E0 |
| B1_P4_ROUTE_VS0: 0x400119E0 | B1_P5_ROUTE_VS0: 0x40011BE0 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

UDB Channel VS Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration nibble for BOTTOM UDB vertical segmentation configuration |
| 3:0 | vs_top[3:0] | RAM configuration nibble for TOP UDB vertical segmentation configuration |

1.3.1227 B[0..3]_P[0..7]_ROUTE_VS1 VS1

Reset: N/A

Register : Address

| | |
|-----------------------------|-----------------------------|
| B0_P0_ROUTE_VS1: 0x400101E2 | B0_P1_ROUTE_VS1: 0x400103E2 |
| B0_P2_ROUTE_VS1: 0x400105E2 | B0_P3_ROUTE_VS1: 0x400107E2 |
| B0_P4_ROUTE_VS1: 0x400109E2 | B0_P5_ROUTE_VS1: 0x40010BE2 |
| B0_P6_ROUTE_VS1: 0x40010DE2 | B0_P7_ROUTE_VS1: 0x40010FE2 |
| B1_P2_ROUTE_VS1: 0x400115E2 | B1_P3_ROUTE_VS1: 0x400117E2 |
| B1_P4_ROUTE_VS1: 0x400119E2 | B1_P5_ROUTE_VS1: 0x40011BE2 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

UDB Channel VS Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration nibble for BOTTOM UDB vertical segmentation configuration |
| 3:0 | vs_top[3:0] | RAM configuration nibble for TOP UDB vertical segmentation configuration |

1.3.1228 B[0..3]_P[0..7]_ROUTE_VS2

VS2

Reset: N/A

Register : Address

| | |
|-----------------------------|-----------------------------|
| B0_P0_ROUTE_VS2: 0x400101E4 | B0_P1_ROUTE_VS2: 0x400103E4 |
| B0_P2_ROUTE_VS2: 0x400105E4 | B0_P3_ROUTE_VS2: 0x400107E4 |
| B0_P4_ROUTE_VS2: 0x400109E4 | B0_P5_ROUTE_VS2: 0x40010BE4 |
| B0_P6_ROUTE_VS2: 0x40010DE4 | B0_P7_ROUTE_VS2: 0x40010FE4 |
| B1_P2_ROUTE_VS2: 0x400115E4 | B1_P3_ROUTE_VS2: 0x400117E4 |
| B1_P4_ROUTE_VS2: 0x400119E4 | B1_P5_ROUTE_VS2: 0x40011BE4 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

UDB Channel VS Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration nibble for BOTTOM UDB vertical segmentation configuration |
| 3:0 | vs_top[3:0] | RAM configuration nibble for TOP UDB vertical segmentation configuration |

1.3.1229 B[0..3]_P[0..7]_ROUTE_VS3

VS3

Reset: N/A

Register : Address

| | |
|-----------------------------|-----------------------------|
| B0_P0_ROUTE_VS3: 0x400101E6 | B0_P1_ROUTE_VS3: 0x400103E6 |
| B0_P2_ROUTE_VS3: 0x400105E6 | B0_P3_ROUTE_VS3: 0x400107E6 |
| B0_P4_ROUTE_VS3: 0x400109E6 | B0_P5_ROUTE_VS3: 0x40010BE6 |
| B0_P6_ROUTE_VS3: 0x40010DE6 | B0_P7_ROUTE_VS3: 0x40010FE6 |
| B1_P2_ROUTE_VS3: 0x400115E6 | B1_P3_ROUTE_VS3: 0x400117E6 |
| B1_P4_ROUTE_VS3: 0x400119E6 | B1_P5_ROUTE_VS3: 0x40011BE6 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

UDB Channel VS Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration nibble for BOTTOM UDB vertical segmentation configuration |
| 3:0 | vs_top[3:0] | RAM configuration nibble for TOP UDB vertical segmentation configuration |

1.3.1230 B[0..3]_P[0..7]_ROUTE_VS4

VS4

Reset: N/A

Register : Address

| | |
|-----------------------------|-----------------------------|
| B0_P0_ROUTE_VS4: 0x400101E8 | B0_P1_ROUTE_VS4: 0x400103E8 |
| B0_P2_ROUTE_VS4: 0x400105E8 | B0_P3_ROUTE_VS4: 0x400107E8 |
| B0_P4_ROUTE_VS4: 0x400109E8 | B0_P5_ROUTE_VS4: 0x40010BE8 |
| B0_P6_ROUTE_VS4: 0x40010DE8 | B0_P7_ROUTE_VS4: 0x40010FE8 |
| B1_P2_ROUTE_VS4: 0x400115E8 | B1_P3_ROUTE_VS4: 0x400117E8 |
| B1_P4_ROUTE_VS4: 0x400119E8 | B1_P5_ROUTE_VS4: 0x40011BE8 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

UDB Channel VS Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration nibble for BOTTOM UDB vertical segmentation configuration |
| 3:0 | vs_top[3:0] | RAM configuration nibble for TOP UDB vertical segmentation configuration |

1.3.1231 B[0..3]_P[0..7]_ROUTE_VS5

VS5

Reset: N/A

Register : Address

| | |
|-----------------------------|-----------------------------|
| B0_P0_ROUTE_VS5: 0x400101EA | B0_P1_ROUTE_VS5: 0x400103EA |
| B0_P2_ROUTE_VS5: 0x400105EA | B0_P3_ROUTE_VS5: 0x400107EA |
| B0_P4_ROUTE_VS5: 0x400109EA | B0_P5_ROUTE_VS5: 0x40010BEA |
| B0_P6_ROUTE_VS5: 0x40010DEA | B0_P7_ROUTE_VS5: 0x40010FEA |
| B1_P2_ROUTE_VS5: 0x400115EA | B1_P3_ROUTE_VS5: 0x400117EA |
| B1_P4_ROUTE_VS5: 0x400119EA | B1_P5_ROUTE_VS5: 0x40011BEA |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

UDB Channel VS Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration nibble for BOTTOM UDB vertical segmentation configuration |
| 3:0 | vs_top[3:0] | RAM configuration nibble for TOP UDB vertical segmentation configuration |

1.3.1232 B[0..3]_P[0..7]_ROUTE_VS6

VS6

Reset: N/A

Register : Address

| | |
|-----------------------------|-----------------------------|
| B0_P0_ROUTE_VS6: 0x400101EC | B0_P1_ROUTE_VS6: 0x400103EC |
| B0_P2_ROUTE_VS6: 0x400105EC | B0_P3_ROUTE_VS6: 0x400107EC |
| B0_P4_ROUTE_VS6: 0x400109EC | B0_P5_ROUTE_VS6: 0x40010BEC |
| B0_P6_ROUTE_VS6: 0x40010DEC | B0_P7_ROUTE_VS6: 0x40010FEC |
| B1_P2_ROUTE_VS6: 0x400115EC | B1_P3_ROUTE_VS6: 0x400117EC |
| B1_P4_ROUTE_VS6: 0x400119EC | B1_P5_ROUTE_VS6: 0x40011BEC |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

UDB Channel VS Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration nibble for BOTTOM UDB vertical segmentation configuration |
| 3:0 | vs_top[3:0] | RAM configuration nibble for TOP UDB vertical segmentation configuration |

1.3.1233 B[0..3]_P[0..7]_ROUTE_VS7

VS7

Reset: N/A

Register : Address

| | |
|-----------------------------|-----------------------------|
| B0_P0_ROUTE_VS7: 0x400101EE | B0_P1_ROUTE_VS7: 0x400103EE |
| B0_P2_ROUTE_VS7: 0x400105EE | B0_P3_ROUTE_VS7: 0x400107EE |
| B0_P4_ROUTE_VS7: 0x400109EE | B0_P5_ROUTE_VS7: 0x40010BEE |
| B0_P6_ROUTE_VS7: 0x40010DEE | B0_P7_ROUTE_VS7: 0x40010FEE |
| B1_P2_ROUTE_VS7: 0x400115EE | B1_P3_ROUTE_VS7: 0x400117EE |
| B1_P4_ROUTE_VS7: 0x400119EE | B1_P5_ROUTE_VS7: 0x40011BEE |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

UDB Channel VS Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration nibble for BOTTOM UDB vertical segmentation configuration |
| 3:0 | vs_top[3:0] | RAM configuration nibble for TOP UDB vertical segmentation configuration |

1.3.1234 DSI[0..15]_HC[0..127]

HC

Reset: N/A

Register : Address

| | |
|-----------------------|-----------------------|
| DSI0_HC0: 0x40014000 | DSI0_HC1: 0x40014001 |
| DSI0_HC2: 0x40014002 | DSI0_HC3: 0x40014003 |
| DSI0_HC4: 0x40014004 | DSI0_HC5: 0x40014005 |
| DSI0_HC6: 0x40014006 | DSI0_HC7: 0x40014007 |
| DSI0_HC8: 0x40014008 | DSI0_HC9: 0x40014009 |
| DSI0_HC10: 0x4001400A | DSI0_HC11: 0x4001400B |
| DSI0_HC12: 0x4001400C | DSI0_HC13: 0x4001400D |
| DSI0_HC14: 0x4001400E | DSI0_HC15: 0x4001400F |
| DSI0_HC16: 0x40014010 | DSI0_HC17: 0x40014011 |
| DSI0_HC18: 0x40014012 | DSI0_HC19: 0x40014013 |
| DSI0_HC20: 0x40014014 | DSI0_HC21: 0x40014015 |
| DSI0_HC22: 0x40014016 | DSI0_HC23: 0x40014017 |
| DSI0_HC24: 0x40014018 | DSI0_HC25: 0x40014019 |
| DSI0_HC26: 0x4001401A | DSI0_HC27: 0x4001401B |
| DSI0_HC28: 0x4001401C | DSI0_HC29: 0x4001401D |
| DSI0_HC30: 0x4001401E | DSI0_HC31: 0x4001401F |
| DSI0_HC32: 0x40014020 | DSI0_HC33: 0x40014021 |
| DSI0_HC34: 0x40014022 | DSI0_HC35: 0x40014023 |
| DSI0_HC36: 0x40014024 | DSI0_HC37: 0x40014025 |
| DSI0_HC38: 0x40014026 | DSI0_HC39: 0x40014027 |
| DSI0_HC40: 0x40014028 | DSI0_HC41: 0x40014029 |
| DSI0_HC42: 0x4001402A | DSI0_HC43: 0x4001402B |
| DSI0_HC44: 0x4001402C | DSI0_HC45: 0x4001402D |
| DSI0_HC46: 0x4001402E | DSI0_HC47: 0x4001402F |
| DSI0_HC48: 0x40014030 | DSI0_HC49: 0x40014031 |
| DSI0_HC50: 0x40014032 | DSI0_HC51: 0x40014033 |
| DSI0_HC52: 0x40014034 | DSI0_HC53: 0x40014035 |
| DSI0_HC54: 0x40014036 | DSI0_HC55: 0x40014037 |
| DSI0_HC56: 0x40014038 | DSI0_HC57: 0x40014039 |
| DSI0_HC58: 0x4001403A | DSI0_HC59: 0x4001403B |
| DSI0_HC60: 0x4001403C | DSI0_HC61: 0x4001403D |
| DSI0_HC62: 0x4001403E | DSI0_HC63: 0x4001403F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI0_HC64: 0x40014040 | DSI0_HC65: 0x40014041 |
| DSI0_HC66: 0x40014042 | DSI0_HC67: 0x40014043 |
| DSI0_HC68: 0x40014044 | DSI0_HC69: 0x40014045 |
| DSI0_HC70: 0x40014046 | DSI0_HC71: 0x40014047 |
| DSI0_HC72: 0x40014048 | DSI0_HC73: 0x40014049 |
| DSI0_HC74: 0x4001404A | DSI0_HC75: 0x4001404B |
| DSI0_HC76: 0x4001404C | DSI0_HC77: 0x4001404D |
| DSI0_HC78: 0x4001404E | DSI0_HC79: 0x4001404F |
| DSI0_HC80: 0x40014050 | DSI0_HC81: 0x40014051 |
| DSI0_HC82: 0x40014052 | DSI0_HC83: 0x40014053 |
| DSI0_HC84: 0x40014054 | DSI0_HC85: 0x40014055 |
| DSI0_HC86: 0x40014056 | DSI0_HC87: 0x40014057 |
| DSI0_HC88: 0x40014058 | DSI0_HC89: 0x40014059 |
| DSI0_HC90: 0x4001405A | DSI0_HC91: 0x4001405B |
| DSI0_HC92: 0x4001405C | DSI0_HC93: 0x4001405D |
| DSI0_HC94: 0x4001405E | DSI0_HC95: 0x4001405F |
| DSI0_HC96: 0x40014060 | DSI0_HC97: 0x40014061 |
| DSI0_HC98: 0x40014062 | DSI0_HC99: 0x40014063 |
| DSI0_HC100: 0x40014064 | DSI0_HC101: 0x40014065 |
| DSI0_HC102: 0x40014066 | DSI0_HC103: 0x40014067 |
| DSI0_HC104: 0x40014068 | DSI0_HC105: 0x40014069 |
| DSI0_HC106: 0x4001406A | DSI0_HC107: 0x4001406B |
| DSI0_HC108: 0x4001406C | DSI0_HC109: 0x4001406D |
| DSI0_HC110: 0x4001406E | DSI0_HC111: 0x4001406F |
| DSI0_HC112: 0x40014070 | DSI0_HC113: 0x40014071 |
| DSI0_HC114: 0x40014072 | DSI0_HC115: 0x40014073 |
| DSI0_HC116: 0x40014074 | DSI0_HC117: 0x40014075 |
| DSI0_HC118: 0x40014076 | DSI0_HC119: 0x40014077 |
| DSI0_HC120: 0x40014078 | DSI0_HC121: 0x40014079 |
| DSI0_HC122: 0x4001407A | DSI0_HC123: 0x4001407B |
| DSI0_HC124: 0x4001407C | DSI0_HC125: 0x4001407D |
| DSI0_HC126: 0x4001407E | DSI0_HC127: 0x4001407F |
| DSI1_HC0: 0x40014100 | DSI1_HC1: 0x40014101 |
| DSI1_HC2: 0x40014102 | DSI1_HC3: 0x40014103 |
| DSI1_HC4: 0x40014104 | DSI1_HC5: 0x40014105 |
| DSI1_HC6: 0x40014106 | DSI1_HC7: 0x40014107 |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|-----------------------|-----------------------|
| DSI1_HC8: 0x40014108 | DSI1_HC9: 0x40014109 |
| DSI1_HC10: 0x4001410A | DSI1_HC11: 0x4001410B |
| DSI1_HC12: 0x4001410C | DSI1_HC13: 0x4001410D |
| DSI1_HC14: 0x4001410E | DSI1_HC15: 0x4001410F |
| DSI1_HC16: 0x40014110 | DSI1_HC17: 0x40014111 |
| DSI1_HC18: 0x40014112 | DSI1_HC19: 0x40014113 |
| DSI1_HC20: 0x40014114 | DSI1_HC21: 0x40014115 |
| DSI1_HC22: 0x40014116 | DSI1_HC23: 0x40014117 |
| DSI1_HC24: 0x40014118 | DSI1_HC25: 0x40014119 |
| DSI1_HC26: 0x4001411A | DSI1_HC27: 0x4001411B |
| DSI1_HC28: 0x4001411C | DSI1_HC29: 0x4001411D |
| DSI1_HC30: 0x4001411E | DSI1_HC31: 0x4001411F |
| DSI1_HC32: 0x40014120 | DSI1_HC33: 0x40014121 |
| DSI1_HC34: 0x40014122 | DSI1_HC35: 0x40014123 |
| DSI1_HC36: 0x40014124 | DSI1_HC37: 0x40014125 |
| DSI1_HC38: 0x40014126 | DSI1_HC39: 0x40014127 |
| DSI1_HC40: 0x40014128 | DSI1_HC41: 0x40014129 |
| DSI1_HC42: 0x4001412A | DSI1_HC43: 0x4001412B |
| DSI1_HC44: 0x4001412C | DSI1_HC45: 0x4001412D |
| DSI1_HC46: 0x4001412E | DSI1_HC47: 0x4001412F |
| DSI1_HC48: 0x40014130 | DSI1_HC49: 0x40014131 |
| DSI1_HC50: 0x40014132 | DSI1_HC51: 0x40014133 |
| DSI1_HC52: 0x40014134 | DSI1_HC53: 0x40014135 |
| DSI1_HC54: 0x40014136 | DSI1_HC55: 0x40014137 |
| DSI1_HC56: 0x40014138 | DSI1_HC57: 0x40014139 |
| DSI1_HC58: 0x4001413A | DSI1_HC59: 0x4001413B |
| DSI1_HC60: 0x4001413C | DSI1_HC61: 0x4001413D |
| DSI1_HC62: 0x4001413E | DSI1_HC63: 0x4001413F |
| DSI1_HC64: 0x40014140 | DSI1_HC65: 0x40014141 |
| DSI1_HC66: 0x40014142 | DSI1_HC67: 0x40014143 |
| DSI1_HC68: 0x40014144 | DSI1_HC69: 0x40014145 |
| DSI1_HC70: 0x40014146 | DSI1_HC71: 0x40014147 |
| DSI1_HC72: 0x40014148 | DSI1_HC73: 0x40014149 |
| DSI1_HC74: 0x4001414A | DSI1_HC75: 0x4001414B |
| DSI1_HC76: 0x4001414C | DSI1_HC77: 0x4001414D |
| DSI1_HC78: 0x4001414E | DSI1_HC79: 0x4001414F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI1_HC80: 0x40014150 | DSI1_HC81: 0x40014151 |
| DSI1_HC82: 0x40014152 | DSI1_HC83: 0x40014153 |
| DSI1_HC84: 0x40014154 | DSI1_HC85: 0x40014155 |
| DSI1_HC86: 0x40014156 | DSI1_HC87: 0x40014157 |
| DSI1_HC88: 0x40014158 | DSI1_HC89: 0x40014159 |
| DSI1_HC90: 0x4001415A | DSI1_HC91: 0x4001415B |
| DSI1_HC92: 0x4001415C | DSI1_HC93: 0x4001415D |
| DSI1_HC94: 0x4001415E | DSI1_HC95: 0x4001415F |
| DSI1_HC96: 0x40014160 | DSI1_HC97: 0x40014161 |
| DSI1_HC98: 0x40014162 | DSI1_HC99: 0x40014163 |
| DSI1_HC100: 0x40014164 | DSI1_HC101: 0x40014165 |
| DSI1_HC102: 0x40014166 | DSI1_HC103: 0x40014167 |
| DSI1_HC104: 0x40014168 | DSI1_HC105: 0x40014169 |
| DSI1_HC106: 0x4001416A | DSI1_HC107: 0x4001416B |
| DSI1_HC108: 0x4001416C | DSI1_HC109: 0x4001416D |
| DSI1_HC110: 0x4001416E | DSI1_HC111: 0x4001416F |
| DSI1_HC112: 0x40014170 | DSI1_HC113: 0x40014171 |
| DSI1_HC114: 0x40014172 | DSI1_HC115: 0x40014173 |
| DSI1_HC116: 0x40014174 | DSI1_HC117: 0x40014175 |
| DSI1_HC118: 0x40014176 | DSI1_HC119: 0x40014177 |
| DSI1_HC120: 0x40014178 | DSI1_HC121: 0x40014179 |
| DSI1_HC122: 0x4001417A | DSI1_HC123: 0x4001417B |
| DSI1_HC124: 0x4001417C | DSI1_HC125: 0x4001417D |
| DSI1_HC126: 0x4001417E | DSI1_HC127: 0x4001417F |
| DSI2_HC0: 0x40014200 | DSI2_HC1: 0x40014201 |
| DSI2_HC2: 0x40014202 | DSI2_HC3: 0x40014203 |
| DSI2_HC4: 0x40014204 | DSI2_HC5: 0x40014205 |
| DSI2_HC6: 0x40014206 | DSI2_HC7: 0x40014207 |
| DSI2_HC8: 0x40014208 | DSI2_HC9: 0x40014209 |
| DSI2_HC10: 0x4001420A | DSI2_HC11: 0x4001420B |
| DSI2_HC12: 0x4001420C | DSI2_HC13: 0x4001420D |
| DSI2_HC14: 0x4001420E | DSI2_HC15: 0x4001420F |
| DSI2_HC16: 0x40014210 | DSI2_HC17: 0x40014211 |
| DSI2_HC18: 0x40014212 | DSI2_HC19: 0x40014213 |
| DSI2_HC20: 0x40014214 | DSI2_HC21: 0x40014215 |
| DSI2_HC22: 0x40014216 | DSI2_HC23: 0x40014217 |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|-----------------------|-----------------------|
| DSI2_HC24: 0x40014218 | DSI2_HC25: 0x40014219 |
| DSI2_HC26: 0x4001421A | DSI2_HC27: 0x4001421B |
| DSI2_HC28: 0x4001421C | DSI2_HC29: 0x4001421D |
| DSI2_HC30: 0x4001421E | DSI2_HC31: 0x4001421F |
| DSI2_HC32: 0x40014220 | DSI2_HC33: 0x40014221 |
| DSI2_HC34: 0x40014222 | DSI2_HC35: 0x40014223 |
| DSI2_HC36: 0x40014224 | DSI2_HC37: 0x40014225 |
| DSI2_HC38: 0x40014226 | DSI2_HC39: 0x40014227 |
| DSI2_HC40: 0x40014228 | DSI2_HC41: 0x40014229 |
| DSI2_HC42: 0x4001422A | DSI2_HC43: 0x4001422B |
| DSI2_HC44: 0x4001422C | DSI2_HC45: 0x4001422D |
| DSI2_HC46: 0x4001422E | DSI2_HC47: 0x4001422F |
| DSI2_HC48: 0x40014230 | DSI2_HC49: 0x40014231 |
| DSI2_HC50: 0x40014232 | DSI2_HC51: 0x40014233 |
| DSI2_HC52: 0x40014234 | DSI2_HC53: 0x40014235 |
| DSI2_HC54: 0x40014236 | DSI2_HC55: 0x40014237 |
| DSI2_HC56: 0x40014238 | DSI2_HC57: 0x40014239 |
| DSI2_HC58: 0x4001423A | DSI2_HC59: 0x4001423B |
| DSI2_HC60: 0x4001423C | DSI2_HC61: 0x4001423D |
| DSI2_HC62: 0x4001423E | DSI2_HC63: 0x4001423F |
| DSI2_HC64: 0x40014240 | DSI2_HC65: 0x40014241 |
| DSI2_HC66: 0x40014242 | DSI2_HC67: 0x40014243 |
| DSI2_HC68: 0x40014244 | DSI2_HC69: 0x40014245 |
| DSI2_HC70: 0x40014246 | DSI2_HC71: 0x40014247 |
| DSI2_HC72: 0x40014248 | DSI2_HC73: 0x40014249 |
| DSI2_HC74: 0x4001424A | DSI2_HC75: 0x4001424B |
| DSI2_HC76: 0x4001424C | DSI2_HC77: 0x4001424D |
| DSI2_HC78: 0x4001424E | DSI2_HC79: 0x4001424F |
| DSI2_HC80: 0x40014250 | DSI2_HC81: 0x40014251 |
| DSI2_HC82: 0x40014252 | DSI2_HC83: 0x40014253 |
| DSI2_HC84: 0x40014254 | DSI2_HC85: 0x40014255 |
| DSI2_HC86: 0x40014256 | DSI2_HC87: 0x40014257 |
| DSI2_HC88: 0x40014258 | DSI2_HC89: 0x40014259 |
| DSI2_HC90: 0x4001425A | DSI2_HC91: 0x4001425B |
| DSI2_HC92: 0x4001425C | DSI2_HC93: 0x4001425D |
| DSI2_HC94: 0x4001425E | DSI2_HC95: 0x4001425F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI2_HC96: 0x40014260 | DSI2_HC97: 0x40014261 |
| DSI2_HC98: 0x40014262 | DSI2_HC99: 0x40014263 |
| DSI2_HC100: 0x40014264 | DSI2_HC101: 0x40014265 |
| DSI2_HC102: 0x40014266 | DSI2_HC103: 0x40014267 |
| DSI2_HC104: 0x40014268 | DSI2_HC105: 0x40014269 |
| DSI2_HC106: 0x4001426A | DSI2_HC107: 0x4001426B |
| DSI2_HC108: 0x4001426C | DSI2_HC109: 0x4001426D |
| DSI2_HC110: 0x4001426E | DSI2_HC111: 0x4001426F |
| DSI2_HC112: 0x40014270 | DSI2_HC113: 0x40014271 |
| DSI2_HC114: 0x40014272 | DSI2_HC115: 0x40014273 |
| DSI2_HC116: 0x40014274 | DSI2_HC117: 0x40014275 |
| DSI2_HC118: 0x40014276 | DSI2_HC119: 0x40014277 |
| DSI2_HC120: 0x40014278 | DSI2_HC121: 0x40014279 |
| DSI2_HC122: 0x4001427A | DSI2_HC123: 0x4001427B |
| DSI2_HC124: 0x4001427C | DSI2_HC125: 0x4001427D |
| DSI2_HC126: 0x4001427E | DSI2_HC127: 0x4001427F |
| DSI3_HC0: 0x40014300 | DSI3_HC1: 0x40014301 |
| DSI3_HC2: 0x40014302 | DSI3_HC3: 0x40014303 |
| DSI3_HC4: 0x40014304 | DSI3_HC5: 0x40014305 |
| DSI3_HC6: 0x40014306 | DSI3_HC7: 0x40014307 |
| DSI3_HC8: 0x40014308 | DSI3_HC9: 0x40014309 |
| DSI3_HC10: 0x4001430A | DSI3_HC11: 0x4001430B |
| DSI3_HC12: 0x4001430C | DSI3_HC13: 0x4001430D |
| DSI3_HC14: 0x4001430E | DSI3_HC15: 0x4001430F |
| DSI3_HC16: 0x40014310 | DSI3_HC17: 0x40014311 |
| DSI3_HC18: 0x40014312 | DSI3_HC19: 0x40014313 |
| DSI3_HC20: 0x40014314 | DSI3_HC21: 0x40014315 |
| DSI3_HC22: 0x40014316 | DSI3_HC23: 0x40014317 |
| DSI3_HC24: 0x40014318 | DSI3_HC25: 0x40014319 |
| DSI3_HC26: 0x4001431A | DSI3_HC27: 0x4001431B |
| DSI3_HC28: 0x4001431C | DSI3_HC29: 0x4001431D |
| DSI3_HC30: 0x4001431E | DSI3_HC31: 0x4001431F |
| DSI3_HC32: 0x40014320 | DSI3_HC33: 0x40014321 |
| DSI3_HC34: 0x40014322 | DSI3_HC35: 0x40014323 |
| DSI3_HC36: 0x40014324 | DSI3_HC37: 0x40014325 |
| DSI3_HC38: 0x40014326 | DSI3_HC39: 0x40014327 |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI3_HC40: 0x40014328 | DSI3_HC41: 0x40014329 |
| DSI3_HC42: 0x4001432A | DSI3_HC43: 0x4001432B |
| DSI3_HC44: 0x4001432C | DSI3_HC45: 0x4001432D |
| DSI3_HC46: 0x4001432E | DSI3_HC47: 0x4001432F |
| DSI3_HC48: 0x40014330 | DSI3_HC49: 0x40014331 |
| DSI3_HC50: 0x40014332 | DSI3_HC51: 0x40014333 |
| DSI3_HC52: 0x40014334 | DSI3_HC53: 0x40014335 |
| DSI3_HC54: 0x40014336 | DSI3_HC55: 0x40014337 |
| DSI3_HC56: 0x40014338 | DSI3_HC57: 0x40014339 |
| DSI3_HC58: 0x4001433A | DSI3_HC59: 0x4001433B |
| DSI3_HC60: 0x4001433C | DSI3_HC61: 0x4001433D |
| DSI3_HC62: 0x4001433E | DSI3_HC63: 0x4001433F |
| DSI3_HC64: 0x40014340 | DSI3_HC65: 0x40014341 |
| DSI3_HC66: 0x40014342 | DSI3_HC67: 0x40014343 |
| DSI3_HC68: 0x40014344 | DSI3_HC69: 0x40014345 |
| DSI3_HC70: 0x40014346 | DSI3_HC71: 0x40014347 |
| DSI3_HC72: 0x40014348 | DSI3_HC73: 0x40014349 |
| DSI3_HC74: 0x4001434A | DSI3_HC75: 0x4001434B |
| DSI3_HC76: 0x4001434C | DSI3_HC77: 0x4001434D |
| DSI3_HC78: 0x4001434E | DSI3_HC79: 0x4001434F |
| DSI3_HC80: 0x40014350 | DSI3_HC81: 0x40014351 |
| DSI3_HC82: 0x40014352 | DSI3_HC83: 0x40014353 |
| DSI3_HC84: 0x40014354 | DSI3_HC85: 0x40014355 |
| DSI3_HC86: 0x40014356 | DSI3_HC87: 0x40014357 |
| DSI3_HC88: 0x40014358 | DSI3_HC89: 0x40014359 |
| DSI3_HC90: 0x4001435A | DSI3_HC91: 0x4001435B |
| DSI3_HC92: 0x4001435C | DSI3_HC93: 0x4001435D |
| DSI3_HC94: 0x4001435E | DSI3_HC95: 0x4001435F |
| DSI3_HC96: 0x40014360 | DSI3_HC97: 0x40014361 |
| DSI3_HC98: 0x40014362 | DSI3_HC99: 0x40014363 |
| DSI3_HC100: 0x40014364 | DSI3_HC101: 0x40014365 |
| DSI3_HC102: 0x40014366 | DSI3_HC103: 0x40014367 |
| DSI3_HC104: 0x40014368 | DSI3_HC105: 0x40014369 |
| DSI3_HC106: 0x4001436A | DSI3_HC107: 0x4001436B |
| DSI3_HC108: 0x4001436C | DSI3_HC109: 0x4001436D |
| DSI3_HC110: 0x4001436E | DSI3_HC111: 0x4001436F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI3_HC112: 0x40014370 | DSI3_HC113: 0x40014371 |
| DSI3_HC114: 0x40014372 | DSI3_HC115: 0x40014373 |
| DSI3_HC116: 0x40014374 | DSI3_HC117: 0x40014375 |
| DSI3_HC118: 0x40014376 | DSI3_HC119: 0x40014377 |
| DSI3_HC120: 0x40014378 | DSI3_HC121: 0x40014379 |
| DSI3_HC122: 0x4001437A | DSI3_HC123: 0x4001437B |
| DSI3_HC124: 0x4001437C | DSI3_HC125: 0x4001437D |
| DSI3_HC126: 0x4001437E | DSI3_HC127: 0x4001437F |
| DSI4_HC0: 0x40014400 | DSI4_HC1: 0x40014401 |
| DSI4_HC2: 0x40014402 | DSI4_HC3: 0x40014403 |
| DSI4_HC4: 0x40014404 | DSI4_HC5: 0x40014405 |
| DSI4_HC6: 0x40014406 | DSI4_HC7: 0x40014407 |
| DSI4_HC8: 0x40014408 | DSI4_HC9: 0x40014409 |
| DSI4_HC10: 0x4001440A | DSI4_HC11: 0x4001440B |
| DSI4_HC12: 0x4001440C | DSI4_HC13: 0x4001440D |
| DSI4_HC14: 0x4001440E | DSI4_HC15: 0x4001440F |
| DSI4_HC16: 0x40014410 | DSI4_HC17: 0x40014411 |
| DSI4_HC18: 0x40014412 | DSI4_HC19: 0x40014413 |
| DSI4_HC20: 0x40014414 | DSI4_HC21: 0x40014415 |
| DSI4_HC22: 0x40014416 | DSI4_HC23: 0x40014417 |
| DSI4_HC24: 0x40014418 | DSI4_HC25: 0x40014419 |
| DSI4_HC26: 0x4001441A | DSI4_HC27: 0x4001441B |
| DSI4_HC28: 0x4001441C | DSI4_HC29: 0x4001441D |
| DSI4_HC30: 0x4001441E | DSI4_HC31: 0x4001441F |
| DSI4_HC32: 0x40014420 | DSI4_HC33: 0x40014421 |
| DSI4_HC34: 0x40014422 | DSI4_HC35: 0x40014423 |
| DSI4_HC36: 0x40014424 | DSI4_HC37: 0x40014425 |
| DSI4_HC38: 0x40014426 | DSI4_HC39: 0x40014427 |
| DSI4_HC40: 0x40014428 | DSI4_HC41: 0x40014429 |
| DSI4_HC42: 0x4001442A | DSI4_HC43: 0x4001442B |
| DSI4_HC44: 0x4001442C | DSI4_HC45: 0x4001442D |
| DSI4_HC46: 0x4001442E | DSI4_HC47: 0x4001442F |
| DSI4_HC48: 0x40014430 | DSI4_HC49: 0x40014431 |
| DSI4_HC50: 0x40014432 | DSI4_HC51: 0x40014433 |
| DSI4_HC52: 0x40014434 | DSI4_HC53: 0x40014435 |
| DSI4_HC54: 0x40014436 | DSI4_HC55: 0x40014437 |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI4_HC56: 0x40014438 | DSI4_HC57: 0x40014439 |
| DSI4_HC58: 0x4001443A | DSI4_HC59: 0x4001443B |
| DSI4_HC60: 0x4001443C | DSI4_HC61: 0x4001443D |
| DSI4_HC62: 0x4001443E | DSI4_HC63: 0x4001443F |
| DSI4_HC64: 0x40014440 | DSI4_HC65: 0x40014441 |
| DSI4_HC66: 0x40014442 | DSI4_HC67: 0x40014443 |
| DSI4_HC68: 0x40014444 | DSI4_HC69: 0x40014445 |
| DSI4_HC70: 0x40014446 | DSI4_HC71: 0x40014447 |
| DSI4_HC72: 0x40014448 | DSI4_HC73: 0x40014449 |
| DSI4_HC74: 0x4001444A | DSI4_HC75: 0x4001444B |
| DSI4_HC76: 0x4001444C | DSI4_HC77: 0x4001444D |
| DSI4_HC78: 0x4001444E | DSI4_HC79: 0x4001444F |
| DSI4_HC80: 0x40014450 | DSI4_HC81: 0x40014451 |
| DSI4_HC82: 0x40014452 | DSI4_HC83: 0x40014453 |
| DSI4_HC84: 0x40014454 | DSI4_HC85: 0x40014455 |
| DSI4_HC86: 0x40014456 | DSI4_HC87: 0x40014457 |
| DSI4_HC88: 0x40014458 | DSI4_HC89: 0x40014459 |
| DSI4_HC90: 0x4001445A | DSI4_HC91: 0x4001445B |
| DSI4_HC92: 0x4001445C | DSI4_HC93: 0x4001445D |
| DSI4_HC94: 0x4001445E | DSI4_HC95: 0x4001445F |
| DSI4_HC96: 0x40014460 | DSI4_HC97: 0x40014461 |
| DSI4_HC98: 0x40014462 | DSI4_HC99: 0x40014463 |
| DSI4_HC100: 0x40014464 | DSI4_HC101: 0x40014465 |
| DSI4_HC102: 0x40014466 | DSI4_HC103: 0x40014467 |
| DSI4_HC104: 0x40014468 | DSI4_HC105: 0x40014469 |
| DSI4_HC106: 0x4001446A | DSI4_HC107: 0x4001446B |
| DSI4_HC108: 0x4001446C | DSI4_HC109: 0x4001446D |
| DSI4_HC110: 0x4001446E | DSI4_HC111: 0x4001446F |
| DSI4_HC112: 0x40014470 | DSI4_HC113: 0x40014471 |
| DSI4_HC114: 0x40014472 | DSI4_HC115: 0x40014473 |
| DSI4_HC116: 0x40014474 | DSI4_HC117: 0x40014475 |
| DSI4_HC118: 0x40014476 | DSI4_HC119: 0x40014477 |
| DSI4_HC120: 0x40014478 | DSI4_HC121: 0x40014479 |
| DSI4_HC122: 0x4001447A | DSI4_HC123: 0x4001447B |
| DSI4_HC124: 0x4001447C | DSI4_HC125: 0x4001447D |
| DSI4_HC126: 0x4001447E | DSI4_HC127: 0x4001447F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|-----------------------|-----------------------|
| DSI5_HC0: 0x40014500 | DSI5_HC1: 0x40014501 |
| DSI5_HC2: 0x40014502 | DSI5_HC3: 0x40014503 |
| DSI5_HC4: 0x40014504 | DSI5_HC5: 0x40014505 |
| DSI5_HC6: 0x40014506 | DSI5_HC7: 0x40014507 |
| DSI5_HC8: 0x40014508 | DSI5_HC9: 0x40014509 |
| DSI5_HC10: 0x4001450A | DSI5_HC11: 0x4001450B |
| DSI5_HC12: 0x4001450C | DSI5_HC13: 0x4001450D |
| DSI5_HC14: 0x4001450E | DSI5_HC15: 0x4001450F |
| DSI5_HC16: 0x40014510 | DSI5_HC17: 0x40014511 |
| DSI5_HC18: 0x40014512 | DSI5_HC19: 0x40014513 |
| DSI5_HC20: 0x40014514 | DSI5_HC21: 0x40014515 |
| DSI5_HC22: 0x40014516 | DSI5_HC23: 0x40014517 |
| DSI5_HC24: 0x40014518 | DSI5_HC25: 0x40014519 |
| DSI5_HC26: 0x4001451A | DSI5_HC27: 0x4001451B |
| DSI5_HC28: 0x4001451C | DSI5_HC29: 0x4001451D |
| DSI5_HC30: 0x4001451E | DSI5_HC31: 0x4001451F |
| DSI5_HC32: 0x40014520 | DSI5_HC33: 0x40014521 |
| DSI5_HC34: 0x40014522 | DSI5_HC35: 0x40014523 |
| DSI5_HC36: 0x40014524 | DSI5_HC37: 0x40014525 |
| DSI5_HC38: 0x40014526 | DSI5_HC39: 0x40014527 |
| DSI5_HC40: 0x40014528 | DSI5_HC41: 0x40014529 |
| DSI5_HC42: 0x4001452A | DSI5_HC43: 0x4001452B |
| DSI5_HC44: 0x4001452C | DSI5_HC45: 0x4001452D |
| DSI5_HC46: 0x4001452E | DSI5_HC47: 0x4001452F |
| DSI5_HC48: 0x40014530 | DSI5_HC49: 0x40014531 |
| DSI5_HC50: 0x40014532 | DSI5_HC51: 0x40014533 |
| DSI5_HC52: 0x40014534 | DSI5_HC53: 0x40014535 |
| DSI5_HC54: 0x40014536 | DSI5_HC55: 0x40014537 |
| DSI5_HC56: 0x40014538 | DSI5_HC57: 0x40014539 |
| DSI5_HC58: 0x4001453A | DSI5_HC59: 0x4001453B |
| DSI5_HC60: 0x4001453C | DSI5_HC61: 0x4001453D |
| DSI5_HC62: 0x4001453E | DSI5_HC63: 0x4001453F |
| DSI5_HC64: 0x40014540 | DSI5_HC65: 0x40014541 |
| DSI5_HC66: 0x40014542 | DSI5_HC67: 0x40014543 |
| DSI5_HC68: 0x40014544 | DSI5_HC69: 0x40014545 |
| DSI5_HC70: 0x40014546 | DSI5_HC71: 0x40014547 |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI5_HC72: 0x40014548 | DSI5_HC73: 0x40014549 |
| DSI5_HC74: 0x4001454A | DSI5_HC75: 0x4001454B |
| DSI5_HC76: 0x4001454C | DSI5_HC77: 0x4001454D |
| DSI5_HC78: 0x4001454E | DSI5_HC79: 0x4001454F |
| DSI5_HC80: 0x40014550 | DSI5_HC81: 0x40014551 |
| DSI5_HC82: 0x40014552 | DSI5_HC83: 0x40014553 |
| DSI5_HC84: 0x40014554 | DSI5_HC85: 0x40014555 |
| DSI5_HC86: 0x40014556 | DSI5_HC87: 0x40014557 |
| DSI5_HC88: 0x40014558 | DSI5_HC89: 0x40014559 |
| DSI5_HC90: 0x4001455A | DSI5_HC91: 0x4001455B |
| DSI5_HC92: 0x4001455C | DSI5_HC93: 0x4001455D |
| DSI5_HC94: 0x4001455E | DSI5_HC95: 0x4001455F |
| DSI5_HC96: 0x40014560 | DSI5_HC97: 0x40014561 |
| DSI5_HC98: 0x40014562 | DSI5_HC99: 0x40014563 |
| DSI5_HC100: 0x40014564 | DSI5_HC101: 0x40014565 |
| DSI5_HC102: 0x40014566 | DSI5_HC103: 0x40014567 |
| DSI5_HC104: 0x40014568 | DSI5_HC105: 0x40014569 |
| DSI5_HC106: 0x4001456A | DSI5_HC107: 0x4001456B |
| DSI5_HC108: 0x4001456C | DSI5_HC109: 0x4001456D |
| DSI5_HC110: 0x4001456E | DSI5_HC111: 0x4001456F |
| DSI5_HC112: 0x40014570 | DSI5_HC113: 0x40014571 |
| DSI5_HC114: 0x40014572 | DSI5_HC115: 0x40014573 |
| DSI5_HC116: 0x40014574 | DSI5_HC117: 0x40014575 |
| DSI5_HC118: 0x40014576 | DSI5_HC119: 0x40014577 |
| DSI5_HC120: 0x40014578 | DSI5_HC121: 0x40014579 |
| DSI5_HC122: 0x4001457A | DSI5_HC123: 0x4001457B |
| DSI5_HC124: 0x4001457C | DSI5_HC125: 0x4001457D |
| DSI5_HC126: 0x4001457E | DSI5_HC127: 0x4001457F |
| DSI6_HC0: 0x40014600 | DSI6_HC1: 0x40014601 |
| DSI6_HC2: 0x40014602 | DSI6_HC3: 0x40014603 |
| DSI6_HC4: 0x40014604 | DSI6_HC5: 0x40014605 |
| DSI6_HC6: 0x40014606 | DSI6_HC7: 0x40014607 |
| DSI6_HC8: 0x40014608 | DSI6_HC9: 0x40014609 |
| DSI6_HC10: 0x4001460A | DSI6_HC11: 0x4001460B |
| DSI6_HC12: 0x4001460C | DSI6_HC13: 0x4001460D |
| DSI6_HC14: 0x4001460E | DSI6_HC15: 0x4001460F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|-----------------------|-----------------------|
| DSI6_HC16: 0x40014610 | DSI6_HC17: 0x40014611 |
| DSI6_HC18: 0x40014612 | DSI6_HC19: 0x40014613 |
| DSI6_HC20: 0x40014614 | DSI6_HC21: 0x40014615 |
| DSI6_HC22: 0x40014616 | DSI6_HC23: 0x40014617 |
| DSI6_HC24: 0x40014618 | DSI6_HC25: 0x40014619 |
| DSI6_HC26: 0x4001461A | DSI6_HC27: 0x4001461B |
| DSI6_HC28: 0x4001461C | DSI6_HC29: 0x4001461D |
| DSI6_HC30: 0x4001461E | DSI6_HC31: 0x4001461F |
| DSI6_HC32: 0x40014620 | DSI6_HC33: 0x40014621 |
| DSI6_HC34: 0x40014622 | DSI6_HC35: 0x40014623 |
| DSI6_HC36: 0x40014624 | DSI6_HC37: 0x40014625 |
| DSI6_HC38: 0x40014626 | DSI6_HC39: 0x40014627 |
| DSI6_HC40: 0x40014628 | DSI6_HC41: 0x40014629 |
| DSI6_HC42: 0x4001462A | DSI6_HC43: 0x4001462B |
| DSI6_HC44: 0x4001462C | DSI6_HC45: 0x4001462D |
| DSI6_HC46: 0x4001462E | DSI6_HC47: 0x4001462F |
| DSI6_HC48: 0x40014630 | DSI6_HC49: 0x40014631 |
| DSI6_HC50: 0x40014632 | DSI6_HC51: 0x40014633 |
| DSI6_HC52: 0x40014634 | DSI6_HC53: 0x40014635 |
| DSI6_HC54: 0x40014636 | DSI6_HC55: 0x40014637 |
| DSI6_HC56: 0x40014638 | DSI6_HC57: 0x40014639 |
| DSI6_HC58: 0x4001463A | DSI6_HC59: 0x4001463B |
| DSI6_HC60: 0x4001463C | DSI6_HC61: 0x4001463D |
| DSI6_HC62: 0x4001463E | DSI6_HC63: 0x4001463F |
| DSI6_HC64: 0x40014640 | DSI6_HC65: 0x40014641 |
| DSI6_HC66: 0x40014642 | DSI6_HC67: 0x40014643 |
| DSI6_HC68: 0x40014644 | DSI6_HC69: 0x40014645 |
| DSI6_HC70: 0x40014646 | DSI6_HC71: 0x40014647 |
| DSI6_HC72: 0x40014648 | DSI6_HC73: 0x40014649 |
| DSI6_HC74: 0x4001464A | DSI6_HC75: 0x4001464B |
| DSI6_HC76: 0x4001464C | DSI6_HC77: 0x4001464D |
| DSI6_HC78: 0x4001464E | DSI6_HC79: 0x4001464F |
| DSI6_HC80: 0x40014650 | DSI6_HC81: 0x40014651 |
| DSI6_HC82: 0x40014652 | DSI6_HC83: 0x40014653 |
| DSI6_HC84: 0x40014654 | DSI6_HC85: 0x40014655 |
| DSI6_HC86: 0x40014656 | DSI6_HC87: 0x40014657 |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI6_HC88: 0x40014658 | DSI6_HC89: 0x40014659 |
| DSI6_HC90: 0x4001465A | DSI6_HC91: 0x4001465B |
| DSI6_HC92: 0x4001465C | DSI6_HC93: 0x4001465D |
| DSI6_HC94: 0x4001465E | DSI6_HC95: 0x4001465F |
| DSI6_HC96: 0x40014660 | DSI6_HC97: 0x40014661 |
| DSI6_HC98: 0x40014662 | DSI6_HC99: 0x40014663 |
| DSI6_HC100: 0x40014664 | DSI6_HC101: 0x40014665 |
| DSI6_HC102: 0x40014666 | DSI6_HC103: 0x40014667 |
| DSI6_HC104: 0x40014668 | DSI6_HC105: 0x40014669 |
| DSI6_HC106: 0x4001466A | DSI6_HC107: 0x4001466B |
| DSI6_HC108: 0x4001466C | DSI6_HC109: 0x4001466D |
| DSI6_HC110: 0x4001466E | DSI6_HC111: 0x4001466F |
| DSI6_HC112: 0x40014670 | DSI6_HC113: 0x40014671 |
| DSI6_HC114: 0x40014672 | DSI6_HC115: 0x40014673 |
| DSI6_HC116: 0x40014674 | DSI6_HC117: 0x40014675 |
| DSI6_HC118: 0x40014676 | DSI6_HC119: 0x40014677 |
| DSI6_HC120: 0x40014678 | DSI6_HC121: 0x40014679 |
| DSI6_HC122: 0x4001467A | DSI6_HC123: 0x4001467B |
| DSI6_HC124: 0x4001467C | DSI6_HC125: 0x4001467D |
| DSI6_HC126: 0x4001467E | DSI6_HC127: 0x4001467F |
| DSI7_HC0: 0x40014700 | DSI7_HC1: 0x40014701 |
| DSI7_HC2: 0x40014702 | DSI7_HC3: 0x40014703 |
| DSI7_HC4: 0x40014704 | DSI7_HC5: 0x40014705 |
| DSI7_HC6: 0x40014706 | DSI7_HC7: 0x40014707 |
| DSI7_HC8: 0x40014708 | DSI7_HC9: 0x40014709 |
| DSI7_HC10: 0x4001470A | DSI7_HC11: 0x4001470B |
| DSI7_HC12: 0x4001470C | DSI7_HC13: 0x4001470D |
| DSI7_HC14: 0x4001470E | DSI7_HC15: 0x4001470F |
| DSI7_HC16: 0x40014710 | DSI7_HC17: 0x40014711 |
| DSI7_HC18: 0x40014712 | DSI7_HC19: 0x40014713 |
| DSI7_HC20: 0x40014714 | DSI7_HC21: 0x40014715 |
| DSI7_HC22: 0x40014716 | DSI7_HC23: 0x40014717 |
| DSI7_HC24: 0x40014718 | DSI7_HC25: 0x40014719 |
| DSI7_HC26: 0x4001471A | DSI7_HC27: 0x4001471B |
| DSI7_HC28: 0x4001471C | DSI7_HC29: 0x4001471D |
| DSI7_HC30: 0x4001471E | DSI7_HC31: 0x4001471F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI7_HC32: 0x40014720 | DSI7_HC33: 0x40014721 |
| DSI7_HC34: 0x40014722 | DSI7_HC35: 0x40014723 |
| DSI7_HC36: 0x40014724 | DSI7_HC37: 0x40014725 |
| DSI7_HC38: 0x40014726 | DSI7_HC39: 0x40014727 |
| DSI7_HC40: 0x40014728 | DSI7_HC41: 0x40014729 |
| DSI7_HC42: 0x4001472A | DSI7_HC43: 0x4001472B |
| DSI7_HC44: 0x4001472C | DSI7_HC45: 0x4001472D |
| DSI7_HC46: 0x4001472E | DSI7_HC47: 0x4001472F |
| DSI7_HC48: 0x40014730 | DSI7_HC49: 0x40014731 |
| DSI7_HC50: 0x40014732 | DSI7_HC51: 0x40014733 |
| DSI7_HC52: 0x40014734 | DSI7_HC53: 0x40014735 |
| DSI7_HC54: 0x40014736 | DSI7_HC55: 0x40014737 |
| DSI7_HC56: 0x40014738 | DSI7_HC57: 0x40014739 |
| DSI7_HC58: 0x4001473A | DSI7_HC59: 0x4001473B |
| DSI7_HC60: 0x4001473C | DSI7_HC61: 0x4001473D |
| DSI7_HC62: 0x4001473E | DSI7_HC63: 0x4001473F |
| DSI7_HC64: 0x40014740 | DSI7_HC65: 0x40014741 |
| DSI7_HC66: 0x40014742 | DSI7_HC67: 0x40014743 |
| DSI7_HC68: 0x40014744 | DSI7_HC69: 0x40014745 |
| DSI7_HC70: 0x40014746 | DSI7_HC71: 0x40014747 |
| DSI7_HC72: 0x40014748 | DSI7_HC73: 0x40014749 |
| DSI7_HC74: 0x4001474A | DSI7_HC75: 0x4001474B |
| DSI7_HC76: 0x4001474C | DSI7_HC77: 0x4001474D |
| DSI7_HC78: 0x4001474E | DSI7_HC79: 0x4001474F |
| DSI7_HC80: 0x40014750 | DSI7_HC81: 0x40014751 |
| DSI7_HC82: 0x40014752 | DSI7_HC83: 0x40014753 |
| DSI7_HC84: 0x40014754 | DSI7_HC85: 0x40014755 |
| DSI7_HC86: 0x40014756 | DSI7_HC87: 0x40014757 |
| DSI7_HC88: 0x40014758 | DSI7_HC89: 0x40014759 |
| DSI7_HC90: 0x4001475A | DSI7_HC91: 0x4001475B |
| DSI7_HC92: 0x4001475C | DSI7_HC93: 0x4001475D |
| DSI7_HC94: 0x4001475E | DSI7_HC95: 0x4001475F |
| DSI7_HC96: 0x40014760 | DSI7_HC97: 0x40014761 |
| DSI7_HC98: 0x40014762 | DSI7_HC99: 0x40014763 |
| DSI7_HC100: 0x40014764 | DSI7_HC101: 0x40014765 |
| DSI7_HC102: 0x40014766 | DSI7_HC103: 0x40014767 |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI7_HC104: 0x40014768 | DSI7_HC105: 0x40014769 |
| DSI7_HC106: 0x4001476A | DSI7_HC107: 0x4001476B |
| DSI7_HC108: 0x4001476C | DSI7_HC109: 0x4001476D |
| DSI7_HC110: 0x4001476E | DSI7_HC111: 0x4001476F |
| DSI7_HC112: 0x40014770 | DSI7_HC113: 0x40014771 |
| DSI7_HC114: 0x40014772 | DSI7_HC115: 0x40014773 |
| DSI7_HC116: 0x40014774 | DSI7_HC117: 0x40014775 |
| DSI7_HC118: 0x40014776 | DSI7_HC119: 0x40014777 |
| DSI7_HC120: 0x40014778 | DSI7_HC121: 0x40014779 |
| DSI7_HC122: 0x4001477A | DSI7_HC123: 0x4001477B |
| DSI7_HC124: 0x4001477C | DSI7_HC125: 0x4001477D |
| DSI7_HC126: 0x4001477E | DSI7_HC127: 0x4001477F |
| DSI8_HC0: 0x40014800 | DSI8_HC1: 0x40014801 |
| DSI8_HC2: 0x40014802 | DSI8_HC3: 0x40014803 |
| DSI8_HC4: 0x40014804 | DSI8_HC5: 0x40014805 |
| DSI8_HC6: 0x40014806 | DSI8_HC7: 0x40014807 |
| DSI8_HC8: 0x40014808 | DSI8_HC9: 0x40014809 |
| DSI8_HC10: 0x4001480A | DSI8_HC11: 0x4001480B |
| DSI8_HC12: 0x4001480C | DSI8_HC13: 0x4001480D |
| DSI8_HC14: 0x4001480E | DSI8_HC15: 0x4001480F |
| DSI8_HC16: 0x40014810 | DSI8_HC17: 0x40014811 |
| DSI8_HC18: 0x40014812 | DSI8_HC19: 0x40014813 |
| DSI8_HC20: 0x40014814 | DSI8_HC21: 0x40014815 |
| DSI8_HC22: 0x40014816 | DSI8_HC23: 0x40014817 |
| DSI8_HC24: 0x40014818 | DSI8_HC25: 0x40014819 |
| DSI8_HC26: 0x4001481A | DSI8_HC27: 0x4001481B |
| DSI8_HC28: 0x4001481C | DSI8_HC29: 0x4001481D |
| DSI8_HC30: 0x4001481E | DSI8_HC31: 0x4001481F |
| DSI8_HC32: 0x40014820 | DSI8_HC33: 0x40014821 |
| DSI8_HC34: 0x40014822 | DSI8_HC35: 0x40014823 |
| DSI8_HC36: 0x40014824 | DSI8_HC37: 0x40014825 |
| DSI8_HC38: 0x40014826 | DSI8_HC39: 0x40014827 |
| DSI8_HC40: 0x40014828 | DSI8_HC41: 0x40014829 |
| DSI8_HC42: 0x4001482A | DSI8_HC43: 0x4001482B |
| DSI8_HC44: 0x4001482C | DSI8_HC45: 0x4001482D |
| DSI8_HC46: 0x4001482E | DSI8_HC47: 0x4001482F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI8_HC48: 0x40014830 | DSI8_HC49: 0x40014831 |
| DSI8_HC50: 0x40014832 | DSI8_HC51: 0x40014833 |
| DSI8_HC52: 0x40014834 | DSI8_HC53: 0x40014835 |
| DSI8_HC54: 0x40014836 | DSI8_HC55: 0x40014837 |
| DSI8_HC56: 0x40014838 | DSI8_HC57: 0x40014839 |
| DSI8_HC58: 0x4001483A | DSI8_HC59: 0x4001483B |
| DSI8_HC60: 0x4001483C | DSI8_HC61: 0x4001483D |
| DSI8_HC62: 0x4001483E | DSI8_HC63: 0x4001483F |
| DSI8_HC64: 0x40014840 | DSI8_HC65: 0x40014841 |
| DSI8_HC66: 0x40014842 | DSI8_HC67: 0x40014843 |
| DSI8_HC68: 0x40014844 | DSI8_HC69: 0x40014845 |
| DSI8_HC70: 0x40014846 | DSI8_HC71: 0x40014847 |
| DSI8_HC72: 0x40014848 | DSI8_HC73: 0x40014849 |
| DSI8_HC74: 0x4001484A | DSI8_HC75: 0x4001484B |
| DSI8_HC76: 0x4001484C | DSI8_HC77: 0x4001484D |
| DSI8_HC78: 0x4001484E | DSI8_HC79: 0x4001484F |
| DSI8_HC80: 0x40014850 | DSI8_HC81: 0x40014851 |
| DSI8_HC82: 0x40014852 | DSI8_HC83: 0x40014853 |
| DSI8_HC84: 0x40014854 | DSI8_HC85: 0x40014855 |
| DSI8_HC86: 0x40014856 | DSI8_HC87: 0x40014857 |
| DSI8_HC88: 0x40014858 | DSI8_HC89: 0x40014859 |
| DSI8_HC90: 0x4001485A | DSI8_HC91: 0x4001485B |
| DSI8_HC92: 0x4001485C | DSI8_HC93: 0x4001485D |
| DSI8_HC94: 0x4001485E | DSI8_HC95: 0x4001485F |
| DSI8_HC96: 0x40014860 | DSI8_HC97: 0x40014861 |
| DSI8_HC98: 0x40014862 | DSI8_HC99: 0x40014863 |
| DSI8_HC100: 0x40014864 | DSI8_HC101: 0x40014865 |
| DSI8_HC102: 0x40014866 | DSI8_HC103: 0x40014867 |
| DSI8_HC104: 0x40014868 | DSI8_HC105: 0x40014869 |
| DSI8_HC106: 0x4001486A | DSI8_HC107: 0x4001486B |
| DSI8_HC108: 0x4001486C | DSI8_HC109: 0x4001486D |
| DSI8_HC110: 0x4001486E | DSI8_HC111: 0x4001486F |
| DSI8_HC112: 0x40014870 | DSI8_HC113: 0x40014871 |
| DSI8_HC114: 0x40014872 | DSI8_HC115: 0x40014873 |
| DSI8_HC116: 0x40014874 | DSI8_HC117: 0x40014875 |
| DSI8_HC118: 0x40014876 | DSI8_HC119: 0x40014877 |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI8_HC120: 0x40014878 | DSI8_HC121: 0x40014879 |
| DSI8_HC122: 0x4001487A | DSI8_HC123: 0x4001487B |
| DSI8_HC124: 0x4001487C | DSI8_HC125: 0x4001487D |
| DSI8_HC126: 0x4001487E | DSI8_HC127: 0x4001487F |
| DSI9_HC0: 0x40014900 | DSI9_HC1: 0x40014901 |
| DSI9_HC2: 0x40014902 | DSI9_HC3: 0x40014903 |
| DSI9_HC4: 0x40014904 | DSI9_HC5: 0x40014905 |
| DSI9_HC6: 0x40014906 | DSI9_HC7: 0x40014907 |
| DSI9_HC8: 0x40014908 | DSI9_HC9: 0x40014909 |
| DSI9_HC10: 0x4001490A | DSI9_HC11: 0x4001490B |
| DSI9_HC12: 0x4001490C | DSI9_HC13: 0x4001490D |
| DSI9_HC14: 0x4001490E | DSI9_HC15: 0x4001490F |
| DSI9_HC16: 0x40014910 | DSI9_HC17: 0x40014911 |
| DSI9_HC18: 0x40014912 | DSI9_HC19: 0x40014913 |
| DSI9_HC20: 0x40014914 | DSI9_HC21: 0x40014915 |
| DSI9_HC22: 0x40014916 | DSI9_HC23: 0x40014917 |
| DSI9_HC24: 0x40014918 | DSI9_HC25: 0x40014919 |
| DSI9_HC26: 0x4001491A | DSI9_HC27: 0x4001491B |
| DSI9_HC28: 0x4001491C | DSI9_HC29: 0x4001491D |
| DSI9_HC30: 0x4001491E | DSI9_HC31: 0x4001491F |
| DSI9_HC32: 0x40014920 | DSI9_HC33: 0x40014921 |
| DSI9_HC34: 0x40014922 | DSI9_HC35: 0x40014923 |
| DSI9_HC36: 0x40014924 | DSI9_HC37: 0x40014925 |
| DSI9_HC38: 0x40014926 | DSI9_HC39: 0x40014927 |
| DSI9_HC40: 0x40014928 | DSI9_HC41: 0x40014929 |
| DSI9_HC42: 0x4001492A | DSI9_HC43: 0x4001492B |
| DSI9_HC44: 0x4001492C | DSI9_HC45: 0x4001492D |
| DSI9_HC46: 0x4001492E | DSI9_HC47: 0x4001492F |
| DSI9_HC48: 0x40014930 | DSI9_HC49: 0x40014931 |
| DSI9_HC50: 0x40014932 | DSI9_HC51: 0x40014933 |
| DSI9_HC52: 0x40014934 | DSI9_HC53: 0x40014935 |
| DSI9_HC54: 0x40014936 | DSI9_HC55: 0x40014937 |
| DSI9_HC56: 0x40014938 | DSI9_HC57: 0x40014939 |
| DSI9_HC58: 0x4001493A | DSI9_HC59: 0x4001493B |
| DSI9_HC60: 0x4001493C | DSI9_HC61: 0x4001493D |
| DSI9_HC62: 0x4001493E | DSI9_HC63: 0x4001493F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI9_HC64: 0x40014940 | DSI9_HC65: 0x40014941 |
| DSI9_HC66: 0x40014942 | DSI9_HC67: 0x40014943 |
| DSI9_HC68: 0x40014944 | DSI9_HC69: 0x40014945 |
| DSI9_HC70: 0x40014946 | DSI9_HC71: 0x40014947 |
| DSI9_HC72: 0x40014948 | DSI9_HC73: 0x40014949 |
| DSI9_HC74: 0x4001494A | DSI9_HC75: 0x4001494B |
| DSI9_HC76: 0x4001494C | DSI9_HC77: 0x4001494D |
| DSI9_HC78: 0x4001494E | DSI9_HC79: 0x4001494F |
| DSI9_HC80: 0x40014950 | DSI9_HC81: 0x40014951 |
| DSI9_HC82: 0x40014952 | DSI9_HC83: 0x40014953 |
| DSI9_HC84: 0x40014954 | DSI9_HC85: 0x40014955 |
| DSI9_HC86: 0x40014956 | DSI9_HC87: 0x40014957 |
| DSI9_HC88: 0x40014958 | DSI9_HC89: 0x40014959 |
| DSI9_HC90: 0x4001495A | DSI9_HC91: 0x4001495B |
| DSI9_HC92: 0x4001495C | DSI9_HC93: 0x4001495D |
| DSI9_HC94: 0x4001495E | DSI9_HC95: 0x4001495F |
| DSI9_HC96: 0x40014960 | DSI9_HC97: 0x40014961 |
| DSI9_HC98: 0x40014962 | DSI9_HC99: 0x40014963 |
| DSI9_HC100: 0x40014964 | DSI9_HC101: 0x40014965 |
| DSI9_HC102: 0x40014966 | DSI9_HC103: 0x40014967 |
| DSI9_HC104: 0x40014968 | DSI9_HC105: 0x40014969 |
| DSI9_HC106: 0x4001496A | DSI9_HC107: 0x4001496B |
| DSI9_HC108: 0x4001496C | DSI9_HC109: 0x4001496D |
| DSI9_HC110: 0x4001496E | DSI9_HC111: 0x4001496F |
| DSI9_HC112: 0x40014970 | DSI9_HC113: 0x40014971 |
| DSI9_HC114: 0x40014972 | DSI9_HC115: 0x40014973 |
| DSI9_HC116: 0x40014974 | DSI9_HC117: 0x40014975 |
| DSI9_HC118: 0x40014976 | DSI9_HC119: 0x40014977 |
| DSI9_HC120: 0x40014978 | DSI9_HC121: 0x40014979 |
| DSI9_HC122: 0x4001497A | DSI9_HC123: 0x4001497B |
| DSI9_HC124: 0x4001497C | DSI9_HC125: 0x4001497D |
| DSI9_HC126: 0x4001497E | DSI9_HC127: 0x4001497F |
| DSI12_HC0: 0x40014C00 | DSI12_HC1: 0x40014C01 |
| DSI12_HC2: 0x40014C02 | DSI12_HC3: 0x40014C03 |
| DSI12_HC4: 0x40014C04 | DSI12_HC5: 0x40014C05 |
| DSI12_HC6: 0x40014C06 | DSI12_HC7: 0x40014C07 |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI12_HC8: 0x40014C08 | DSI12_HC9: 0x40014C09 |
| DSI12_HC10: 0x40014C0A | DSI12_HC11: 0x40014C0B |
| DSI12_HC12: 0x40014C0C | DSI12_HC13: 0x40014C0D |
| DSI12_HC14: 0x40014C0E | DSI12_HC15: 0x40014C0F |
| DSI12_HC16: 0x40014C10 | DSI12_HC17: 0x40014C11 |
| DSI12_HC18: 0x40014C12 | DSI12_HC19: 0x40014C13 |
| DSI12_HC20: 0x40014C14 | DSI12_HC21: 0x40014C15 |
| DSI12_HC22: 0x40014C16 | DSI12_HC23: 0x40014C17 |
| DSI12_HC24: 0x40014C18 | DSI12_HC25: 0x40014C19 |
| DSI12_HC26: 0x40014C1A | DSI12_HC27: 0x40014C1B |
| DSI12_HC28: 0x40014C1C | DSI12_HC29: 0x40014C1D |
| DSI12_HC30: 0x40014C1E | DSI12_HC31: 0x40014C1F |
| DSI12_HC32: 0x40014C20 | DSI12_HC33: 0x40014C21 |
| DSI12_HC34: 0x40014C22 | DSI12_HC35: 0x40014C23 |
| DSI12_HC36: 0x40014C24 | DSI12_HC37: 0x40014C25 |
| DSI12_HC38: 0x40014C26 | DSI12_HC39: 0x40014C27 |
| DSI12_HC40: 0x40014C28 | DSI12_HC41: 0x40014C29 |
| DSI12_HC42: 0x40014C2A | DSI12_HC43: 0x40014C2B |
| DSI12_HC44: 0x40014C2C | DSI12_HC45: 0x40014C2D |
| DSI12_HC46: 0x40014C2E | DSI12_HC47: 0x40014C2F |
| DSI12_HC48: 0x40014C30 | DSI12_HC49: 0x40014C31 |
| DSI12_HC50: 0x40014C32 | DSI12_HC51: 0x40014C33 |
| DSI12_HC52: 0x40014C34 | DSI12_HC53: 0x40014C35 |
| DSI12_HC54: 0x40014C36 | DSI12_HC55: 0x40014C37 |
| DSI12_HC56: 0x40014C38 | DSI12_HC57: 0x40014C39 |
| DSI12_HC58: 0x40014C3A | DSI12_HC59: 0x40014C3B |
| DSI12_HC60: 0x40014C3C | DSI12_HC61: 0x40014C3D |
| DSI12_HC62: 0x40014C3E | DSI12_HC63: 0x40014C3F |
| DSI12_HC64: 0x40014C40 | DSI12_HC65: 0x40014C41 |
| DSI12_HC66: 0x40014C42 | DSI12_HC67: 0x40014C43 |
| DSI12_HC68: 0x40014C44 | DSI12_HC69: 0x40014C45 |
| DSI12_HC70: 0x40014C46 | DSI12_HC71: 0x40014C47 |
| DSI12_HC72: 0x40014C48 | DSI12_HC73: 0x40014C49 |
| DSI12_HC74: 0x40014C4A | DSI12_HC75: 0x40014C4B |
| DSI12_HC76: 0x40014C4C | DSI12_HC77: 0x40014C4D |
| DSI12_HC78: 0x40014C4E | DSI12_HC79: 0x40014C4F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|-------------------------|-------------------------|
| DSI12_HC80: 0x40014C50 | DSI12_HC81: 0x40014C51 |
| DSI12_HC82: 0x40014C52 | DSI12_HC83: 0x40014C53 |
| DSI12_HC84: 0x40014C54 | DSI12_HC85: 0x40014C55 |
| DSI12_HC86: 0x40014C56 | DSI12_HC87: 0x40014C57 |
| DSI12_HC88: 0x40014C58 | DSI12_HC89: 0x40014C59 |
| DSI12_HC90: 0x40014C5A | DSI12_HC91: 0x40014C5B |
| DSI12_HC92: 0x40014C5C | DSI12_HC93: 0x40014C5D |
| DSI12_HC94: 0x40014C5E | DSI12_HC95: 0x40014C5F |
| DSI12_HC96: 0x40014C60 | DSI12_HC97: 0x40014C61 |
| DSI12_HC98: 0x40014C62 | DSI12_HC99: 0x40014C63 |
| DSI12_HC100: 0x40014C64 | DSI12_HC101: 0x40014C65 |
| DSI12_HC102: 0x40014C66 | DSI12_HC103: 0x40014C67 |
| DSI12_HC104: 0x40014C68 | DSI12_HC105: 0x40014C69 |
| DSI12_HC106: 0x40014C6A | DSI12_HC107: 0x40014C6B |
| DSI12_HC108: 0x40014C6C | DSI12_HC109: 0x40014C6D |
| DSI12_HC110: 0x40014C6E | DSI12_HC111: 0x40014C6F |
| DSI12_HC112: 0x40014C70 | DSI12_HC113: 0x40014C71 |
| DSI12_HC114: 0x40014C72 | DSI12_HC115: 0x40014C73 |
| DSI12_HC116: 0x40014C74 | DSI12_HC117: 0x40014C75 |
| DSI12_HC118: 0x40014C76 | DSI12_HC119: 0x40014C77 |
| DSI12_HC120: 0x40014C78 | DSI12_HC121: 0x40014C79 |
| DSI12_HC122: 0x40014C7A | DSI12_HC123: 0x40014C7B |
| DSI12_HC124: 0x40014C7C | DSI12_HC125: 0x40014C7D |
| DSI12_HC126: 0x40014C7E | DSI12_HC127: 0x40014C7F |
| DSI13_HC0: 0x40014D00 | DSI13_HC1: 0x40014D01 |
| DSI13_HC2: 0x40014D02 | DSI13_HC3: 0x40014D03 |
| DSI13_HC4: 0x40014D04 | DSI13_HC5: 0x40014D05 |
| DSI13_HC6: 0x40014D06 | DSI13_HC7: 0x40014D07 |
| DSI13_HC8: 0x40014D08 | DSI13_HC9: 0x40014D09 |
| DSI13_HC10: 0x40014D0A | DSI13_HC11: 0x40014D0B |
| DSI13_HC12: 0x40014D0C | DSI13_HC13: 0x40014D0D |
| DSI13_HC14: 0x40014D0E | DSI13_HC15: 0x40014D0F |
| DSI13_HC16: 0x40014D10 | DSI13_HC17: 0x40014D11 |
| DSI13_HC18: 0x40014D12 | DSI13_HC19: 0x40014D13 |
| DSI13_HC20: 0x40014D14 | DSI13_HC21: 0x40014D15 |
| DSI13_HC22: 0x40014D16 | DSI13_HC23: 0x40014D17 |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI13_HC24: 0x40014D18 | DSI13_HC25: 0x40014D19 |
| DSI13_HC26: 0x40014D1A | DSI13_HC27: 0x40014D1B |
| DSI13_HC28: 0x40014D1C | DSI13_HC29: 0x40014D1D |
| DSI13_HC30: 0x40014D1E | DSI13_HC31: 0x40014D1F |
| DSI13_HC32: 0x40014D20 | DSI13_HC33: 0x40014D21 |
| DSI13_HC34: 0x40014D22 | DSI13_HC35: 0x40014D23 |
| DSI13_HC36: 0x40014D24 | DSI13_HC37: 0x40014D25 |
| DSI13_HC38: 0x40014D26 | DSI13_HC39: 0x40014D27 |
| DSI13_HC40: 0x40014D28 | DSI13_HC41: 0x40014D29 |
| DSI13_HC42: 0x40014D2A | DSI13_HC43: 0x40014D2B |
| DSI13_HC44: 0x40014D2C | DSI13_HC45: 0x40014D2D |
| DSI13_HC46: 0x40014D2E | DSI13_HC47: 0x40014D2F |
| DSI13_HC48: 0x40014D30 | DSI13_HC49: 0x40014D31 |
| DSI13_HC50: 0x40014D32 | DSI13_HC51: 0x40014D33 |
| DSI13_HC52: 0x40014D34 | DSI13_HC53: 0x40014D35 |
| DSI13_HC54: 0x40014D36 | DSI13_HC55: 0x40014D37 |
| DSI13_HC56: 0x40014D38 | DSI13_HC57: 0x40014D39 |
| DSI13_HC58: 0x40014D3A | DSI13_HC59: 0x40014D3B |
| DSI13_HC60: 0x40014D3C | DSI13_HC61: 0x40014D3D |
| DSI13_HC62: 0x40014D3E | DSI13_HC63: 0x40014D3F |
| DSI13_HC64: 0x40014D40 | DSI13_HC65: 0x40014D41 |
| DSI13_HC66: 0x40014D42 | DSI13_HC67: 0x40014D43 |
| DSI13_HC68: 0x40014D44 | DSI13_HC69: 0x40014D45 |
| DSI13_HC70: 0x40014D46 | DSI13_HC71: 0x40014D47 |
| DSI13_HC72: 0x40014D48 | DSI13_HC73: 0x40014D49 |
| DSI13_HC74: 0x40014D4A | DSI13_HC75: 0x40014D4B |
| DSI13_HC76: 0x40014D4C | DSI13_HC77: 0x40014D4D |
| DSI13_HC78: 0x40014D4E | DSI13_HC79: 0x40014D4F |
| DSI13_HC80: 0x40014D50 | DSI13_HC81: 0x40014D51 |
| DSI13_HC82: 0x40014D52 | DSI13_HC83: 0x40014D53 |
| DSI13_HC84: 0x40014D54 | DSI13_HC85: 0x40014D55 |
| DSI13_HC86: 0x40014D56 | DSI13_HC87: 0x40014D57 |
| DSI13_HC88: 0x40014D58 | DSI13_HC89: 0x40014D59 |
| DSI13_HC90: 0x40014D5A | DSI13_HC91: 0x40014D5B |
| DSI13_HC92: 0x40014D5C | DSI13_HC93: 0x40014D5D |
| DSI13_HC94: 0x40014D5E | DSI13_HC95: 0x40014D5F |

1.3.1234 DSI[0..15]_HC[0..127] (continued)

Register : Address

| | |
|-------------------------|-------------------------|
| DSI13_HC96: 0x40014D60 | DSI13_HC97: 0x40014D61 |
| DSI13_HC98: 0x40014D62 | DSI13_HC99: 0x40014D63 |
| DSI13_HC100: 0x40014D64 | DSI13_HC101: 0x40014D65 |
| DSI13_HC102: 0x40014D66 | DSI13_HC103: 0x40014D67 |
| DSI13_HC104: 0x40014D68 | DSI13_HC105: 0x40014D69 |
| DSI13_HC106: 0x40014D6A | DSI13_HC107: 0x40014D6B |
| DSI13_HC108: 0x40014D6C | DSI13_HC109: 0x40014D6D |
| DSI13_HC110: 0x40014D6E | DSI13_HC111: 0x40014D6F |
| DSI13_HC112: 0x40014D70 | DSI13_HC113: 0x40014D71 |
| DSI13_HC114: 0x40014D72 | DSI13_HC115: 0x40014D73 |
| DSI13_HC116: 0x40014D74 | DSI13_HC117: 0x40014D75 |
| DSI13_HC118: 0x40014D76 | DSI13_HC119: 0x40014D77 |
| DSI13_HC120: 0x40014D78 | DSI13_HC121: 0x40014D79 |
| DSI13_HC122: 0x40014D7A | DSI13_HC123: 0x40014D7B |
| DSI13_HC124: 0x40014D7C | DSI13_HC125: 0x40014D7D |
| DSI13_HC126: 0x40014D7E | DSI13_HC127: 0x40014D7F |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | hc_byte | | | | | | | |

DSI HC Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | hc_byte[7:0] | RAM configuration for DSI channel bytes |

1.3.1235 DSI[0..15]_HV_L[0..15]

HV_L

Reset: N/A

Register : Address

| | |
|-------------------------|-------------------------|
| DSI0_HV_L0: 0x40014080 | DSI0_HV_L1: 0x40014081 |
| DSI0_HV_L2: 0x40014082 | DSI0_HV_L3: 0x40014083 |
| DSI0_HV_L4: 0x40014084 | DSI0_HV_L5: 0x40014085 |
| DSI0_HV_L6: 0x40014086 | DSI0_HV_L7: 0x40014087 |
| DSI0_HV_L8: 0x40014088 | DSI0_HV_L9: 0x40014089 |
| DSI0_HV_L10: 0x4001408A | DSI0_HV_L11: 0x4001408B |
| DSI0_HV_L12: 0x4001408C | DSI0_HV_L13: 0x4001408D |
| DSI0_HV_L14: 0x4001408E | DSI0_HV_L15: 0x4001408F |
| DSI1_HV_L0: 0x40014180 | DSI1_HV_L1: 0x40014181 |
| DSI1_HV_L2: 0x40014182 | DSI1_HV_L3: 0x40014183 |
| DSI1_HV_L4: 0x40014184 | DSI1_HV_L5: 0x40014185 |
| DSI1_HV_L6: 0x40014186 | DSI1_HV_L7: 0x40014187 |
| DSI1_HV_L8: 0x40014188 | DSI1_HV_L9: 0x40014189 |
| DSI1_HV_L10: 0x4001418A | DSI1_HV_L11: 0x4001418B |
| DSI1_HV_L12: 0x4001418C | DSI1_HV_L13: 0x4001418D |
| DSI1_HV_L14: 0x4001418E | DSI1_HV_L15: 0x4001418F |
| DSI2_HV_L0: 0x40014280 | DSI2_HV_L1: 0x40014281 |
| DSI2_HV_L2: 0x40014282 | DSI2_HV_L3: 0x40014283 |
| DSI2_HV_L4: 0x40014284 | DSI2_HV_L5: 0x40014285 |
| DSI2_HV_L6: 0x40014286 | DSI2_HV_L7: 0x40014287 |
| DSI2_HV_L8: 0x40014288 | DSI2_HV_L9: 0x40014289 |
| DSI2_HV_L10: 0x4001428A | DSI2_HV_L11: 0x4001428B |
| DSI2_HV_L12: 0x4001428C | DSI2_HV_L13: 0x4001428D |
| DSI2_HV_L14: 0x4001428E | DSI2_HV_L15: 0x4001428F |
| DSI3_HV_L0: 0x40014380 | DSI3_HV_L1: 0x40014381 |
| DSI3_HV_L2: 0x40014382 | DSI3_HV_L3: 0x40014383 |
| DSI3_HV_L4: 0x40014384 | DSI3_HV_L5: 0x40014385 |
| DSI3_HV_L6: 0x40014386 | DSI3_HV_L7: 0x40014387 |
| DSI3_HV_L8: 0x40014388 | DSI3_HV_L9: 0x40014389 |
| DSI3_HV_L10: 0x4001438A | DSI3_HV_L11: 0x4001438B |
| DSI3_HV_L12: 0x4001438C | DSI3_HV_L13: 0x4001438D |
| DSI3_HV_L14: 0x4001438E | DSI3_HV_L15: 0x4001438F |

1.3.1235 DSI[0..15]_HV_L[0..15] (continued)

Register : Address

| | |
|-------------------------|-------------------------|
| DSI4_HV_L0: 0x40014480 | DSI4_HV_L1: 0x40014481 |
| DSI4_HV_L2: 0x40014482 | DSI4_HV_L3: 0x40014483 |
| DSI4_HV_L4: 0x40014484 | DSI4_HV_L5: 0x40014485 |
| DSI4_HV_L6: 0x40014486 | DSI4_HV_L7: 0x40014487 |
| DSI4_HV_L8: 0x40014488 | DSI4_HV_L9: 0x40014489 |
| DSI4_HV_L10: 0x4001448A | DSI4_HV_L11: 0x4001448B |
| DSI4_HV_L12: 0x4001448C | DSI4_HV_L13: 0x4001448D |
| DSI4_HV_L14: 0x4001448E | DSI4_HV_L15: 0x4001448F |
| DSI5_HV_L0: 0x40014580 | DSI5_HV_L1: 0x40014581 |
| DSI5_HV_L2: 0x40014582 | DSI5_HV_L3: 0x40014583 |
| DSI5_HV_L4: 0x40014584 | DSI5_HV_L5: 0x40014585 |
| DSI5_HV_L6: 0x40014586 | DSI5_HV_L7: 0x40014587 |
| DSI5_HV_L8: 0x40014588 | DSI5_HV_L9: 0x40014589 |
| DSI5_HV_L10: 0x4001458A | DSI5_HV_L11: 0x4001458B |
| DSI5_HV_L12: 0x4001458C | DSI5_HV_L13: 0x4001458D |
| DSI5_HV_L14: 0x4001458E | DSI5_HV_L15: 0x4001458F |
| DSI6_HV_L0: 0x40014680 | DSI6_HV_L1: 0x40014681 |
| DSI6_HV_L2: 0x40014682 | DSI6_HV_L3: 0x40014683 |
| DSI6_HV_L4: 0x40014684 | DSI6_HV_L5: 0x40014685 |
| DSI6_HV_L6: 0x40014686 | DSI6_HV_L7: 0x40014687 |
| DSI6_HV_L8: 0x40014688 | DSI6_HV_L9: 0x40014689 |
| DSI6_HV_L10: 0x4001468A | DSI6_HV_L11: 0x4001468B |
| DSI6_HV_L12: 0x4001468C | DSI6_HV_L13: 0x4001468D |
| DSI6_HV_L14: 0x4001468E | DSI6_HV_L15: 0x4001468F |
| DSI7_HV_L0: 0x40014780 | DSI7_HV_L1: 0x40014781 |
| DSI7_HV_L2: 0x40014782 | DSI7_HV_L3: 0x40014783 |
| DSI7_HV_L4: 0x40014784 | DSI7_HV_L5: 0x40014785 |
| DSI7_HV_L6: 0x40014786 | DSI7_HV_L7: 0x40014787 |
| DSI7_HV_L8: 0x40014788 | DSI7_HV_L9: 0x40014789 |
| DSI7_HV_L10: 0x4001478A | DSI7_HV_L11: 0x4001478B |
| DSI7_HV_L12: 0x4001478C | DSI7_HV_L13: 0x4001478D |
| DSI7_HV_L14: 0x4001478E | DSI7_HV_L15: 0x4001478F |
| DSI8_HV_L0: 0x40014880 | DSI8_HV_L1: 0x40014881 |
| DSI8_HV_L2: 0x40014882 | DSI8_HV_L3: 0x40014883 |
| DSI8_HV_L4: 0x40014884 | DSI8_HV_L5: 0x40014885 |
| DSI8_HV_L6: 0x40014886 | DSI8_HV_L7: 0x40014887 |

1.3.1235 DSI[0..15]_HV_L[0..15] (continued)

Register : Address

| | |
|--------------------------|--------------------------|
| DSI8_HV_L8: 0x40014888 | DSI8_HV_L9: 0x40014889 |
| DSI8_HV_L10: 0x4001488A | DSI8_HV_L11: 0x4001488B |
| DSI8_HV_L12: 0x4001488C | DSI8_HV_L13: 0x4001488D |
| DSI8_HV_L14: 0x4001488E | DSI8_HV_L15: 0x4001488F |
| DSI9_HV_L0: 0x40014980 | DSI9_HV_L1: 0x40014981 |
| DSI9_HV_L2: 0x40014982 | DSI9_HV_L3: 0x40014983 |
| DSI9_HV_L4: 0x40014984 | DSI9_HV_L5: 0x40014985 |
| DSI9_HV_L6: 0x40014986 | DSI9_HV_L7: 0x40014987 |
| DSI9_HV_L8: 0x40014988 | DSI9_HV_L9: 0x40014989 |
| DSI9_HV_L10: 0x4001498A | DSI9_HV_L11: 0x4001498B |
| DSI9_HV_L12: 0x4001498C | DSI9_HV_L13: 0x4001498D |
| DSI9_HV_L14: 0x4001498E | DSI9_HV_L15: 0x4001498F |
| DSI12_HV_L0: 0x40014C80 | DSI12_HV_L1: 0x40014C81 |
| DSI12_HV_L2: 0x40014C82 | DSI12_HV_L3: 0x40014C83 |
| DSI12_HV_L4: 0x40014C84 | DSI12_HV_L5: 0x40014C85 |
| DSI12_HV_L6: 0x40014C86 | DSI12_HV_L7: 0x40014C87 |
| DSI12_HV_L8: 0x40014C88 | DSI12_HV_L9: 0x40014C89 |
| DSI12_HV_L10: 0x40014C8A | DSI12_HV_L11: 0x40014C8B |
| DSI12_HV_L12: 0x40014C8C | DSI12_HV_L13: 0x40014C8D |
| DSI12_HV_L14: 0x40014C8E | DSI12_HV_L15: 0x40014C8F |
| DSI13_HV_L0: 0x40014D80 | DSI13_HV_L1: 0x40014D81 |
| DSI13_HV_L2: 0x40014D82 | DSI13_HV_L3: 0x40014D83 |
| DSI13_HV_L4: 0x40014D84 | DSI13_HV_L5: 0x40014D85 |
| DSI13_HV_L6: 0x40014D86 | DSI13_HV_L7: 0x40014D87 |
| DSI13_HV_L8: 0x40014D88 | DSI13_HV_L9: 0x40014D89 |
| DSI13_HV_L10: 0x40014D8A | DSI13_HV_L11: 0x40014D8B |
| DSI13_HV_L12: 0x40014D8C | DSI13_HV_L13: 0x40014D8D |
| DSI13_HV_L14: 0x40014D8E | DSI13_HV_L15: 0x40014D8F |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | hv_byte | | | | | | | |

DSI HV Tile Configuration

Register Segment: 2

@(0x40014000 + [0..15 * 0x100]) + 0x80 + [0..15 * 0x1]

1.3.1235 DSI[0..15]_HV_L[0..15] (continued)

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | hv_byte[7:0] | RAM configuration for DSI channel bytes |

1.3.1236 DSI[0..15]_HS[0..23]

HS

Reset: N/A

Register : Address

| | |
|-----------------------|-----------------------|
| DSI0_HS0: 0x40014090 | DSI0_HS1: 0x40014091 |
| DSI0_HS2: 0x40014092 | DSI0_HS3: 0x40014093 |
| DSI0_HS4: 0x40014094 | DSI0_HS5: 0x40014095 |
| DSI0_HS6: 0x40014096 | DSI0_HS7: 0x40014097 |
| DSI0_HS8: 0x40014098 | DSI0_HS9: 0x40014099 |
| DSI0_HS10: 0x4001409A | DSI0_HS11: 0x4001409B |
| DSI0_HS12: 0x4001409C | DSI0_HS13: 0x4001409D |
| DSI0_HS14: 0x4001409E | DSI0_HS15: 0x4001409F |
| DSI0_HS16: 0x400140A0 | DSI0_HS17: 0x400140A1 |
| DSI0_HS18: 0x400140A2 | DSI0_HS19: 0x400140A3 |
| DSI0_HS20: 0x400140A4 | DSI0_HS21: 0x400140A5 |
| DSI0_HS22: 0x400140A6 | DSI0_HS23: 0x400140A7 |
| DSI1_HS0: 0x40014190 | DSI1_HS1: 0x40014191 |
| DSI1_HS2: 0x40014192 | DSI1_HS3: 0x40014193 |
| DSI1_HS4: 0x40014194 | DSI1_HS5: 0x40014195 |
| DSI1_HS6: 0x40014196 | DSI1_HS7: 0x40014197 |
| DSI1_HS8: 0x40014198 | DSI1_HS9: 0x40014199 |
| DSI1_HS10: 0x4001419A | DSI1_HS11: 0x4001419B |
| DSI1_HS12: 0x4001419C | DSI1_HS13: 0x4001419D |
| DSI1_HS14: 0x4001419E | DSI1_HS15: 0x4001419F |
| DSI1_HS16: 0x400141A0 | DSI1_HS17: 0x400141A1 |
| DSI1_HS18: 0x400141A2 | DSI1_HS19: 0x400141A3 |
| DSI1_HS20: 0x400141A4 | DSI1_HS21: 0x400141A5 |
| DSI1_HS22: 0x400141A6 | DSI1_HS23: 0x400141A7 |
| DSI2_HS0: 0x40014290 | DSI2_HS1: 0x40014291 |
| DSI2_HS2: 0x40014292 | DSI2_HS3: 0x40014293 |
| DSI2_HS4: 0x40014294 | DSI2_HS5: 0x40014295 |
| DSI2_HS6: 0x40014296 | DSI2_HS7: 0x40014297 |
| DSI2_HS8: 0x40014298 | DSI2_HS9: 0x40014299 |
| DSI2_HS10: 0x4001429A | DSI2_HS11: 0x4001429B |
| DSI2_HS12: 0x4001429C | DSI2_HS13: 0x4001429D |
| DSI2_HS14: 0x4001429E | DSI2_HS15: 0x4001429F |

1.3.1236 DSI[0..15]_HS[0..23] (continued)

Register : Address

| | |
|-----------------------|-----------------------|
| DSI2_HS16: 0x400142A0 | DSI2_HS17: 0x400142A1 |
| DSI2_HS18: 0x400142A2 | DSI2_HS19: 0x400142A3 |
| DSI2_HS20: 0x400142A4 | DSI2_HS21: 0x400142A5 |
| DSI2_HS22: 0x400142A6 | DSI2_HS23: 0x400142A7 |
| DSI3_HS0: 0x40014390 | DSI3_HS1: 0x40014391 |
| DSI3_HS2: 0x40014392 | DSI3_HS3: 0x40014393 |
| DSI3_HS4: 0x40014394 | DSI3_HS5: 0x40014395 |
| DSI3_HS6: 0x40014396 | DSI3_HS7: 0x40014397 |
| DSI3_HS8: 0x40014398 | DSI3_HS9: 0x40014399 |
| DSI3_HS10: 0x4001439A | DSI3_HS11: 0x4001439B |
| DSI3_HS12: 0x4001439C | DSI3_HS13: 0x4001439D |
| DSI3_HS14: 0x4001439E | DSI3_HS15: 0x4001439F |
| DSI3_HS16: 0x400143A0 | DSI3_HS17: 0x400143A1 |
| DSI3_HS18: 0x400143A2 | DSI3_HS19: 0x400143A3 |
| DSI3_HS20: 0x400143A4 | DSI3_HS21: 0x400143A5 |
| DSI3_HS22: 0x400143A6 | DSI3_HS23: 0x400143A7 |
| DSI4_HS0: 0x40014490 | DSI4_HS1: 0x40014491 |
| DSI4_HS2: 0x40014492 | DSI4_HS3: 0x40014493 |
| DSI4_HS4: 0x40014494 | DSI4_HS5: 0x40014495 |
| DSI4_HS6: 0x40014496 | DSI4_HS7: 0x40014497 |
| DSI4_HS8: 0x40014498 | DSI4_HS9: 0x40014499 |
| DSI4_HS10: 0x4001449A | DSI4_HS11: 0x4001449B |
| DSI4_HS12: 0x4001449C | DSI4_HS13: 0x4001449D |
| DSI4_HS14: 0x4001449E | DSI4_HS15: 0x4001449F |
| DSI4_HS16: 0x400144A0 | DSI4_HS17: 0x400144A1 |
| DSI4_HS18: 0x400144A2 | DSI4_HS19: 0x400144A3 |
| DSI4_HS20: 0x400144A4 | DSI4_HS21: 0x400144A5 |
| DSI4_HS22: 0x400144A6 | DSI4_HS23: 0x400144A7 |
| DSI5_HS0: 0x40014590 | DSI5_HS1: 0x40014591 |
| DSI5_HS2: 0x40014592 | DSI5_HS3: 0x40014593 |
| DSI5_HS4: 0x40014594 | DSI5_HS5: 0x40014595 |
| DSI5_HS6: 0x40014596 | DSI5_HS7: 0x40014597 |
| DSI5_HS8: 0x40014598 | DSI5_HS9: 0x40014599 |
| DSI5_HS10: 0x4001459A | DSI5_HS11: 0x4001459B |
| DSI5_HS12: 0x4001459C | DSI5_HS13: 0x4001459D |
| DSI5_HS14: 0x4001459E | DSI5_HS15: 0x4001459F |

1.3.1236 DSI[0..15]_HS[0..23] (continued)

Register : Address

| | |
|-----------------------|-----------------------|
| DSI5_HS16: 0x400145A0 | DSI5_HS17: 0x400145A1 |
| DSI5_HS18: 0x400145A2 | DSI5_HS19: 0x400145A3 |
| DSI5_HS20: 0x400145A4 | DSI5_HS21: 0x400145A5 |
| DSI5_HS22: 0x400145A6 | DSI5_HS23: 0x400145A7 |
| DSI6_HS0: 0x40014690 | DSI6_HS1: 0x40014691 |
| DSI6_HS2: 0x40014692 | DSI6_HS3: 0x40014693 |
| DSI6_HS4: 0x40014694 | DSI6_HS5: 0x40014695 |
| DSI6_HS6: 0x40014696 | DSI6_HS7: 0x40014697 |
| DSI6_HS8: 0x40014698 | DSI6_HS9: 0x40014699 |
| DSI6_HS10: 0x4001469A | DSI6_HS11: 0x4001469B |
| DSI6_HS12: 0x4001469C | DSI6_HS13: 0x4001469D |
| DSI6_HS14: 0x4001469E | DSI6_HS15: 0x4001469F |
| DSI6_HS16: 0x400146A0 | DSI6_HS17: 0x400146A1 |
| DSI6_HS18: 0x400146A2 | DSI6_HS19: 0x400146A3 |
| DSI6_HS20: 0x400146A4 | DSI6_HS21: 0x400146A5 |
| DSI6_HS22: 0x400146A6 | DSI6_HS23: 0x400146A7 |
| DSI7_HS0: 0x40014790 | DSI7_HS1: 0x40014791 |
| DSI7_HS2: 0x40014792 | DSI7_HS3: 0x40014793 |
| DSI7_HS4: 0x40014794 | DSI7_HS5: 0x40014795 |
| DSI7_HS6: 0x40014796 | DSI7_HS7: 0x40014797 |
| DSI7_HS8: 0x40014798 | DSI7_HS9: 0x40014799 |
| DSI7_HS10: 0x4001479A | DSI7_HS11: 0x4001479B |
| DSI7_HS12: 0x4001479C | DSI7_HS13: 0x4001479D |
| DSI7_HS14: 0x4001479E | DSI7_HS15: 0x4001479F |
| DSI7_HS16: 0x400147A0 | DSI7_HS17: 0x400147A1 |
| DSI7_HS18: 0x400147A2 | DSI7_HS19: 0x400147A3 |
| DSI7_HS20: 0x400147A4 | DSI7_HS21: 0x400147A5 |
| DSI7_HS22: 0x400147A6 | DSI7_HS23: 0x400147A7 |
| DSI8_HS0: 0x40014890 | DSI8_HS1: 0x40014891 |
| DSI8_HS2: 0x40014892 | DSI8_HS3: 0x40014893 |
| DSI8_HS4: 0x40014894 | DSI8_HS5: 0x40014895 |
| DSI8_HS6: 0x40014896 | DSI8_HS7: 0x40014897 |
| DSI8_HS8: 0x40014898 | DSI8_HS9: 0x40014899 |
| DSI8_HS10: 0x4001489A | DSI8_HS11: 0x4001489B |
| DSI8_HS12: 0x4001489C | DSI8_HS13: 0x4001489D |
| DSI8_HS14: 0x4001489E | DSI8_HS15: 0x4001489F |

1.3.1236 DSI[0..15]_HS[0..23] (continued)

Register : Address

| | |
|------------------------|------------------------|
| DSI8_HS16: 0x400148A0 | DSI8_HS17: 0x400148A1 |
| DSI8_HS18: 0x400148A2 | DSI8_HS19: 0x400148A3 |
| DSI8_HS20: 0x400148A4 | DSI8_HS21: 0x400148A5 |
| DSI8_HS22: 0x400148A6 | DSI8_HS23: 0x400148A7 |
| DSI9_HS0: 0x40014990 | DSI9_HS1: 0x40014991 |
| DSI9_HS2: 0x40014992 | DSI9_HS3: 0x40014993 |
| DSI9_HS4: 0x40014994 | DSI9_HS5: 0x40014995 |
| DSI9_HS6: 0x40014996 | DSI9_HS7: 0x40014997 |
| DSI9_HS8: 0x40014998 | DSI9_HS9: 0x40014999 |
| DSI9_HS10: 0x4001499A | DSI9_HS11: 0x4001499B |
| DSI9_HS12: 0x4001499C | DSI9_HS13: 0x4001499D |
| DSI9_HS14: 0x4001499E | DSI9_HS15: 0x4001499F |
| DSI9_HS16: 0x400149A0 | DSI9_HS17: 0x400149A1 |
| DSI9_HS18: 0x400149A2 | DSI9_HS19: 0x400149A3 |
| DSI9_HS20: 0x400149A4 | DSI9_HS21: 0x400149A5 |
| DSI9_HS22: 0x400149A6 | DSI9_HS23: 0x400149A7 |
| DSI12_HS0: 0x40014C90 | DSI12_HS1: 0x40014C91 |
| DSI12_HS2: 0x40014C92 | DSI12_HS3: 0x40014C93 |
| DSI12_HS4: 0x40014C94 | DSI12_HS5: 0x40014C95 |
| DSI12_HS6: 0x40014C96 | DSI12_HS7: 0x40014C97 |
| DSI12_HS8: 0x40014C98 | DSI12_HS9: 0x40014C99 |
| DSI12_HS10: 0x40014C9A | DSI12_HS11: 0x40014C9B |
| DSI12_HS12: 0x40014C9C | DSI12_HS13: 0x40014C9D |
| DSI12_HS14: 0x40014C9E | DSI12_HS15: 0x40014C9F |
| DSI12_HS16: 0x40014CA0 | DSI12_HS17: 0x40014CA1 |
| DSI12_HS18: 0x40014CA2 | DSI12_HS19: 0x40014CA3 |
| DSI12_HS20: 0x40014CA4 | DSI12_HS21: 0x40014CA5 |
| DSI12_HS22: 0x40014CA6 | DSI12_HS23: 0x40014CA7 |
| DSI13_HS0: 0x40014D90 | DSI13_HS1: 0x40014D91 |
| DSI13_HS2: 0x40014D92 | DSI13_HS3: 0x40014D93 |
| DSI13_HS4: 0x40014D94 | DSI13_HS5: 0x40014D95 |
| DSI13_HS6: 0x40014D96 | DSI13_HS7: 0x40014D97 |
| DSI13_HS8: 0x40014D98 | DSI13_HS9: 0x40014D99 |
| DSI13_HS10: 0x40014D9A | DSI13_HS11: 0x40014D9B |
| DSI13_HS12: 0x40014D9C | DSI13_HS13: 0x40014D9D |
| DSI13_HS14: 0x40014D9E | DSI13_HS15: 0x40014D9F |

1.3.1236 DSI[0..15]_HS[0..23] (continued)

Register : Address

DSI13_HS16: 0x40014DA0

DSI13_HS17: 0x40014DA1

DSI13_HS18: 0x40014DA2

DSI13_HS19: 0x40014DA3

DSI13_HS20: 0x40014DA4

DSI13_HS21: 0x40014DA5

DSI13_HS22: 0x40014DA6

DSI13_HS23: 0x40014DA7

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | RW:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | hs_byte | | | | | | | |

DSI HS Tile Configuration

Register Segment: 2

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | hs_byte[7:0] | RAM configuration for DSI channel bytes |

1.3.1237 DSI[0..15]_HV_R[0..15]

HV_R

Reset: N/A

Register : Address

| | |
|-------------------------|-------------------------|
| DSI0_HV_R0: 0x400140A8 | DSI0_HV_R1: 0x400140A9 |
| DSI0_HV_R2: 0x400140AA | DSI0_HV_R3: 0x400140AB |
| DSI0_HV_R4: 0x400140AC | DSI0_HV_R5: 0x400140AD |
| DSI0_HV_R6: 0x400140AE | DSI0_HV_R7: 0x400140AF |
| DSI0_HV_R8: 0x400140B0 | DSI0_HV_R9: 0x400140B1 |
| DSI0_HV_R10: 0x400140B2 | DSI0_HV_R11: 0x400140B3 |
| DSI0_HV_R12: 0x400140B4 | DSI0_HV_R13: 0x400140B5 |
| DSI0_HV_R14: 0x400140B6 | DSI0_HV_R15: 0x400140B7 |
| DSI1_HV_R0: 0x400141A8 | DSI1_HV_R1: 0x400141A9 |
| DSI1_HV_R2: 0x400141AA | DSI1_HV_R3: 0x400141AB |
| DSI1_HV_R4: 0x400141AC | DSI1_HV_R5: 0x400141AD |
| DSI1_HV_R6: 0x400141AE | DSI1_HV_R7: 0x400141AF |
| DSI1_HV_R8: 0x400141B0 | DSI1_HV_R9: 0x400141B1 |
| DSI1_HV_R10: 0x400141B2 | DSI1_HV_R11: 0x400141B3 |
| DSI1_HV_R12: 0x400141B4 | DSI1_HV_R13: 0x400141B5 |
| DSI1_HV_R14: 0x400141B6 | DSI1_HV_R15: 0x400141B7 |
| DSI2_HV_R0: 0x400142A8 | DSI2_HV_R1: 0x400142A9 |
| DSI2_HV_R2: 0x400142AA | DSI2_HV_R3: 0x400142AB |
| DSI2_HV_R4: 0x400142AC | DSI2_HV_R5: 0x400142AD |
| DSI2_HV_R6: 0x400142AE | DSI2_HV_R7: 0x400142AF |
| DSI2_HV_R8: 0x400142B0 | DSI2_HV_R9: 0x400142B1 |
| DSI2_HV_R10: 0x400142B2 | DSI2_HV_R11: 0x400142B3 |
| DSI2_HV_R12: 0x400142B4 | DSI2_HV_R13: 0x400142B5 |
| DSI2_HV_R14: 0x400142B6 | DSI2_HV_R15: 0x400142B7 |
| DSI3_HV_R0: 0x400143A8 | DSI3_HV_R1: 0x400143A9 |
| DSI3_HV_R2: 0x400143AA | DSI3_HV_R3: 0x400143AB |
| DSI3_HV_R4: 0x400143AC | DSI3_HV_R5: 0x400143AD |
| DSI3_HV_R6: 0x400143AE | DSI3_HV_R7: 0x400143AF |
| DSI3_HV_R8: 0x400143B0 | DSI3_HV_R9: 0x400143B1 |
| DSI3_HV_R10: 0x400143B2 | DSI3_HV_R11: 0x400143B3 |
| DSI3_HV_R12: 0x400143B4 | DSI3_HV_R13: 0x400143B5 |
| DSI3_HV_R14: 0x400143B6 | DSI3_HV_R15: 0x400143B7 |

1.3.1237 DSI[0..15]_HV_R[0..15] (continued)

Register : Address

| | |
|-------------------------|-------------------------|
| DSI4_HV_R0: 0x400144A8 | DSI4_HV_R1: 0x400144A9 |
| DSI4_HV_R2: 0x400144AA | DSI4_HV_R3: 0x400144AB |
| DSI4_HV_R4: 0x400144AC | DSI4_HV_R5: 0x400144AD |
| DSI4_HV_R6: 0x400144AE | DSI4_HV_R7: 0x400144AF |
| DSI4_HV_R8: 0x400144B0 | DSI4_HV_R9: 0x400144B1 |
| DSI4_HV_R10: 0x400144B2 | DSI4_HV_R11: 0x400144B3 |
| DSI4_HV_R12: 0x400144B4 | DSI4_HV_R13: 0x400144B5 |
| DSI4_HV_R14: 0x400144B6 | DSI4_HV_R15: 0x400144B7 |
| DSI5_HV_R0: 0x400145A8 | DSI5_HV_R1: 0x400145A9 |
| DSI5_HV_R2: 0x400145AA | DSI5_HV_R3: 0x400145AB |
| DSI5_HV_R4: 0x400145AC | DSI5_HV_R5: 0x400145AD |
| DSI5_HV_R6: 0x400145AE | DSI5_HV_R7: 0x400145AF |
| DSI5_HV_R8: 0x400145B0 | DSI5_HV_R9: 0x400145B1 |
| DSI5_HV_R10: 0x400145B2 | DSI5_HV_R11: 0x400145B3 |
| DSI5_HV_R12: 0x400145B4 | DSI5_HV_R13: 0x400145B5 |
| DSI5_HV_R14: 0x400145B6 | DSI5_HV_R15: 0x400145B7 |
| DSI6_HV_R0: 0x400146A8 | DSI6_HV_R1: 0x400146A9 |
| DSI6_HV_R2: 0x400146AA | DSI6_HV_R3: 0x400146AB |
| DSI6_HV_R4: 0x400146AC | DSI6_HV_R5: 0x400146AD |
| DSI6_HV_R6: 0x400146AE | DSI6_HV_R7: 0x400146AF |
| DSI6_HV_R8: 0x400146B0 | DSI6_HV_R9: 0x400146B1 |
| DSI6_HV_R10: 0x400146B2 | DSI6_HV_R11: 0x400146B3 |
| DSI6_HV_R12: 0x400146B4 | DSI6_HV_R13: 0x400146B5 |
| DSI6_HV_R14: 0x400146B6 | DSI6_HV_R15: 0x400146B7 |
| DSI7_HV_R0: 0x400147A8 | DSI7_HV_R1: 0x400147A9 |
| DSI7_HV_R2: 0x400147AA | DSI7_HV_R3: 0x400147AB |
| DSI7_HV_R4: 0x400147AC | DSI7_HV_R5: 0x400147AD |
| DSI7_HV_R6: 0x400147AE | DSI7_HV_R7: 0x400147AF |
| DSI7_HV_R8: 0x400147B0 | DSI7_HV_R9: 0x400147B1 |
| DSI7_HV_R10: 0x400147B2 | DSI7_HV_R11: 0x400147B3 |
| DSI7_HV_R12: 0x400147B4 | DSI7_HV_R13: 0x400147B5 |
| DSI7_HV_R14: 0x400147B6 | DSI7_HV_R15: 0x400147B7 |
| DSI8_HV_R0: 0x400148A8 | DSI8_HV_R1: 0x400148A9 |
| DSI8_HV_R2: 0x400148AA | DSI8_HV_R3: 0x400148AB |
| DSI8_HV_R4: 0x400148AC | DSI8_HV_R5: 0x400148AD |
| DSI8_HV_R6: 0x400148AE | DSI8_HV_R7: 0x400148AF |

1.3.1237 DSI[0..15]_HV_R[0..15] (continued)

Register : Address

| | |
|--------------------------|--------------------------|
| DSI8_HV_R8: 0x400148B0 | DSI8_HV_R9: 0x400148B1 |
| DSI8_HV_R10: 0x400148B2 | DSI8_HV_R11: 0x400148B3 |
| DSI8_HV_R12: 0x400148B4 | DSI8_HV_R13: 0x400148B5 |
| DSI8_HV_R14: 0x400148B6 | DSI8_HV_R15: 0x400148B7 |
| DSI9_HV_R0: 0x400149A8 | DSI9_HV_R1: 0x400149A9 |
| DSI9_HV_R2: 0x400149AA | DSI9_HV_R3: 0x400149AB |
| DSI9_HV_R4: 0x400149AC | DSI9_HV_R5: 0x400149AD |
| DSI9_HV_R6: 0x400149AE | DSI9_HV_R7: 0x400149AF |
| DSI9_HV_R8: 0x400149B0 | DSI9_HV_R9: 0x400149B1 |
| DSI9_HV_R10: 0x400149B2 | DSI9_HV_R11: 0x400149B3 |
| DSI9_HV_R12: 0x400149B4 | DSI9_HV_R13: 0x400149B5 |
| DSI9_HV_R14: 0x400149B6 | DSI9_HV_R15: 0x400149B7 |
| DSI12_HV_R0: 0x40014CA8 | DSI12_HV_R1: 0x40014CA9 |
| DSI12_HV_R2: 0x40014CAA | DSI12_HV_R3: 0x40014CAB |
| DSI12_HV_R4: 0x40014CAC | DSI12_HV_R5: 0x40014CAD |
| DSI12_HV_R6: 0x40014CAE | DSI12_HV_R7: 0x40014CAF |
| DSI12_HV_R8: 0x40014CB0 | DSI12_HV_R9: 0x40014CB1 |
| DSI12_HV_R10: 0x40014CB2 | DSI12_HV_R11: 0x40014CB3 |
| DSI12_HV_R12: 0x40014CB4 | DSI12_HV_R13: 0x40014CB5 |
| DSI12_HV_R14: 0x40014CB6 | DSI12_HV_R15: 0x40014CB7 |
| DSI13_HV_R0: 0x40014DA8 | DSI13_HV_R1: 0x40014DA9 |
| DSI13_HV_R2: 0x40014DAA | DSI13_HV_R3: 0x40014DAB |
| DSI13_HV_R4: 0x40014DAC | DSI13_HV_R5: 0x40014DAD |
| DSI13_HV_R6: 0x40014DAE | DSI13_HV_R7: 0x40014DAF |
| DSI13_HV_R8: 0x40014DB0 | DSI13_HV_R9: 0x40014DB1 |
| DSI13_HV_R10: 0x40014DB2 | DSI13_HV_R11: 0x40014DB3 |
| DSI13_HV_R12: 0x40014DB4 | DSI13_HV_R13: 0x40014DB5 |
| DSI13_HV_R14: 0x40014DB6 | DSI13_HV_R15: 0x40014DB7 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | hv_byte | | | | | | | |

DSI HV Tile Configuration

Register Segment: 2

1.3.1237 DSI[0..15]_HV_R[0..15] (continued)

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | hv_byte[7:0] | RAM configuration for DSI channel bytes |

1.3.1238 DSI[0..15]_DSIINP0

DSIINP0

Reset: N/A

Register : Address

| | |
|---------------------------|---------------------------|
| DSI0_DSIINP0: 0x400140C0 | DSI1_DSIINP0: 0x400141C0 |
| DSI2_DSIINP0: 0x400142C0 | DSI3_DSIINP0: 0x400143C0 |
| DSI4_DSIINP0: 0x400144C0 | DSI5_DSIINP0: 0x400145C0 |
| DSI6_DSIINP0: 0x400146C0 | DSI7_DSIINP0: 0x400147C0 |
| DSI8_DSIINP0: 0x400148C0 | DSI9_DSIINP0: 0x400149C0 |
| DSI12_DSIINP0: 0x40014CC0 | DSI13_DSIINP0: 0x40014DC0 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1239 DSI[0..15]_DSIINP1

DSIINP1

Reset: N/A

Register : Address

| | |
|---------------------------|---------------------------|
| DSI0_DSIINP1: 0x400140C2 | DSI1_DSIINP1: 0x400141C2 |
| DSI2_DSIINP1: 0x400142C2 | DSI3_DSIINP1: 0x400143C2 |
| DSI4_DSIINP1: 0x400144C2 | DSI5_DSIINP1: 0x400145C2 |
| DSI6_DSIINP1: 0x400146C2 | DSI7_DSIINP1: 0x400147C2 |
| DSI8_DSIINP1: 0x400148C2 | DSI9_DSIINP1: 0x400149C2 |
| DSI12_DSIINP1: 0x40014CC2 | DSI13_DSIINP1: 0x40014DC2 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1240 DSI[0..15]_DSIINP2

DSIINP2

Reset: N/A

Register : Address

| | |
|---------------------------|---------------------------|
| DSI0_DSIINP2: 0x400140C4 | DSI1_DSIINP2: 0x400141C4 |
| DSI2_DSIINP2: 0x400142C4 | DSI3_DSIINP2: 0x400143C4 |
| DSI4_DSIINP2: 0x400144C4 | DSI5_DSIINP2: 0x400145C4 |
| DSI6_DSIINP2: 0x400146C4 | DSI7_DSIINP2: 0x400147C4 |
| DSI8_DSIINP2: 0x400148C4 | DSI9_DSIINP2: 0x400149C4 |
| DSI12_DSIINP2: 0x40014CC4 | DSI13_DSIINP2: 0x40014DC4 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1241 DSI[0..15]_DSIINP3

DSIINP3

Reset: N/A

Register : Address

| | |
|---------------------------|---------------------------|
| DSI0_DSIINP3: 0x400140C6 | DSI1_DSIINP3: 0x400141C6 |
| DSI2_DSIINP3: 0x400142C6 | DSI3_DSIINP3: 0x400143C6 |
| DSI4_DSIINP3: 0x400144C6 | DSI5_DSIINP3: 0x400145C6 |
| DSI6_DSIINP3: 0x400146C6 | DSI7_DSIINP3: 0x400147C6 |
| DSI8_DSIINP3: 0x400148C6 | DSI9_DSIINP3: 0x400149C6 |
| DSI12_DSIINP3: 0x40014CC6 | DSI13_DSIINP3: 0x40014DC6 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1242 DSI[0..15]_DSIINP4

DSIINP4

Reset: N/A

Register : Address

DSI0_DSIINP4: 0x400140C8

DSI1_DSIINP4: 0x400141C8

DSI2_DSIINP4: 0x400142C8

DSI3_DSIINP4: 0x400143C8

DSI4_DSIINP4: 0x400144C8

DSI5_DSIINP4: 0x400145C8

DSI6_DSIINP4: 0x400146C8

DSI7_DSIINP4: 0x400147C8

DSI8_DSIINP4: 0x400148C8

DSI9_DSIINP4: 0x400149C8

DSI12_DSIINP4: 0x40014CC8

DSI13_DSIINP4: 0x40014DC8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1243 DSI[0..15]_DSIINP5

DSIINP5

Reset: N/A

Register : Address

| | |
|---------------------------|---------------------------|
| DSI0_DSIINP5: 0x400140CA | DSI1_DSIINP5: 0x400141CA |
| DSI2_DSIINP5: 0x400142CA | DSI3_DSIINP5: 0x400143CA |
| DSI4_DSIINP5: 0x400144CA | DSI5_DSIINP5: 0x400145CA |
| DSI6_DSIINP5: 0x400146CA | DSI7_DSIINP5: 0x400147CA |
| DSI8_DSIINP5: 0x400148CA | DSI9_DSIINP5: 0x400149CA |
| DSI12_DSIINP5: 0x40014CCA | DSI13_DSIINP5: 0x40014DCA |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1244 DSI[0..15]_DSIOUTP0

DSIOUTP0

Reset: N/A

Register : Address

DSI0_DSIOUTP0: 0x400140CC

DSI1_DSIOUTP0: 0x400141CC

DSI2_DSIOUTP0: 0x400142CC

DSI3_DSIOUTP0: 0x400143CC

DSI4_DSIOUTP0: 0x400144CC

DSI5_DSIOUTP0: 0x400145CC

DSI6_DSIOUTP0: 0x400146CC

DSI7_DSIOUTP0: 0x400147CC

DSI8_DSIOUTP0: 0x400148CC

DSI9_DSIOUTP0: 0x400149CC

DSI12_DSIOUTP0: 0x40014CCC

DSI13_DSIOUTP0: 0x40014DCC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1245 DSI[0..15]_DSIOUTP1

DSIOUTP1

Reset: N/A

Register : Address

| | |
|----------------------------|----------------------------|
| DSI0_DSIOUTP1: 0x400140CE | DSI1_DSIOUTP1: 0x400141CE |
| DSI2_DSIOUTP1: 0x400142CE | DSI3_DSIOUTP1: 0x400143CE |
| DSI4_DSIOUTP1: 0x400144CE | DSI5_DSIOUTP1: 0x400145CE |
| DSI6_DSIOUTP1: 0x400146CE | DSI7_DSIOUTP1: 0x400147CE |
| DSI8_DSIOUTP1: 0x400148CE | DSI9_DSIOUTP1: 0x400149CE |
| DSI12_DSIOUTP1: 0x40014CCE | DSI13_DSIOUTP1: 0x40014DCE |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1246 DSI[0..15]_DSIOUTP2

DSIOUTP2

Reset: N/A

Register : Address

DSI0_DSIOUTP2: 0x400140D0

DSI1_DSIOUTP2: 0x400141D0

DSI2_DSIOUTP2: 0x400142D0

DSI3_DSIOUTP2: 0x400143D0

DSI4_DSIOUTP2: 0x400144D0

DSI5_DSIOUTP2: 0x400145D0

DSI6_DSIOUTP2: 0x400146D0

DSI7_DSIOUTP2: 0x400147D0

DSI8_DSIOUTP2: 0x400148D0

DSI9_DSIOUTP2: 0x400149D0

DSI12_DSIOUTP2: 0x40014CD0

DSI13_DSIOUTP2: 0x40014DD0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1247 DSI[0..15]_DSIOUTP3

DSIOUTP3

Reset: N/A

Register : Address

| | |
|---------------------------|----------------------------|
| DSI0_DSIOUTP3: 0x400140D2 | DSI11_DSIOUTP3: 0x40014CD2 |
| DSI2_DSIOUTP3: 0x400142D2 | DSI12_DSIOUTP3: 0x40014DD2 |
| DSI4_DSIOUTP3: 0x400144D2 | DSI13_DSIOUTP3: 0x40014E2 |
| DSI6_DSIOUTP3: 0x400146D2 | |
| DSI8_DSIOUTP3: 0x400148D2 | |
| | |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1248 DSI[0..15]_DSIOUTT0

DSIOUTT0

Reset: N/A

Register : Address

DSI0_DSIOUTT0: 0x400140D4

DSI1_DSIOUTT0: 0x400141D4

DSI2_DSIOUTT0: 0x400142D4

DSI3_DSIOUTT0: 0x400143D4

DSI4_DSIOUTT0: 0x400144D4

DSI5_DSIOUTT0: 0x400145D4

DSI6_DSIOUTT0: 0x400146D4

DSI7_DSIOUTT0: 0x400147D4

DSI8_DSIOUTT0: 0x400148D4

DSI9_DSIOUTT0: 0x400149D4

DSI12_DSIOUTT0: 0x40014CD4

DSI13_DSIOUTT0: 0x40014DD4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1249 DSI[0..15]_DSIOUTT1

DSIOUTT1

Reset: N/A

Register : Address

| | |
|---------------------------|----------------------------|
| DSI0_DSIOUTT1: 0x400140D6 | DSI11_DSIOUTT1: 0x40014CD6 |
| DSI2_DSIOUTT1: 0x400142D6 | DSI12_DSIOUTT1: 0x40014DD6 |
| DSI4_DSIOUTT1: 0x400144D6 | DSI13_DSIOUTT1: 0x40014E6 |
| DSI6_DSIOUTT1: 0x400146D6 | |
| DSI8_DSIOUTT1: 0x400148D6 | |
| | |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1250 DSI[0..15]_DSIOUTT2

DSIOUTT2

Reset: N/A

Register : Address

DSI0_DSIOUTT2: 0x400140D8

DSI1_DSIOUTT2: 0x400141D8

DSI2_DSIOUTT2: 0x400142D8

DSI3_DSIOUTT2: 0x400143D8

DSI4_DSIOUTT2: 0x400144D8

DSI5_DSIOUTT2: 0x400145D8

DSI6_DSIOUTT2: 0x400146D8

DSI7_DSIOUTT2: 0x400147D8

DSI8_DSIOUTT2: 0x400148D8

DSI9_DSIOUTT2: 0x400149D8

DSI12_DSIOUTT2: 0x40014CD8

DSI13_DSIOUTT2: 0x40014DD8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1251 DSI[0..15]_DSIOUTT3

DSIOUTT3

Reset: N/A

Register : Address

| | |
|----------------------------|----------------------------|
| DSI0_DSIOUTT3: 0x400140DA | DSI1_DSIOUTT3: 0x400141DA |
| DSI2_DSIOUTT3: 0x400142DA | DSI3_DSIOUTT3: 0x400143DA |
| DSI4_DSIOUTT3: 0x400144DA | DSI5_DSIOUTT3: 0x400145DA |
| DSI6_DSIOUTT3: 0x400146DA | DSI7_DSIOUTT3: 0x400147DA |
| DSI8_DSIOUTT3: 0x400148DA | DSI9_DSIOUTT3: 0x400149DA |
| DSI12_DSIOUTT3: 0x40014CDA | DSI13_DSIOUTT3: 0x40014DDA |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1252 DSI[0..15]_DSIOUTT4

DSIOUTT4

Reset: N/A

Register : Address

DSI0_DSIOUTT4: 0x400140DC

DSI1_DSIOUTT4: 0x400141DC

DSI2_DSIOUTT4: 0x400142DC

DSI3_DSIOUTT4: 0x400143DC

DSI4_DSIOUTT4: 0x400144DC

DSI5_DSIOUTT4: 0x400145DC

DSI6_DSIOUTT4: 0x400146DC

DSI7_DSIOUTT4: 0x400147DC

DSI8_DSIOUTT4: 0x400148DC

DSI9_DSIOUTT4: 0x400149DC

DSI12_DSIOUTT4: 0x40014CDC

DSI13_DSIOUTT4: 0x40014DDC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1253 DSI[0..15]_DSIOUTT5

DSIOUTT5

Reset: N/A

Register : Address

| | |
|----------------------------|----------------------------|
| DSI0_DSIOUTT5: 0x400140DE | DSI1_DSIOUTT5: 0x400141DE |
| DSI2_DSIOUTT5: 0x400142DE | DSI3_DSIOUTT5: 0x400143DE |
| DSI4_DSIOUTT5: 0x400144DE | DSI5_DSIOUTT5: 0x400145DE |
| DSI6_DSIOUTT5: 0x400146DE | DSI7_DSIOUTT5: 0x400147DE |
| DSI8_DSIOUTT5: 0x400148DE | DSI9_DSIOUTT5: 0x400149DE |
| DSI12_DSIOUTT5: 0x40014CDE | DSI13_DSIOUTT5: 0x40014DDE |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | pi_bot | | | | pi_top | | | |

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7:4 | pi_bot[3:0] | RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks |
| 3:0 | pi_top[3:0] | RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks |

1.3.1254 DSI[0..15]_VS0

VS0

Reset: N/A

Register : Address

| | |
|-----------------------|-----------------------|
| DSI0_VS0: 0x400140E0 | DSI1_VS0: 0x400141E0 |
| DSI2_VS0: 0x400142E0 | DSI3_VS0: 0x400143E0 |
| DSI4_VS0: 0x400144E0 | DSI5_VS0: 0x400145E0 |
| DSI6_VS0: 0x400146E0 | DSI7_VS0: 0x400147E0 |
| DSI8_VS0: 0x400148E0 | DSI9_VS0: 0x400149E0 |
| DSI12_VS0: 0x40014CE0 | DSI13_VS0: 0x40014DE0 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks |
| 3:0 | vs_top[3:0] | RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks |

1.3.1255 DSI[0..15]_VS1

VS1

Reset: N/A

Register : Address

| | |
|-----------------------|-----------------------|
| DSI0_VS1: 0x400140E2 | DSI1_VS1: 0x400141E2 |
| DSI2_VS1: 0x400142E2 | DSI3_VS1: 0x400143E2 |
| DSI4_VS1: 0x400144E2 | DSI5_VS1: 0x400145E2 |
| DSI6_VS1: 0x400146E2 | DSI7_VS1: 0x400147E2 |
| DSI8_VS1: 0x400148E2 | DSI9_VS1: 0x400149E2 |
| DSI12_VS1: 0x40014CE2 | DSI13_VS1: 0x40014DE2 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks |
| 3:0 | vs_top[3:0] | RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks |

1.3.1256 DSI[0..15]_VS2

VS2

Reset: N/A

Register : Address

| | |
|-----------------------|-----------------------|
| DSI0_VS2: 0x400140E4 | DSI1_VS2: 0x400141E4 |
| DSI2_VS2: 0x400142E4 | DSI3_VS2: 0x400143E4 |
| DSI4_VS2: 0x400144E4 | DSI5_VS2: 0x400145E4 |
| DSI6_VS2: 0x400146E4 | DSI7_VS2: 0x400147E4 |
| DSI8_VS2: 0x400148E4 | DSI9_VS2: 0x400149E4 |
| DSI12_VS2: 0x40014CE4 | DSI13_VS2: 0x40014DE4 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks |
| 3:0 | vs_top[3:0] | RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks |

1.3.1257 DSI[0..15]_VS3

VS3

Reset: N/A

Register : Address

| | |
|-----------------------|-----------------------|
| DSI0_VS3: 0x400140E6 | DSI1_VS3: 0x400141E6 |
| DSI2_VS3: 0x400142E6 | DSI3_VS3: 0x400143E6 |
| DSI4_VS3: 0x400144E6 | DSI5_VS3: 0x400145E6 |
| DSI6_VS3: 0x400146E6 | DSI7_VS3: 0x400147E6 |
| DSI8_VS3: 0x400148E6 | DSI9_VS3: 0x400149E6 |
| DSI12_VS3: 0x40014CE6 | DSI13_VS3: 0x40014DE6 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks |
| 3:0 | vs_top[3:0] | RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks |

1.3.1258 DSI[0..15]_VS4

VS4

Reset: N/A

Register : Address

| | |
|-----------------------|-----------------------|
| DSI0_VS4: 0x400140E8 | DSI1_VS4: 0x400141E8 |
| DSI2_VS4: 0x400142E8 | DSI3_VS4: 0x400143E8 |
| DSI4_VS4: 0x400144E8 | DSI5_VS4: 0x400145E8 |
| DSI6_VS4: 0x400146E8 | DSI7_VS4: 0x400147E8 |
| DSI8_VS4: 0x400148E8 | DSI9_VS4: 0x400149E8 |
| DSI12_VS4: 0x40014CE8 | DSI13_VS4: 0x40014DE8 |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks |
| 3:0 | vs_top[3:0] | RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks |

1.3.1259 DSI[0..15]_VS5

VS5

Reset: N/A

Register : Address

| | |
|-----------------------|-----------------------|
| DSI0_VS5: 0x400140EA | DSI1_VS5: 0x400141EA |
| DSI2_VS5: 0x400142EA | DSI3_VS5: 0x400143EA |
| DSI4_VS5: 0x400144EA | DSI5_VS5: 0x400145EA |
| DSI6_VS5: 0x400146EA | DSI7_VS5: 0x400147EA |
| DSI8_VS5: 0x400148EA | DSI9_VS5: 0x400149EA |
| DSI12_VS5: 0x40014CEA | DSI13_VS5: 0x40014DEA |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks |
| 3:0 | vs_top[3:0] | RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks |

1.3.1260 DSI[0..15]_VS6

VS6

Reset: N/A

Register : Address

DSI0_VS6: 0x400140EC

DSI1_VS6: 0x400141EC

DSI2_VS6: 0x400142EC

DSI3_VS6: 0x400143EC

DSI4_VS6: 0x400144EC

DSI5_VS6: 0x400145EC

DSI6_VS6: 0x400146EC

DSI7_VS6: 0x400147EC

DSI8_VS6: 0x400148EC

DSI9_VS6: 0x400149EC

DSI12_VS6: 0x40014CEC

DSI13_VS6: 0x40014DEC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks |
| 3:0 | vs_top[3:0] | RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks |

1.3.1261 DSI[0..15]_VS7

VS7

Reset: N/A

Register : Address

| | |
|-----------------------|-----------------------|
| DSI0_VS7: 0x400140EE | DSI1_VS7: 0x400141EE |
| DSI2_VS7: 0x400142EE | DSI3_VS7: 0x400143EE |
| DSI4_VS7: 0x400144EE | DSI5_VS7: 0x400145EE |
| DSI6_VS7: 0x400146EE | DSI7_VS7: 0x400147EE |
| DSI8_VS7: 0x400148EE | DSI9_VS7: 0x400149EE |
| DSI12_VS7: 0x40014CEE | DSI13_VS7: 0x40014DEE |

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R/W:UUUU | | | | R/W:UUUU | | | |
| HW Access | R | | | | R | | | |
| Name | vs_bot | | | | vs_top | | | |

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Register Segment: 2

| Bits | Name | Description |
|------|-------------|---|
| 7:4 | vs_bot[3:0] | RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks |
| 3:0 | vs_top[3:0] | RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks |

1.3.1262 BCTL[0..3]_MDCLK_EN

MDCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_MDCLK_EN: 0x40015000

BCTL1_MDCLK_EN: 0x40015010

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | DCEN7 | DCEN6 | DCEN5 | DCEN4 | DCEN3 | DCEN2 | DCEN1 | DCEN0 |

Master Digital Global Clock Enable Register

Register Segment: 2

| Bits | Name | Description |
|------|-------|---|
| 7 | DCEN7 | Bank Clock Enable Control See Table 1-850. |
| 6 | DCEN6 | Bank Clock Enable Control See Table 1-850. |
| 5 | DCEN5 | Bank Clock Enable Control See Table 1-850. |
| 4 | DCEN4 | Bank Clock Enable Control See Table 1-850. |
| 3 | DCEN3 | Bank Clock Enable Control See Table 1-850. |
| 2 | DCEN2 | Bank Clock Enable Control See Table 1-850. |
| 1 | DCEN1 | Bank Clock Enable Control See Table 1-850. |
| 0 | DCEN0 | Bank Clock Enable Control See Table 1-850. |

Table 1-850. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | DISABLE | Digital Global clock is disabled. |
| 1'b1 | ENABLE | Digital Global clock is enabled. |

1.3.1263 BCTL[0..3]_MBCLK_EN

MBCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_MBCLK_EN: 0x40015001

BCTL1_MBCLK_EN: 0x40015011

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|-----------------|------------------|-------------------|---------------|---------------|------------------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | USCAN_M ODE | SCAN_DRV _EN | CHAN_DRV _DIS | SA1_DSI_P D_EN | SA1_PD_E N | SA1_PU_E N | RDWR_RA M_OPT | BCEN |

Master Digital Global Clock Enable Register

Register Segment: 2

| Bits | Name | Description |
|------|---------------|---|
| 7 | USCAN_MODE | Test only: Used for UDB DFT operation. Enable UDB scan mode. When this bit is set, UDB scan operation is controlled by the UDBIF See Table 1-858. |
| 6 | SCAN_DRV_EN | Test only: Used for UDB DFT operation. Enables scan flip flops on DSI inputs to drive test data to the routing inputs (DSI VROUTES). DSI input drivers (PI memory bits) must be OFF for this test. This bit also qualifies the USCAN_SE bit to control shifts of the bypass scan chain used to select DSI blocks to be scanned or bypassed. See Table 1-857. |
| 5 | CHAN_DRV_DIS | Test only: Disables all UDB output drivers to the routing matrix. Supports SA1 routing matrix switch control testing. See Table 1-851. |
| 4 | SA1_DSI_PD_EN | Test only: Enables weak pulldown on all DSI outputs. Supports SA1 DSI output buffer control control testing. See Table 1-854. |
| 3 | SA1_PD_EN | Test only: Enables weak pulldown on all vertical routes. Supports SA1 routing matrix buffer and switch control testing. See Table 1-855. |
| 2 | SA1_PU_EN | Test only: Enables strong pullup on horizontal routes that traverse the System Interface. Note: Need horizontal segmentation buffers on to drive strong to all horizontal routes. Supports SA1 routing matrix switch control testing. See Table 1-856. |
| 1 | RDWR_RAM_OPT | Test only: Controls the generation of the internal RAM read and write signals See Table 1-853. |
| 0 | BCEN | Bank Clock Enable Control See Table 1-852. |

1.3.1263 BCTL[0..3]_MBCLK_EN (continued)

Table 1-851. Bit field encoding: CHAN_DRV_DIS_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | ENABLE | Normal Operation, UDB drivers are enabled. |
| 1'b1 | DISABLE | UDB output drivers to routing are disabled. |

Table 1-852. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | DISABLE | Digital Global clock is disabled. |
| 1'b1 | ENABLE | Digital Global clock is enabled. |

Table 1-853. Bit field encoding: RDWR_RAM_OPT_ENUM

| Value | Name | Description |
|-------|--------------|---|
| 1'b0 | NEG_EDGE_GEN | RAM read/write signal is generated from the negative edge of bus clock. When this bit is zero single cycle configuration reads/writes are not available |
| 1'b1 | POS_EDGE_GEN | RAM read/write signal is generated from the positive edge of bus clock |

Table 1-854. Bit field encoding: SA1_DSI_PD_EN_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Normal Operation, weak pulldown disabled. |
| 1'b1 | ENABLE | Weak pulldown enabled. |

Table 1-855. Bit field encoding: SA1_PD_EN_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Normal Operation, weak pulldown disabled. |
| 1'b1 | ENABLE | Weak pulldown enabled. |

Table 1-856. Bit field encoding: SA1_PU_EN_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Normal Operation, strong pullup disabled. |
| 1'b1 | ENABLE | Strong pullup enabled. |

Table 1-857. Bit field encoding: SCAN_DRV_EN_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | Normal Operation, DSI input scan drivers are disabled. Bypass scan chain holds current data. |
| 1'b1 | ENABLE | DSI input scan drivers are enabled. Bypass scan chain will shift depending upon state of USCAN_SE. |

Table 1-858. Bit field encoding: SCAN_MODE_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | UDB DSI scan is used by full chip scan controller. |
| 1'b1 | ENABLE | UDB DSI scan is controlled by UDBIF interface. |

1.3.1264 BCTL[0..3]_WAIT_CFG

WAIT_CFG

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_WAIT_CFG: 0x40015002

BCTL1_WAIT_CFG: 0x40015012

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|-------------|---|-------------|---|-------------|---|
| SW Access:Reset | R/W:00 | | R/W:00 | | R/W:00 | | R/W:00 | |
| HW Access | R | | R | | R | | R | |
| Name | WR_WRK_WAIT | | RD_WRK_WAIT | | WR_CFG_WAIT | | RD_CFG_WAIT | |

Wait State Configuration Register

Register Segment: 2

| Bits | Name | Description |
|------|------------------|---|
| 7:6 | WR_WRK_WAIT[1:0] | Wait States for Writing UDB Working Registers See Table 1-862. |
| 5:4 | RD_WRK_WAIT[1:0] | Wait States for Reading UDB Working Registers See Table 1-860. |
| 3:2 | WR_CFG_WAIT[1:0] | Wait States for Writing UDB Configuration See Table 1-861. |
| 1:0 | RD_CFG_WAIT[1:0] | Wait States for Reading UDB Configuration See Table 1-859. |

Table 1-859. Bit field encoding: RD_CFG_WAIT_ENUM

| Value | Name | Description |
|-------|-------------|---------------|
| 2'b00 | FIVE_WAITS | 5 wait states |
| 2'b01 | FOUR_WAITS | 4 wait state |
| 2'b10 | THREE_WAITS | 3 wait states |
| 2'b11 | ONE_WAITS | 1 wait states |

Table 1-860. Bit field encoding: RD_WRK_WAIT_ENUM

| Value | Name | Description |
|-------|-------------|---------------|
| 2'b00 | ONE_WAITS | 1 wait states |
| 2'b01 | TWO_WAITS | 2 wait state |
| 2'b10 | THREE_WAITS | 3 wait states |
| 2'b11 | ZERO_WAITS | 0 wait states |

Table 1-861. Bit field encoding: WR_CFG_WAIT_ENUM

| Value | Name | Description |
|-------|-------------|---|
| 2'b00 | ONE_WAITS | 1 wait state |
| 2'b01 | TWO_WAITS | 2 wait states |
| 2'b10 | THREE_WAITS | 3 wait states |
| 2'b11 | ILLEGAL | Unsupported configuration value. Use of this value will cause device to fail. |

1.3.1264 BCTL[0..3]_WAIT_CFG (continued)

Table 1-862. Bit field encoding: WR_WRK_WAIT_ENUM

| Value | Name | Description |
|-------|-------------|---------------|
| 2'b00 | ONE_WAITS | 1 wait states |
| 2'b01 | TWO_WAITS | 2 wait state |
| 2'b10 | THREE_WAITS | 3 wait states |
| 2'b11 | ZERO_WAITS | 0 wait states |

1.3.1265 BCTL[0..3]_BANK_CTL

BANK_CTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_BANK_CTL: 0x40015003

BCTL1_BANK_CTL: 0x40015013

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|----------|-------------|-----------|---------|-----------|---------------|---------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R/W | R | R | R | R | R | R | R |
| Name | USCAN_CLK | USCAN_SE | USCAN_RESET | USCAN_SET | GLBL_WR | DPARAM_TM | ROUTE_ENABLED | DIS_COR |

Bank Control Register

Register Segment: 2

| Bits | Name | Description |
|------|-------------|--|
| 7 | USCAN_CLK | Test only: Used for UDB DFT operation. Controls the scan clock to the UDB DSI scan chain, when USCAN MODE is enabled. See Table 1-867. |
| 6 | USCAN_SE | Test only: Used for UDB DFT operation. Controls the shift enable to the UDB DSI scan chain, when USCAN MODE is enabled. See Table 1-870. |
| 5 | USCAN_RESET | Test only: Used for UDB DFT operation. Asserts a RESET to all UDBs in the DSI scan chain in this bank. See Table 1-868. |
| 4 | USCAN_SET | Test only: Used for UDB DFT operation. Asserts a SET to all UDBs in the DSI scan chain this bank, when USCAN_MODE is enabled. See Table 1-869. |
| 3 | GLBL_WR | Global Write Test Mode: The purpose of this bit is to accelerate configuration and working register writing for test purposes. When this bit is set, the bank is in global write mode. In this mode a set of UDBs or UDB channels are selected for writing in parallel based on the setting of the GUDB WR bits and GCH WR bits in the individual UDB. See Table 1-865. |
| 2 | DPARAM_TM | DPARAM Test Mode: The DP RAM (s8dparam_ram16x8) has two read ports, one connected to the system bus (for configuration of the RAM), and one port that drives the DP control bits. When this bit is set, the DP RAM control port is connected to the system bus for reading (the system bus read port is tri-stated) See Table 1-864. |

1.3.1265 BCTL[0..3]_BANK_CTL (continued)

1 ROUTE_ENABLE Route Enable: When this bit is a 0, all routing drivers are gated off to drive '0'. This results in nets either at 'Z' or '0' state and prevents driver conflicts with random configuration RAM on POR. This bit also controls gating of buffer inputs to prevent high current states in the case of 'Z' nets. After configuration, this bit may be enabled.

[See Table 1-866.](#)

0 DIS_COR Disable Clear On Read: The status registers have an automatic clear on read function to maintain firmware synchronization with UDB processing. When the system is stopped in debug mode, this bit can be used to prevent the status from clearing on a debug read. It also prevents a read pop from the FIFO blocks. Only the top of FIFO can be read when this bit is set.

[See Table 1-863.](#)

Table 1-863. Bit field encoding: COR_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | ENABLE | Status register clear on read enabled. (default) |
| 1'b1 | DISABLE | Status register clear on read disabled. |

Table 1-864. Bit field encoding: DPARAM_TM_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | DPARAM test mode is disabled. (default) |
| 1'b1 | ENABLE | DPARAM test mode is enabled. |

Table 1-865. Bit field encoding: GLBL_WR_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Global Write Test Mode is disabled. (default) |
| 1'b1 | ENABLE | Global Write Test Mode enabled. |

Table 1-866. Bit field encoding: ROUTE_ENABLE

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | Routing input drivers are gated off to '0' (default) |
| 1'b1 | ENABLE | Routing input drivers are enabled. |

Table 1-867. Bit field encoding: USCAN_CLK_ENUM

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | UDB DSI scan clk is idle |
| 1'b1 | ENABLE | UDB DSI scan clk asserted for 1 clock pulse if USCAN_SE = 0 (capture mode) or for 32 clock pulses if USCAN_SE = 1 (shift mode). Register bit auto-clears after one clock. |

Table 1-868. Bit field encoding: USCAN_RES_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | RESET is not asserted to the UDB DSI scan registers. |
| 1'b1 | ENABLE | RESET is asserted to the UDB DSI scan registers. |

Table 1-869. Bit field encoding: USCAN_SET_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | SET is not asserted to the UDB DSI scan registers. |
| 1'b1 | ENABLE | SET is asserted to the UDB DSI scan registers. |

Table 1-870. Bit field encoding: USCAN_SE_ENUM

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | UDB DSI scan chain is in capture mode. |
| 1'b1 | ENABLE | UDB DSI scan chain is in shift mode. |

1.3.1266 BCTL[0..3]_UDB_TEST_0

UDB_TEST_0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_UDB_TEST_0: 0x40015004

BCTL1_UDB_TEST_0: 0x40015014

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11111111 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | TEST_CRC_OUT_L | | | | | | | |

UDB Test Register 0

Register Segment: 2

| Bits | Name | Description |
|------|---------------------|---|
| 7:0 | TEST_CRC_OUT_L[7:0] | Test only: Low byte result (7:0) of CRC for UDB DFT vectors |

1.3.1267 BCTL[0..3]_UDB_TEST_1

UDB_TEST_1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_UDB_TEST_1: 0x40015005

BCTL1_UDB_TEST_1: 0x40015015

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11111111 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | TEST_CRC_OUT_H | | | | | | | |

UDB Test Register 1

Register Segment: 2

| Bits | Name | Description |
|------|---------------------|--|
| 7:0 | TEST_CRC_OUT_H[7:0] | Test only: High byte result (15:8) of CRC result for UDB DFT vectors |

1.3.1268 BCTL[0..3]_UDB_TEST_2

UDB_TEST_2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_UDB_TEST_2: 0x40015006

BCTL1_UDB_TEST_2: 0x40015016

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---------|---------------|---|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:000000 | | | | | |
| HW Access | R | R/W | R | | | | | |
| Name | CRC_EN | CRC_RST | TEST_CHAIN_IN | | | | | |

UDB Test Register 2

Register Segment: 2

| Bits | Name | Description |
|------|--------------------|--|
| 7 | CRC_EN | Test only: Enable CRC processing in UDBIF to compute CRC on UDB DFT vectors. See Table 1-871. |
| 6 | CRC_RST | Test only: Reset the CRC block in the UDBIF. LFSR register bits are reset to original seed value (0xffff) See Table 1-872. |
| 5:0 | TEST_CHAIN_IN[5:0] | Test only: Inputs to OR reduction chains to support SA1 control testing. There are 6 chains for a given array consisting of 32 UDBs or less. Each DSI has one OR chain, and each UDB channel has 2 OR chains. Bit 0 is connected to the bottom DSI chain, bit 1 to the lower UDB bottom, bit 2 to the lower UDB top, bit 3 to the upper UDB bottom, bit 4 to the upper UDB top, and bit 5 to the top DSI chain. BCTL0_UDB_TEST_2 drives the S8UDB array. BCTL1_UDB_TEST_2 is not used. |

Table 1-871. Bit field encoding: CRC_EN_ENUM

| Value | Name | Description |
|-------|---------|------------------|
| 1'b0 | DISABLE | CRC is disabled. |
| 1'b1 | ENABLE | CRC is enabled. |

Table 1-872. Bit field encoding: CRC_RST_ENUM

| Value | Name | Description |
|-------|------------------|---|
| 1'b0 | NORMAL_OPERATION | CRC is not in reset state. |
| 1'b1 | RESET | CRC is reset. Register bit auto-clears after one clock. |

1.3.1269 BCTL[0..3]_UDB_TEST_3

UDB_TEST_3

Reset: Reset Signals Listed Below

Register : Address

BCTL0_UDB_TEST_3: 0x40015007

BCTL1_UDB_TEST_3: 0x40015017

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|----------|----------------|---|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0 | R:UUUUUU | | | | | |
| HW Access | R | R | W | | | | | |
| Name | WRITE2READ | USCAN_SI | TEST_CHAIN_OUT | | | | | |

UDB Test Register 3

Register Segment: 2

| Bits | Name | Description |
|------|---------------------|---|
| 7 | WRITE2READ | Test only: Convert a UDB Array write to a read in the UDBIF. When this bit is set, any writes to the UDB Array address spaces are converted to reads. Used to reduce register test time. Note: This register may still be written when this bit is set. For this address only, a write operation translated into a read operation as a result of this bit being set is converted back into a write. This allows the mode to be exited. However, an intentional read of this register with this bit set will also be translated into a write and will load this bit and the USCAN_SI bit with what is on the data bus. See Table 1-874. |
| 6 | USCAN_SI | Test Only: Used for UDB DFT operation. This bit is the source for the scan data in, when USCAN MODE is enabled. A write to this register with USCAN_MODE and USCAN_SE set will generate a single scan clock pulse which will result in the USCAN_SI value being shifted into the UDB DSI scan chain. This method is used for loading arbitrary values into the DSI scan chain. See Table 1-873. |
| 5:0 | TEST_CHAIN_OUT[5:0] | Test only: Outputs from OR reduction chains to support SA1 control testing. There are 6 chains for a given array consisting of 32 UDBs or less. Each DSI has one OR chain, and each UDB channel has 2 OR chains. Bit 0 is connected to the bottom DSI chain, bit 1 to the lower UDB bottom, bit 2 to the lower UDB top, bit 3 to the upper UDB bottom, bit 4 to the upper UDB top, and bit 5 to the top DSI chain. BCTL0_UDB_TEST_3 receives the S8UDB array outputs. Inputs to BCTL1_UDB_TEST_3 are grounded. |

Reset Table

| resetsignal | field(s) |
|--|----------------------|
| N/A | TEST_CHAIN_OUT[5:0] |
| System reset for retention flops [reset_all_retention] | USCAN_SI, WRITE2READ |

1.3.1269 BCTL[0..3]_UDB_TEST_3 (continued)

Table 1-873. Bit field encoding: USCAN_SI_ENUM

| Value | Name | Description |
|-------|------------|---|
| 1'b0 | DISABLED_0 | Bus clock enable is not pipelined. UDB DSI scan in data is 0. |
| 1'b1 | ENABLED_1 | Bus clock enable is pipelined. UDB DSI scan in data is 1. |

Table 1-874. Bit field encoding: WRITE_2_READ_ENUM

| Value | Name | Description |
|-------|------------------|--------------------------------|
| 1'b0 | NORMAL_OPERATION | Writes are executed normally. |
| 1'b1 | WRITE_2_READ | Writes are converted to reads. |

1.3.1270 BCTL[0..3]_DCLK_EN0

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN0: 0x40015008

BCTL1_DCLK_EN0: 0x40015018

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | DCEN7 | DCEN6 | DCEN5 | DCEN4 | DCEN3 | DCEN2 | DCEN1 | DCEN0 |

Digital Global Clock Enable Register

Register Segment: 2

| Bits | Name | Description |
|------|-------|---|
| 7 | DCEN7 | Bank Clock Enable Control See Table 1-875. |
| 6 | DCEN6 | Bank Clock Enable Control See Table 1-875. |
| 5 | DCEN5 | Bank Clock Enable Control See Table 1-875. |
| 4 | DCEN4 | Bank Clock Enable Control See Table 1-875. |
| 3 | DCEN3 | Bank Clock Enable Control See Table 1-875. |
| 2 | DCEN2 | Bank Clock Enable Control See Table 1-875. |
| 1 | DCEN1 | Bank Clock Enable Control See Table 1-875. |
| 0 | DCEN0 | Bank Clock Enable Control See Table 1-875. |

Table 1-875. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | DISABLE | Digital Global clock is disabled. |
| 1'b1 | ENABLE | Digital Global clock is enabled. |

1.3.1271 BCTL[0..3]_BCLK_EN0

BCLK_EN

Reset: Reset Signals Listed Below

Register : Address

BCTL0_BCLK_EN0: 0x40015009

BCTL1_BCLK_EN0: 0x40015019

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|-------|------------|------------|----------------|-----------|-----------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | SLEEP_TEST | NC0 | WR_CFG_OPT | GLB_DSI_WR | DISABLE_R_OUTE | GCH_WR_HI | GCH_WR_LO | BCEN |

Bus Clock Enable Register

Register Segment: 2

| Bits | Name | Description |
|------|------------|---|
| 7 | SLEEP_TEST | <p>Assertion of this bit drives sleep into the s8udb array for internal s8udb test purposes. Assertion does not affect the power switches. This signal drives pulldowns on the write strobes for all configuration memory, inhibiting writes when set. Sleep or sleep_test does not inhibit writes to this bit, allowing it to be cleared once it has been set. Control is split top and bottom.</p> <p>BCTL0_BCLK_EN0 controls Bank 0 UDB pairs 0-3 and DSI blocks 0-3. BCTL0_BCLK_EN3 controls Bank 0 UDB pairs 4-7 and DSI blocks 4-7. BCTL1_BCLK_EN1 controls Bank 1 UDB pairs 2-3 and DSI blocks 8-9. BCTL1_BCLK_EN2 controls Bank 1 UDB pairs 4-5 and DSI blocks 12-13. The SLEEP_TEST bits in the other BCTLx_BCLK_ENy registers are not used. Sleep assertion drives bus_data to zero so bus read transactions will not return data during assertion of certain sleep_test bits. This is only true for assertion of sleep_test in BCTL0_BCLK_EN0 for Bank 0 and BCTL1_BCLK_EN1 for Bank1.</p> <p>See Table 1-881.</p> |
| 6 | NC0 | Spare register bit |
| 5 | WR_CFG_OPT | <p>Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. BCTL1_BCLK_EN1 controls this bit for Bank 1. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used.</p> <p>See Table 1-882.</p> |
| 4 | GLB_DSI_WR | <p>Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. BCTL1_BCLK_EN1 controls DSI blocks 8-9. BCTL1_BCLK_EN2 controls DSI blocks 12-13. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used.</p> <p>See Table 1-880.</p> |

1.3.1271 BCTL[0..3]_BCLK_EN0 (continued)

| | | |
|---|---------------|---|
| 3 | DISABLE_ROUTE | By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-877. |
| 2 | GCH_WR_HI | Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-878. |
| 1 | GCH_WR_LO | Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-879. |
| 0 | BCEN | Bank Clock Enable Control See Table 1-876. |

Reset Table

| resetsignal | field(s) |
|--|--|
| System reset for retention flops [reset_all_retention] | BCEN, GCH_WR_LO, GCH_WR_HI, DISABLE_ROUTE, GLB_DSI_WR, WR_CFG_OPT, NC0 |
| Domain reset for non-retention flops [reset_all_nonretention] | SLEEP_TEST |

Table 1-876. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | DISABLE | Digital Global clock is disabled. |
| 1'b1 | ENABLE | Digital Global clock is enabled. |

Table 1-877. Bit field encoding: DIS_ROUTE

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | ENABLE | The routing in this quadrant can be enabled with the bank route enable bit. (default) |
| 1'b1 | DISABLE | The routing in this quadrant is disabled and held in a benign state. |

Table 1-878. Bit field encoding: GCH_WR_HI

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | Global UDB channel configuration write for higher order address is disabled. |
| 1'b1 | ENABLE | Global UDB channel configuration write for higher order address is enabled. |

Table 1-879. Bit field encoding: GCH_WR_LO

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Global UDB channel configuration write for lower order address is disabled. |
| 1'b1 | ENABLE | Global UDB channel configuration write for lower order address is enabled. |

Table 1-880. Bit field encoding: GLB_DSI_WR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1271 BCTL[0..3]_BCLK_EN0 (continued)

Table 1-880. Bit field encoding: GLB_DSI_WR

| | | |
|------|---------|---|
| 1'b0 | DISABLE | Global DSI channel configuration write is disabled. |
| 1'b1 | ENABLE | Global DSI channel configuration write is enabled. |

Table 1-881. Bit field encoding: SLEEP_TEST_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------|
| 1'b0 | DISABLE | sleep_test is not asserted. |
| 1'b1 | ENABLE | sleep_test is asserted. |

Table 1-882. Bit field encoding: WR_CFG_OPT_ENUM

| Value | Name | Description |
|-------|----------------|--|
| 1'b0 | FULL_CYCLE_STB | bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. |
| 1'b1 | HALF_CYCLE_STB | bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk. |

1.3.1272 BCTL[0..3]_DCLK_EN1

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN1: 0x4001500A

BCTL1_DCLK_EN1: 0x4001501A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | DCEN7 | DCEN6 | DCEN5 | DCEN4 | DCEN3 | DCEN2 | DCEN1 | DCEN0 |

Digital Global Clock Enable Register

Register Segment: 2

| Bits | Name | Description |
|------|-------|---|
| 7 | DCEN7 | Bank Clock Enable Control See Table 1-883. |
| 6 | DCEN6 | Bank Clock Enable Control See Table 1-883. |
| 5 | DCEN5 | Bank Clock Enable Control See Table 1-883. |
| 4 | DCEN4 | Bank Clock Enable Control See Table 1-883. |
| 3 | DCEN3 | Bank Clock Enable Control See Table 1-883. |
| 2 | DCEN2 | Bank Clock Enable Control See Table 1-883. |
| 1 | DCEN1 | Bank Clock Enable Control See Table 1-883. |
| 0 | DCEN0 | Bank Clock Enable Control See Table 1-883. |

Table 1-883. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | DISABLE | Digital Global clock is disabled. |
| 1'b1 | ENABLE | Digital Global clock is enabled. |

1.3.1273 BCTL[0..3]_BCLK_EN1

BCLK_EN

Reset: Reset Signals Listed Below

Register : Address

BCTL0_BCLK_EN1: 0x4001500B

BCTL1_BCLK_EN1: 0x4001501B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|-------|------------|------------|-------------------|-----------|-----------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | SLEEP_TEST | NC0 | WR_CFG_OPT | GLB_DSI_WR | DISABLE_R OUTE | GCH_WR_HI | GCH_WR_LO | BCEN |

Bus Clock Enable Register

Register Segment: 2

| Bits | Name | Description |
|------|------------|---|
| 7 | SLEEP_TEST | <p>Assertion of this bit drives sleep into the s8udb array for internal s8udb test purposes. Assertion does not affect the power switches. This signal drives pulldowns on the write strobes for all configuration memory, inhibiting writes when set. Sleep or sleep_test does not inhibit writes to this bit, allowing it to be cleared once it has been set. Control is split top and bottom.</p> <p>BCTL0_BCLK_EN0 controls Bank 0 UDB pairs 0-3 and DSI blocks 0-3. BCTL0_BCLK_EN3 controls Bank 0 UDB pairs 4-7 and DSI blocks 4-7. BCTL1_BCLK_EN1 controls Bank 1 UDB pairs 2-3 and DSI blocks 8-9. BCTL1_BCLK_EN2 controls Bank 1 UDB pairs 4-5 and DSI blocks 12-13. The SLEEP_TEST bits in the other BCTLx_BCLK_ENy registers are not used. Sleep assertion drives bus_data to zero so bus read transactions will not return data during assertion of certain sleep_test bits. This is only true for assertion of sleep_test in BCTL0_BCLK_EN0 for Bank 0 and BCTL1_BCLK_EN1 for Bank1.</p> <p>See Table 1-889.</p> |
| 6 | NC0 | Spare register bit |
| 5 | WR_CFG_OPT | <p>Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. BCTL1_BCLK_EN1 controls this bit for Bank 1. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used.</p> <p>See Table 1-890.</p> |
| 4 | GLB_DSI_WR | <p>Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. BCTL1_BCLK_EN1 controls DSI blocks 8-9. BCTL1_BCLK_EN2 controls DSI blocks 12-13. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used.</p> <p>See Table 1-888.</p> |

1.3.1273 BCTL[0..3]_BCLK_EN1 (continued)

| | | |
|---|---------------|---|
| 3 | DISABLE_ROUTE | By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-885. |
| 2 | GCH_WR_HI | Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-886. |
| 1 | GCH_WR_LO | Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-887. |
| 0 | BCEN | Bank Clock Enable Control See Table 1-884. |

Reset Table

| resetsignal | field(s) |
|--|--|
| System reset for retention flops [reset_all_retention] | BCEN, GCH_WR_LO, GCH_WR_HI, DISABLE_ROUTE, GLB_DSI_WR, WR_CFG_OPT, NC0 |
| Domain reset for non-retention flops [reset_all_nonretention] | SLEEP_TEST |

Table 1-884. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | DISABLE | Digital Global clock is disabled. |
| 1'b1 | ENABLE | Digital Global clock is enabled. |

Table 1-885. Bit field encoding: DIS_ROUTE

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | ENABLE | The routing in this quadrant can be enabled with the bank route enable bit. (default) |
| 1'b1 | DISABLE | The routing in this quadrant is disabled and held in a benign state. |

Table 1-886. Bit field encoding: GCH_WR_HI

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | Global UDB channel configuration write for higher order address is disabled. |
| 1'b1 | ENABLE | Global UDB channel configuration write for higher order address is enabled. |

Table 1-887. Bit field encoding: GCH_WR_LO

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Global UDB channel configuration write for lower order address is disabled. |
| 1'b1 | ENABLE | Global UDB channel configuration write for lower order address is enabled. |

Table 1-888. Bit field encoding: GLB_DSI_WR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1273 BCTL[0..3]_BCLK_EN1 (continued)

Table 1-888. Bit field encoding: GLB_DSI_WR

| | | |
|------|---------|---|
| 1'b0 | DISABLE | Global DSI channel configuration write is disabled. |
| 1'b1 | ENABLE | Global DSI channel configuration write is enabled. |

Table 1-889. Bit field encoding: SLEEP_TEST_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------|
| 1'b0 | DISABLE | sleep_test is not asserted. |
| 1'b1 | ENABLE | sleep_test is asserted. |

Table 1-890. Bit field encoding: WR_CFG_OPT_ENUM

| Value | Name | Description |
|-------|----------------|--|
| 1'b0 | FULL_CYCLE_STB | bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. |
| 1'b1 | HALF_CYCLE_STB | bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk. |

1.3.1274 BCTL[0..3]_DCLK_EN2

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN2: 0x4001500C

BCTL1_DCLK_EN2: 0x4001501C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | DCEN7 | DCEN6 | DCEN5 | DCEN4 | DCEN3 | DCEN2 | DCEN1 | DCEN0 |

Digital Global Clock Enable Register

Register Segment: 2

| Bits | Name | Description |
|------|-------|---|
| 7 | DCEN7 | Bank Clock Enable Control See Table 1-891. |
| 6 | DCEN6 | Bank Clock Enable Control See Table 1-891. |
| 5 | DCEN5 | Bank Clock Enable Control See Table 1-891. |
| 4 | DCEN4 | Bank Clock Enable Control See Table 1-891. |
| 3 | DCEN3 | Bank Clock Enable Control See Table 1-891. |
| 2 | DCEN2 | Bank Clock Enable Control See Table 1-891. |
| 1 | DCEN1 | Bank Clock Enable Control See Table 1-891. |
| 0 | DCEN0 | Bank Clock Enable Control See Table 1-891. |

Table 1-891. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | DISABLE | Digital Global clock is disabled. |
| 1'b1 | ENABLE | Digital Global clock is enabled. |

1.3.1275 BCTL[0..3]_BCLK_EN2

BCLK_EN

Reset: Reset Signals Listed Below

Register : Address

BCTL0_BCLK_EN2: 0x4001500D

BCTL1_BCLK_EN2: 0x4001501D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|-------|------------|------------|----------------|-----------|-----------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | SLEEP_TEST | NC0 | WR_CFG_OPT | GLB_DSI_WR | DISABLE_R_OUTE | GCH_WR_HI | GCH_WR_LO | BCEN |

Bus Clock Enable Register

Register Segment: 2

| Bits | Name | Description |
|------|------------|---|
| 7 | SLEEP_TEST | <p>Assertion of this bit drives sleep into the s8udb array for internal s8udb test purposes. Assertion does not affect the power switches. This signal drives pulldowns on the write strobes for all configuration memory, inhibiting writes when set. Sleep or sleep_test does not inhibit writes to this bit, allowing it to be cleared once it has been set. Control is split top and bottom.</p> <p>BCTL0_BCLK_EN0 controls Bank 0 UDB pairs 0-3 and DSI blocks 0-3. BCTL0_BCLK_EN3 controls Bank 0 UDB pairs 4-7 and DSI blocks 4-7. BCTL1_BCLK_EN1 controls Bank 1 UDB pairs 2-3 and DSI blocks 8-9. BCTL1_BCLK_EN2 controls Bank 1 UDB pairs 4-5 and DSI blocks 12-13. The SLEEP_TEST bits in the other BCTLx_BCLK_ENy registers are not used. Sleep assertion drives bus_data to zero so bus read transactions will not return data during assertion of certain sleep_test bits. This is only true for assertion of sleep_test in BCTL0_BCLK_EN0 for Bank 0 and BCTL1_BCLK_EN1 for Bank1.</p> <p>See Table 1-897.</p> |
| 6 | NC0 | Spare register bit |
| 5 | WR_CFG_OPT | <p>Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. BCTL1_BCLK_EN1 controls this bit for Bank 1. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used.</p> <p>See Table 1-898.</p> |
| 4 | GLB_DSI_WR | <p>Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. BCTL1_BCLK_EN1 controls DSI blocks 8-9. BCTL1_BCLK_EN2 controls DSI blocks 12-13. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used.</p> <p>See Table 1-896.</p> |

1.3.1275 BCTL[0..3]_BCLK_EN2 (continued)

| | | |
|---|---------------|---|
| 3 | DISABLE_ROUTE | By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-893. |
| 2 | GCH_WR_HI | Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-894. |
| 1 | GCH_WR_LO | Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-895. |
| 0 | BCEN | Bank Clock Enable Control See Table 1-892. |

Reset Table

| resetsignal | field(s) |
|--|--|
| System reset for retention flops [reset_all_retention] | BCEN, GCH_WR_LO, GCH_WR_HI, DISABLE_ROUTE, GLB_DSI_WR, WR_CFG_OPT, NC0 |
| Domain reset for non-retention flops [reset_all_nonretention] | SLEEP_TEST |

Table 1-892. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | DISABLE | Digital Global clock is disabled. |
| 1'b1 | ENABLE | Digital Global clock is enabled. |

Table 1-893. Bit field encoding: DIS_ROUTE

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | ENABLE | The routing in this quadrant can be enabled with the bank route enable bit. (default) |
| 1'b1 | DISABLE | The routing in this quadrant is disabled and held in a benign state. |

Table 1-894. Bit field encoding: GCH_WR_HI

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | Global UDB channel configuration write for higher order address is disabled. |
| 1'b1 | ENABLE | Global UDB channel configuration write for higher order address is enabled. |

Table 1-895. Bit field encoding: GCH_WR_LO

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Global UDB channel configuration write for lower order address is disabled. |
| 1'b1 | ENABLE | Global UDB channel configuration write for lower order address is enabled. |

Table 1-896. Bit field encoding: GLB_DSI_WR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1275 BCTL[0..3]_BCLK_EN2 (continued)

Table 1-896. Bit field encoding: GLB_DSI_WR

| | | |
|------|---------|---|
| 1'b0 | DISABLE | Global DSI channel configuration write is disabled. |
| 1'b1 | ENABLE | Global DSI channel configuration write is enabled. |

Table 1-897. Bit field encoding: SLEEP_TEST_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------|
| 1'b0 | DISABLE | sleep_test is not asserted. |
| 1'b1 | ENABLE | sleep_test is asserted. |

Table 1-898. Bit field encoding: WR_CFG_OPT_ENUM

| Value | Name | Description |
|-------|----------------|--|
| 1'b0 | FULL_CYCLE_STB | bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. |
| 1'b1 | HALF_CYCLE_STB | bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk. |

1.3.1276 BCTL[0..3]_DCLK_EN3

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN3: 0x4001500E

BCTL1_DCLK_EN3: 0x4001501E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | DCEN7 | DCEN6 | DCEN5 | DCEN4 | DCEN3 | DCEN2 | DCEN1 | DCEN0 |

Digital Global Clock Enable Register

Register Segment: 2

| Bits | Name | Description |
|------|-------|---|
| 7 | DCEN7 | Bank Clock Enable Control See Table 1-899. |
| 6 | DCEN6 | Bank Clock Enable Control See Table 1-899. |
| 5 | DCEN5 | Bank Clock Enable Control See Table 1-899. |
| 4 | DCEN4 | Bank Clock Enable Control See Table 1-899. |
| 3 | DCEN3 | Bank Clock Enable Control See Table 1-899. |
| 2 | DCEN2 | Bank Clock Enable Control See Table 1-899. |
| 1 | DCEN1 | Bank Clock Enable Control See Table 1-899. |
| 0 | DCEN0 | Bank Clock Enable Control See Table 1-899. |

Table 1-899. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | DISABLE | Digital Global clock is disabled. |
| 1'b1 | ENABLE | Digital Global clock is enabled. |

1.3.1277 BCTL[0..3]_BCLK_EN3

BCLK_EN

Reset: Reset Signals Listed Below

Register : Address

BCTL0_BCLK_EN3: 0x4001500F

BCTL1_BCLK_EN3: 0x4001501F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|-------|------------|------------|----------------|-----------|-----------|-------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | R | R | R | R | R | R | R |
| Name | SLEEP_TEST | NC0 | WR_CFG_OPT | GLB_DSI_WR | DISABLE_R_OUTE | GCH_WR_HI | GCH_WR_LO | BCEN |

Bus Clock Enable Register

Register Segment: 2

| Bits | Name | Description |
|------|------------|---|
| 7 | SLEEP_TEST | <p>Assertion of this bit drives sleep into the s8udb array for internal s8udb test purposes. Assertion does not affect the power switches. This signal drives pulldowns on the write strobes for all configuration memory, inhibiting writes when set. Sleep or sleep_test does not inhibit writes to this bit, allowing it to be cleared once it has been set. Control is split top and bottom.</p> <p>BCTL0_BCLK_EN0 controls Bank 0 UDB pairs 0-3 and DSI blocks 0-3. BCTL0_BCLK_EN3 controls Bank 0 UDB pairs 4-7 and DSI blocks 4-7. BCTL1_BCLK_EN1 controls Bank 1 UDB pairs 2-3 and DSI blocks 8-9. BCTL1_BCLK_EN2 controls Bank 1 UDB pairs 4-5 and DSI blocks 12-13. The SLEEP_TEST bits in the other BCTLx_BCLK_ENy registers are not used. Sleep assertion drives bus_data to zero so bus read transactions will not return data during assertion of certain sleep_test bits. This is only true for assertion of sleep_test in BCTL0_BCLK_EN0 for Bank 0 and BCTL1_BCLK_EN1 for Bank1.</p> <p>See Table 1-905.</p> |
| 6 | NC0 | Spare register bit |
| 5 | WR_CFG_OPT | <p>Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. BCTL1_BCLK_EN1 controls this bit for Bank 1. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used.</p> <p>See Table 1-906.</p> |
| 4 | GLB_DSI_WR | <p>Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. BCTL1_BCLK_EN1 controls DSI blocks 8-9. BCTL1_BCLK_EN2 controls DSI blocks 12-13. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used.</p> <p>See Table 1-904.</p> |

1.3.1277 BCTL[0..3]_BCLK_EN3 (continued)

| | | |
|---|---------------|---|
| 3 | DISABLE_ROUTE | By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-901. |
| 2 | GCH_WR_HI | Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-902. |
| 1 | GCH_WR_LO | Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-903. |
| 0 | BCEN | Bank Clock Enable Control See Table 1-900. |

Reset Table

| resetsignal | field(s) |
|--|--|
| System reset for retention flops [reset_all_retention] | BCEN, GCH_WR_LO, GCH_WR_HI, DISABLE_ROUTE, GLB_DSI_WR, WR_CFG_OPT, NC0 |
| Domain reset for non-retention flops [reset_all_nonretention] | SLEEP_TEST |

Table 1-900. Bit field encoding: CLK_EN_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------------|
| 1'b0 | DISABLE | Digital Global clock is disabled. |
| 1'b1 | ENABLE | Digital Global clock is enabled. |

Table 1-901. Bit field encoding: DIS_ROUTE

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | ENABLE | The routing in this quadrant can be enabled with the bank route enable bit. (default) |
| 1'b1 | DISABLE | The routing in this quadrant is disabled and held in a benign state. |

Table 1-902. Bit field encoding: GCH_WR_HI

| Value | Name | Description |
|-------|---------|--|
| 1'b0 | DISABLE | Global UDB channel configuration write for higher order address is disabled. |
| 1'b1 | ENABLE | Global UDB channel configuration write for higher order address is enabled. |

Table 1-903. Bit field encoding: GCH_WR_LO

| Value | Name | Description |
|-------|---------|---|
| 1'b0 | DISABLE | Global UDB channel configuration write for lower order address is disabled. |
| 1'b1 | ENABLE | Global UDB channel configuration write for lower order address is enabled. |

Table 1-904. Bit field encoding: GLB_DSI_WR

| Value | Name | Description |
|-------|------|-------------|
|-------|------|-------------|

1.3.1277 BCTL[0..3]_BCLK_EN3 (continued)

Table 1-904. Bit field encoding: GLB_DSI_WR

| | | |
|------|---------|---|
| 1'b0 | DISABLE | Global DSI channel configuration write is disabled. |
| 1'b1 | ENABLE | Global DSI channel configuration write is enabled. |

Table 1-905. Bit field encoding: SLEEP_TEST_ENUM

| Value | Name | Description |
|-------|---------|-----------------------------|
| 1'b0 | DISABLE | sleep_test is not asserted. |
| 1'b1 | ENABLE | sleep_test is asserted. |

Table 1-906. Bit field encoding: WR_CFG_OPT_ENUM

| Value | Name | Description |
|-------|----------------|--|
| 1'b0 | FULL_CYCLE_STB | bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. |
| 1'b1 | HALF_CYCLE_STB | bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk. |

1.3.1278 IDMUX_IRQ_CTL[0..7]

Control Register IRQ_CTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IDMUX_IRQ_CTL0: 0x40015100

IDMUX_IRQ_CTL1: 0x40015101

IDMUX_IRQ_CTL2: 0x40015102

IDMUX_IRQ_CTL3: 0x40015103

IDMUX_IRQ_CTL4: 0x40015104

IDMUX_IRQ_CTL5: 0x40015105

IDMUX_IRQ_CTL6: 0x40015106

IDMUX_IRQ_CTL7: 0x40015107

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|--------|---|--------|---|--------|---|
| SW Access:Reset | R/W:00 | | R/W:00 | | R/W:00 | | R/W:00 | |
| HW Access | R | | R | | R | | R | |
| Name | ICTRL3 | | ICTRL2 | | ICTRL1 | | ICTRL0 | |

This register is used to configure the routing and processing of interrupts.

| Bits | Name | Description |
|------|-------------|---|
| 7:6 | ICTRL3[1:0] | IRQ Control See Table 1-907. |
| 5:4 | ICTRL2[1:0] | IRQ Control See Table 1-907. |
| 3:2 | ICTRL1[1:0] | IRQ Control See Table 1-907. |
| 1:0 | ICTRL0[1:0] | IRQ Control See Table 1-907. |

Table 1-907. Bit field encoding: irq_enum

| Value | Name | Description |
|-------|----------------|---------------------------|
| 2'b00 | Fixed Function | Fixed Function Interrupt. |
| 2'b01 | DMA | DMA Interrupt |
| 2'b10 | UDB | UDB Level Interrupt |
| 2'b11 | UDB EDGE | UDB Edge Detect Interrupt |

1.3.1279 IDMUX_DRQ_CTL[0..5]

Configuration Register DRQ_CTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IDMUX_DRQ_CTL0: 0x40015110

IDMUX_DRQ_CTL1: 0x40015111

IDMUX_DRQ_CTL2: 0x40015112

IDMUX_DRQ_CTL3: 0x40015113

IDMUX_DRQ_CTL4: 0x40015114

IDMUX_DRQ_CTL5: 0x40015115

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|--------|---|--------|---|--------|---|
| SW Access:Reset | R/W:00 | | R/W:00 | | R/W:00 | | R/W:00 | |
| HW Access | R | | R | | R | | R | |
| Name | DCTRL3 | | DCTRL2 | | DCTRL1 | | DCTRL0 | |

This register is used to select between DMA requests (fixed function or udb).

| Bits | Name | Description |
|------|-------------|---|
| 7:6 | DCTRL3[1:0] | DMA input type. See Table 1-908. |
| 5:4 | DCTRL2[1:0] | DMA input type. See Table 1-908. |
| 3:2 | DCTRL1[1:0] | DMA input type. See Table 1-908. |
| 1:0 | DCTRL0[1:0] | DMA input type. See Table 1-908. |

Table 1-908. Bit field encoding: drq_enum

| Value | Name | Description |
|-------|----------------|-----------------------------|
| 2'b00 | Fixed Function | Fixed Function DMA request. |
| 2'b01 | UDB | UDB Level DMA request |
| 2'b10 | UDB EDGE | UDB Edge Detect DMA request |
| 2'b11 | RESERVED | RESERVED |

1.3.1280 CACHERAM_DATA[0..255]

Cache SRAM

Reset: N/A

Register : Address

CACHERAM_DATA: 0x40030000-0x400303FF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cache_sram | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cache_sram | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cache_sram | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cache_sram | | | | | | | |

This is actually two interleaved instances of s8tssc_128x32. Address bit 2 selects which of the two memories is selected.

| Bits | Name | Description |
|------|------------------|------------------|
| 31:0 | cache_sram[31:0] | (no description) |

1.3.1281 SFR_GPIO0

GPIO0 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO0: 0x40050180

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO0 | | | | | | | |

This register is used to set the output data state for Port0

| Bits | Name | Description |
|------|------------|--|
| 7:0 | GPIO0[7:0] | The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO0_SEL register is set to high |

1.3.1282 SFR_GPIRD0

GPIRD0 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIRD0: 0x40050189

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | GPIRD0 | | | | | | | |

This read only register contains pin state value of Port0

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | GPIRD0[7:0] | This register contains the pin state values of Port0 pins |

1.3.1283 SFR_GPIO0_SEL

GPIO0_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO0_SEL: 0x4005018A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO0_SEL | | | | | | | |

This register is used to select the GPIO0 register to set the output data state for Port0

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | GPIO0_SEL[7:0] | This register is used to select each bit of the GPIO0 register to set the output data state for the corresponding pin of Port0. |

1.3.1284 SFR_GPIO1

GPIO1 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO1: 0x40050190

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO1 | | | | | | | |

This register is used to set the output data state for Port1

| Bits | Name | Description |
|------|------------|--|
| 7:0 | GPIO1[7:0] | The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO1_SEL register is set to high |

1.3.1285 SFR_GPIRD1

GPIRD1 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIRD1: 0x40050191

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | GPIRD1 | | | | | | | |

This read only register contains pin state value of Port1

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | GPIRD1[7:0] | This register contains the pin state values of Port1 pins |

1.3.1286 SFR_GPIO2

GPIO2 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO2: 0x40050198

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO2 | | | | | | | |

This register is used to set the output data state for Port2

| Bits | Name | Description |
|------|------------|--|
| 7:0 | GPIO2[7:0] | The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO2_SEL register is set to high |

1.3.1287 SFR_GPIRD2

GPIRD2 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIRD2: 0x40050199

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | GPIRD2 | | | | | | | |

This read only register contains pin state value of Port2

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | GPIRD2[7:0] | This register contains the pin state values of Port2 pins |

1.3.1288 SFR_GPIO2_SEL

GPIO2_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO2_SEL: 0x4005019A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO2_SEL | | | | | | | |

This register is used to select the GPIO2 register to set the output data state for Port2

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | GPIO2_SEL[7:0] | This register is used to select each bit of the GPIO2 register to set the output data state for the corresponding pin of Port2. |

1.3.1289 SFR_GPIO1_SEL

GPIO1_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO1_SEL: 0x400501A2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO1_SEL | | | | | | | |

This register is used to select the GPIO1 register to set the output data state for Port1

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | GPIO1_SEL[7:0] | This register is used to select each bit of the GPIO1 register to set the output data state for the corresponding pin of Port1. |

1.3.1290 SFR_GPIO3

GPIO3 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO3: 0x400501B0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO3 | | | | | | | |

This register is used to set the output data state for Port3

| Bits | Name | Description |
|------|------------|--|
| 7:0 | GPIO3[7:0] | The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO3_SEL register is set to high |

1.3.1291 SFR_GPIRD3

GPIRD3 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIRD3: 0x400501B1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | GPIRD3 | | | | | | | |

This read only register contains pin state value of Port3

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | GPIRD3[7:0] | This register contains the pin state values of Port3 pins |

1.3.1292 SFR_GPIO3_SEL

GPIO3_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO3_SEL: 0x400501B2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO3_SEL | | | | | | | |

This register is used to select the GPIO3 register to set the output data state for Port3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | GPIO3_SEL[7:0] | This register is used to select each bit of the GPIO3 register to set the output data state for the corresponding pin of Port3. |

1.3.1293 SFR_GPIO4

GPIO4 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO4: 0x400501C0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO4 | | | | | | | |

This register is used to set the output data state for Port4

| Bits | Name | Description |
|------|------------|--|
| 7:0 | GPIO4[7:0] | The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO4_SEL register is set to high |

1.3.1294 SFR_GPIRD4

GPIRD4 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIRD4: 0x400501C1

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | GPIRD4 | | | | | | | |

This read only register contains pin state value of Port4

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | GPIRD4[7:0] | This register contains the pin state values of Port4 pins |

1.3.1295 SFR_GPIO4_SEL

GPIO4_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO4_SEL: 0x400501C2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO4_SEL | | | | | | | |

This register is used to select the GPIO4 register to set the output data state for Port4

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | GPIO4_SEL[7:0] | This register is used to select each bit of the GPIO4 register to set the output data state for the corresponding pin of Port4. |

1.3.1296 SFR_GPIO5

GPIO5 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO5: 0x400501C8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO5 | | | | | | | |

This register is used to set the output data state for Port5

| Bits | Name | Description |
|------|------------|--|
| 7:0 | GPIO5[7:0] | The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO5_SEL register is set to high |

1.3.1297 SFR_GPIRD5

GPIRD5 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIRD5: 0x400501C9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | GPIRD5 | | | | | | | |

This read only register contains pin state value of Port5

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | GPIRD5[7:0] | This register contains the pin state values of Port5 pins |

1.3.1298 SFR_GPIO5_SEL

GPIO5_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO5_SEL: 0x400501CA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO5_SEL | | | | | | | |

This register is used to select the GPIO5 register to set the output data state for Port5

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | GPIO5_SEL[7:0] | This register is used to select each bit of the GPIO5 register to set the output data state for the corresponding pin of Port5. |

1.3.1299 SFR_GPIO6

GPIO6 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO6: 0x400501D8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO6 | | | | | | | |

This register is used to set the output data state for Port6

| Bits | Name | Description |
|------|------------|--|
| 7:0 | GPIO6[7:0] | The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO6_SEL register is set to high |

1.3.1300 SFR_GPIRD6

GPIRD6 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIRD6: 0x400501D9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | GPIRD6 | | | | | | | |

This read only register contains pin state value of Port6

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | GPIRD6[7:0] | This register contains the pin state values of Port6 pins |

1.3.1301 SFR_GPIO6_SEL

GPIO6_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO6_SEL: 0x400501DA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO6_SEL | | | | | | | |

This register is used to select the GPIO6 register to set the output data state for Port6

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | GPIO6_SEL[7:0] | This register is used to select each bit of the GPIO6 register to set the output data state for the corresponding pin of Port6. |

1.3.1302 SFR_GPIO12

GPIO12 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO12: 0x400501E8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO12 | | | | | | | |

This register is used to set the output data state for Port12

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | GPIO12[7:0] | The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO12_SEL register is set to high |

1.3.1303 SFR_GPIRD12

GPIRD12 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIRD12: 0x400501E9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | GPIRD12 | | | | | | | |

This read only register contains pin state value of Port12

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | GPIRD12[7:0] | This register contains the pin state values of Port12 pins |

1.3.1304 SFR_GPIO12_SEL

GPIO12_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO12_SEL: 0x400501F2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO12_SEL | | | | | | | |

This register is used to select the GPIO12 register to set the output data state for Port12

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | GPIO12_SEL[7:0] | This register is used to select each bit of the GPIO12 register to set the output data state for the corresponding pin of Port12. |

1.3.1305 SFR_GPIO15

GPIO15 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO15: 0x400501F8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO15 | | | | | | | |

This register is used to set the output data state for Port15

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | GPIO15[7:0] | The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO15_SEL register is set to high |

1.3.1306 SFR_GPIRD15

GPIRD15 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIRD15: 0x400501F9

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | W | | | | | | | |
| Name | GPIRD15 | | | | | | | |

This read only register contains pin state value of Port15

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | GPIRD15[7:0] | This register contains the pin state values of Port15 pins |

1.3.1307 SFR_GPIO15_SEL

GPIO15_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_GPIO15_SEL: 0x400501FA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | GPIO15_SEL | | | | | | | |

This register is used to select the GPIO15 register to set the output data state for Port15

| Bits | Name | Description |
|------|-----------------|---|
| 7:0 | GPIO15_SEL[7:0] | This register is used to select each bit of the GPIO15 register to set the output data state for the corresponding pin of Port15. |

1.3.1308 TC_TST_CR1

Test Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TC_TST_CR1: 0x40050200

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------|------------|------------|------------|-----------|-------|---|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:00 | |
| HW Access | NA | R/W | R/W | R/W | R/W | R/W | NA | |
| Name | | | frcret_slp | frcpwr_off | iddq_synth | iddq_misc | | |

This register activates various production test modes and is written in test mode only. This register is an INTERNAL register.

| Bits | Name | Description |
|------|------------|--|
| 6 | RSVD | This r/w bit has no functional use |
| 5 | frcret_slp | Force retention cells to sleep, when FRCRET_SLP is set to 1 the power controller forces all retention cells to sleep. This does not actually turn off power to retention cells. It's only used for activating nondisturb logic on all retention cells. This bit must be set before 'FRCPWR_OFF' is set. 0 frcret_slp disabled 1 frcret_slp enabled |
| 4 | frcpwr_off | Force Power Off, when FRCPWR_OFF is set to 1 all switched power domains all forced off. This does not include the Vka domain which powers the auxiliary power for retention cells. Also, all voltage-observe paths for each switched off domain are turned on. See power modes and timers for more details. 0 frcpwr_off disabled 1 frcpwr_off enabled |
| 3 | iddq_synth | IDDQ Clock Synthesizer Test Mode, When this bit is set to '1'IDDQ Clock Synthesizer Test Mode is enabled. when set to '0' IDDQ Clock Synthesizer Test Mode is disabled. IDDQ_SYNTH forces all clock synthesizers into a low power state. 0 iddq_synth disabled 1 iddq_synth enabled |
| 2 | iddq_misc | IDDQ Miscellaneous Test Mode, When this bit is set to '1'IDDQ Test Modes for all other blocks are enabled. when set to '0' IDDQ Misc Test Mode is disabled. IDDQ_MISC forces all blocks (except those blocks needed by at-speed scan -PLL) into a low power state. 0 iddq_misc disabled 1 iddq_misc enabled |

1.3.1309 TC_TST_CR2

Test Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TC_TST_CR2: 0x40050201

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|-------|------|-----------|----------|-----------|-------|-----------|
| SW Access:Reset | R/W:0 | R/W:0 | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R/W | R/W | NA | R/W | R/W | R/W | R/W | R/W |
| Name | tstclk_en | entr | | tstrst_en | d_scan_c | scan_mode | ptm | d_scan_as |

This register activates various production test modes and is written in test mode only. This register is an INTERNAL register.

| Bits | Name | Description |
|------|------------------------------|--|
| 7 | tstclk_en | The test clock enable but activates the test clock. |
| 6 | Enable Test Mode Read {entr} | This bit enables test mode reads of the RO port using the RW port using Tri_buf in all instances of s8dparam instances. This is designed to provide Soft-BIST testing support for RO ports. 0 entr disabled 1 entr enabled |
| 4 | tstrst_en | This bit enables test reset. If TSTRST_EN is set to 1 the dedicated XRES pin turns into TSTRST. This means that the JTAG state machine and a select few registers are not reset when the pin is asserted. tstrst_en takes priority over the XRES SONOS bit to enable TSTRST from the dedicated XRES pin. So before this bit is set, you must ensure that P1_2 has its input buffer enabled and that you are drive logic 1 on the pad if you do not wish to reset the part. Also, all other reset sources such as WDR, IRES are automatically disabled. This register must always be connected in some way to PORs to guarantee it is cleared at power on. This bit also reads 1'b0 if JTAG is enabled and the current JTAG state is Test Logic Reset. 0 tstrst_en disabled 1 tstrst_en enabled |
| 3 | d_scan_c | Disable Scan Compression. This bit will disable adaptive scan logic which implements on-chip scan patter decompression and compression. This bit is used for diagnostic purposes. Scan Compression Disable when set to '1', scan compression enabled when set to '0'. The output scan_cmp_en = !(d_scan_c). 0 scan compression is enabled 1 scan compression is disabled (for debug) |
| 2 | scan_mode | Scan Test Mode, When this bit is set to '1' SCAN is enabled. When set to '0' SCAN is disabled. Forces all retention cells on (by default) Forces all power domains on (by default) Forces reset domains off on all non-scanned flops used for scan configuration. Forces the same behavior as when TSTRST_EN =1. The I/PPOR must always be somehow connected to reset this SCAN register bit to avoid powering on into SCAN mode. Forces all scanout los outward. Forces all other IOS inward. So once this bit is set, you can not use JTAG/SWD to read and write registers Before scan test mode will be fully allowed, the Cache Controller mus have completed execution of a Cache memory BIST sequence. 0 scan test mode disabled 1 scan test mode is allowed while JTAG is idle |
| 1 | ptm | Parallel Test Mode, When this bit set to '1' PTM is enabled. When set to '0' PTM is disabled. Once this bit is set only PTM can be used to read or re-write this bit |

[See Table 1-910.](#)

1.3.1309 TC_TST_CR2 (continued)

| | | |
|---|-----------|--|
| 0 | d_scan_as | Disable At-Speed Scan Test Mode, When set to 1 allow all at-speed scan clock support logic to be unconstrained to be disturbed and tested. This register controls the output signal 'dis_scan_as' that goes to clock distribution logic which is required to be constrained while using internally generated at-speed clocks for at-speed scan testing. This signal is always ignored unless scan_test_mode is also set. |
|---|-----------|--|

[See Table 1-909.](#)

Table 1-909. Bit field encoding: D_SCAN_AS_ENUM

| Value | Name | Description |
|-------|-------------|---|
| 1'b1 | SAF_TESTING | Don't constrain at-speed internal clock support logic |
| 1'b0 | TRF_TESTING | Constrain at-speed internal clock support logic to maintain free-running internal clock sources for OCCs. |

Table 1-910. Bit field encoding: PTM_ENUM

| Value | Name | Description |
|-------|-------------|------------------|
| 1'b1 | PTM_ENABLE | PTM is enabled. |
| 1'b0 | PTM_DISABLE | PTM is disabled. |

1.3.1310 TC_TST_CR3

Test Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TC_TST_CR3: 0x40050202

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|----------|----------|------------|----------|------------|----------|----------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | ba_en | wco_tclk | eco_tclk | imo36_tclk | ilo_tclk | imox2_tclk | imo_tclk | pll_tclk |

This register activates various production test modes and is written in test mode only. This register is an INTERNAL register.

| Bits | Name | Description |
|------|------------|--|
| 7 | ba_en | BIST Assit Enable, When set to logic '1' the BIST Assit block becomes an active slave on the PHUB. This bit field is attached to the TC output ba_en |
| 6 | wco_tclk | Test Clock select for Watch Crystal Oscillator (WCO) ouput, when set to 1, Test Clock replaces WCO output |
| 5 | eco_tclk | Test Clock select for External Crystal Oscillator (ECO) output, when set to 1, Test Clock replaces ECO output |
| 4 | imo36_tclk | Test Clock select for 36 MHz IMO output, when set to 1, Test Clock replaces the 36 MHz IMO output |
| 3 | ilo_tclk | Test Clock select for ILO output, when set to 1, Test Clock replaces ILO output |
| 2 | imox2_tclk | Test Clock select for IMO doubler output, when set to 1, Test Clock replaces IMO doubler output |
| 1 | imo_tclk | Test Clock select for IMO output, when set to 1, Test Clock replaces the IMO output |
| 0 | pll_tclk | Test Clock select for PLL output, when set to 1, Test Clock replaces the PLL output. |

1.3.1311 TC_TST_CR4

Test Control Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TC_TST_CR4: 0x40050203

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|------------|------|----------|------|--------------|----------|-----------|
| SW Access:Reset | R/W:0 | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R/W | R/W | NA | R/W | NA | R/W | R/W | R/W |
| Name | occ_bypass | sar_bypass | | ret_scan | | slpbymx_ctrl | frc_isol | frc_bleed |

This register activates various production test modes and is written in test mode only. This register is an INTERNAL register.

| Bits | Name | Description |
|------|--------------|--|
| 7 | occ_bypass | Bypass On Chip Clock (OCC) controllers. When set to 1, disables all at-speed scan controllers so that the test clock is always used. This signal is always ignored unless scan test mode is also set. The at-speed functional clock will always be selected when scan_test_mode is clear. This register controls the output signal 'occ_bypass' that is hooked to OCC controllers. See Table 1-911. |
| 6 | sar_bypass | (RMP) SAR scan chain bypass configuration. |
| 4 | ret_scan | (RMP) Retention cell-only scan mode, enabled when this bit is set to '1'. Once this bit is set you can not use JTAG/SWD to read or write to registers |
| 2 | slpbymx_ctrl | Sleep Regulator Bypass Control, when set to logic '1' the regulator is only bypassed during scan shift operations. When cleared the sleep regulator is always bypassed in scan test mode. |
| 1 | frc_isol | Force Isolation, puts all retention flops in retention mode, except for outputs coming from the test/debug power domain. The output 'force_isolation' is attached to this register bit. |
| 0 | frc_bleed | Force Bleed, Enables domain virtual supply bleeder. When set the virtual supplies of the connected domains are resistively connected to ground, which speeds the discharge process. The output 'force_bleed' is attached to this register bit. |

Table 1-911. Bit field encoding: OCC_BYPASS_ENUM

| Value | Name | Description |
|-------|-------------|--|
| 1'b1 | DISABLE_OCC | Force clock controllers to use test clock. |
| 1'b0 | ENABLE_OCC | Allow OCC controllers to operate. |

1.3.1312 TC_TST_CR5

Test Control Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TC_TST_CR5: 0x40050204

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------------|----------------------|----------------------|---------|---|---|-------------|---|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:000 | | | R/W:00 | |
| HW Access | R | R | R | R | | | R | |
| Name | allow_inp_dis_pkg68 | allow_inp_dis_pkg100 | allow_inp_dis_nontst | sopt_en | | | icg_ctrl_en | |

This register enables scanned option (SOPT) registers and is written in test mode only. When scan_test_mode=0, the controls from these registers are all forced low. When scan_test_mode=1, the controls from these registers are all forced high in when scan_shift_en=1. When scan_test_mode=1 and scan_shift_en=0, the controls from these registers are set high if the associated enable bit in this register as well as the scanned-option bit are set. This register is an INTERNAL register.

| Bits | Name | Description |
|------|----------------------|--|
| 7 | allow_inp_dis_pkg68 | Setting this bit will allow scan to disable IOs not on 68-pin package but on 48-pin package during capture. RTL calls the control signal 'tst_inp_dis_pkg68' |
| 6 | allow_inp_dis_pkg100 | Setting this bit will allow scan to disable IOs not on 100-pin package but on 68-pin package during capture. RTL calls the control signal 'tst_inp_dis_pkg100' |
| 5 | allow_inp_dis_nontst | Setting this bit will allow scan to disable non-scan related IOs not on 68-pin package but on 48-pin package during capture. RTL calls the control 'test_inp_dis_pkg48' which may be a bit of a mis-nomer. |
| 4:2 | sopt_en[2:0] | These SOPT enable bits are reserved for future purposes. |
| 1:0 | icg_ctrl_en[1:0] | These bits enable forcing clock gates into bypass during scan capture. bit-0 is connected to all inferred clock gates and is connected automatically during synthesis. bit-1 is connected to all hierarchical clock gates and is associated with 'test_icg_ctrl' in RTL. |

1.3.1313 TC_TST_CR6

Test Control Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TC_TST_CR6: 0x40050205

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | RESERVED | | | | | | | |

Reserved INTERNAL register

| Bits | Name | Description |
|------|---------------|-------------|
| 7:0 | RESERVED[7:0] | Reserved |

1.3.1314 TC_TST_KEY

Test Key Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TC_TST_KEY: 0x40050210

| | | | | | | | | |
|-----------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | KEY | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | KEY | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | KEY | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | KEY | | | | | | | |

Address place holder for test mode entry

| Bits | Name | Description |
|------|-----------|--|
| 31:0 | KEY[31:0] | Writing the correct key value (0xEA7E30A9) enters the part into test mode. The only way to clear this value is via a chip reset. A read of this register returns zeros |

1.3.1315 TC_PM_CTRL

Power Mode Control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TC_PM_CTRL: 0x40050214

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|-------|---|-----------|-------------|-----------|---|---|
| SW Access:Reset | R/W:0 | NA:00 | | R:0 | R:0 | R:000 | | |
| HW Access | R/W | NA | | R/W | R/W | R/W | | |
| Name | tc_hlt_prt | | | mode_trns | cpu_clk_ind | pm_status | | |

Used to read sleep mode status, and wake up the part from sleep

| Bits | Name | Description |
|------|----------------|---|
| 7 | tc_hlt_prt | Test Controller Halt & Port. Two uses: this can be used to force the CPU to halt when C_DEBUGEN is set. Preferred application is when the CPU is in a low power state, so the device can wake-up with the CPU halted. This bit can also be set during a soft reset assertion to reclaim the Debug port if disabled via MLOGIC_DEBUG.dis_dbg_prt |
| 4 | mode_trns | Power Mode Transitioning, if the power mode is in the process of transitioning from one mode to another this bit is read as a logic '1' otherwise it reads as '0' |
| 3 | cpu_clk_ind | Processor clock indicator, read returns 1 when CPU clock is running. |
| 2:0 | pm_status[2:0] | Power Mode Status, is used to determine the current sleep mode of the part. Refer to the Power Modes and Timers chapter of the PSoC3 IROS for more information. |

1.3.1316 P3BA_Y_START

Y_START

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_Y_START: 0x40050300

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R | | | | | | |
| Name | | y_start | | | | | | |

This register is used to store the Y address value of the target memory. It corresponds to the column address of the target memory on which the memory test begins. In case there is only one column in the memory, both y_start and the y_roll values have to be zero.

| Bits | Name | Description |
|------|--------------|--|
| 6:0 | y_start[6:0] | This is the starting value of Y address. |

1.3.1317 P3BA_YROLL

YROLL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_YROLL: 0x40050301

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R | | | | | | |
| Name | | y_roll | | | | | | |

This register is used to store the roll-over value of the Y address range for the target memory. It corresponds to the column address of the target memory, which value when reached by y_curr results in y_curr value rolling over to y_start or memory test being ended (refer to fast_x). The value depends on the physical map of the memory. In case there is only one column in the memory, both y_start and the y_roll values have to be zero.

| Bits | Name | Description |
|------|-------------|--|
| 6:0 | y_roll[6:0] | This is the roll-over value for Y address. |

1.3.1318 P3BA_YCFG

YCFG

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_YCFG: 0x40050302

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------------|---|---|---|---|---|---|
| SW Access:Reset | R/W:0 | R/W:0000000 | | | | | | |
| HW Access | R | R | | | | | | |
| Name | y_sub | y_inc | | | | | | |

This register is used to store the increment/decrement step value for Y address and the direction of the increment. The y_inc corresponds to the data width of the memory (in bytes). In case there is only one column in the memory, the y_inc value has to be zero. The y_sub specifies if the y_curr has to be incremented by y_inc or decremented by y_inc. Care should be taken while setting this bit, so that the calculates y_curr always lies between y_start and y_roll.

| Bits | Name | Description |
|------|------------|--|
| 7 | y_sub | 1'b0: y_curr is incremented by a value of y_inc. (y_sub can be 1'b0 only when y_roll >= y_start) 1'b1: y_curr is decremented by a value of y_inc. (y_sub can be 1'b0 only when y_roll <= y_start) |
| 6:0 | y_inc[6:0] | This is the increment/decrement step value for Y address. |

1.3.1319 P3BA_X_START1

X_START1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_X_START1: 0x40050303

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | x_start1 | | | | | | | |

x_start is the starting value of X address and corresponds to the row address of the target memory on which the test begins. This register is used to store bits [7:0] of the x_start address of the target memory.

| Bits | Name | Description |
|------|---------------|------------------------|
| 7:0 | x_start1[7:0] | Bits (7:0) of x_start. |

1.3.1320 P3BA_X_START2

X_START2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_X_START2: 0x40050304

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | x_start2 | | | | | | | |

This register is used to store bits [15:8] of the x_start address of the target memory.

| Bits | Name | Description |
|------|---------------|-------------------------|
| 7:0 | x_start2[7:0] | Bits (15:8) of x_start. |

1.3.1321 P3BA_XROLL1

XROLL1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_XROLL1: 0x40050305

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | x_roll1 | | | | | | | |

x_roll is the roll-over value of X address range for the target memory. It corresponds to the row address of the target memory, which value when reached by x_curr results in x_curr value rolling over to x_start or memory test being ended (refer to fast_x). The value depends on the physical map of the memory. This register is used to store bits [7:0] of the x_roll address of the target memory.

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | x_roll1[7:0] | Bits (7:0) of x_roll. |

1.3.1322 P3BA_XROLL2

XROLL2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_XROLL2: 0x40050306

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | x_roll2 | | | | | | | |

This register is used to store bits [15:8] of the x_roll address of the target memory.

| Bits | Name | Description |
|------|--------------|------------------------|
| 7:0 | x_roll2[7:0] | Bits (15:8) of x_roll. |

1.3.1323 P3BA_XINC

XINC

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_XINC: 0x40050307

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | x_inc | | | | | | | |

This register is used to store the increment/decrement step value for Y address. The x_inc corresponds to the row address increment value of the target memory (in bytes).

| Bits | Name | Description |
|------|------------|--|
| 7:0 | x_inc[7:0] | This is the increment/decrement step value for X address. This depends on y_start and y_roll |

1.3.1324 P3BA_XCFG

XCFG

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_XCFG: 0x40050308

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|--------|-------|
| SW Access:Reset | NA:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | NA | | | | | | R | R |
| Name | | | | | | | fast_x | x_sub |

This register is used to store the direction of the increment and the priority of increment. The x_sub specifies if the x_curr has to be incremented by y_inc or decremented by y_inc. Care should be taken while setting this bit, so that the calculated x_curr always lies between x_start and x_roll.

| Bits | Name | Description |
|------|--------|--|
| 1 | fast_x | This bit when set causes incrementing to occur primarily on x_curr (fast-x) instead of on y_curr (fast-y). See Table 1-912. |
| 0 | x_sub | 1'b0: x_curr is incremented by a value of x_inc. (x_sub can be 1'b0 only when x_roll >= x_start) 1'b1: x_curr is decremented by a value of x_inc. (x_sub can be 1'b0 only when x_roll <= x_start) |

Table 1-912. Bit field encoding: fast_x_enum

| Value | Name | Description |
|-------|--------|--|
| 1'b1 | FAST_X | Fast X incrementing: x_curr increments/decrements for each sequence. y_curr increments/decrements when x_curr reaches x_roll. The memory test is terminated when both x_curr and y_curr reach the roll-over values. |
| 1'b0 | FAST_Y | Fast Y incrementing: y_curr increments/decrements for each sequence. x_curr increments/decrements when y_curr reaches y_roll. The memory test is terminated when both x_curr and y_curr reach the roll-over values. |

1.3.1325 P3BA_OFFSETADDR1

OFFSETADDR1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_OFFSETADDR1: 0x40050309

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | offset_addr1 | | | | | | | |

The offset address (offset_addr) corresponds to the peripheral address of the target memory. This register is used to store bits (7:0) of the offset address.

| Bits | Name | Description |
|------|-------------------|-------------------------------|
| 7:0 | offset_addr1[7:0] | Bits (7:0) of offset address. |

1.3.1326 P3BA_OFFSETADDR2

OFFSETADDR2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_OFFSETADDR2: 0x4005030A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | offset_addr2 | | | | | | | |

This register is used to store bits (15:8) of the offset address.

| Bits | Name | Description |
|------|-------------------|--------------------------------|
| 7:0 | offset_addr2[7:0] | Bits (15:8) of offset address. |

1.3.1327 P3BA_OFFSETADDR3

OFFSETADDR3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_OFFSETADDR3: 0x4005030B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | offset_addr3 | | | | | | | |

This register is used to store bits (23:16) of the offset address.

| Bits | Name | Description |
|------|-------------------|---------------------------------|
| 7:0 | offset_addr3[7:0] | Bits (23:16) of offset address. |

1.3.1328 P3BA_ABSADDR1

ABSADDR1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_ABSADDR1: 0x4005030C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | abs_addr1 | | | | | | | |

The absolute address (abs_addr) corresponds to the complete address of a memory location in the target memory. Absolute address is generated by OR ing offset address (h), current X address (x) and current Y address (y) in the following manner hhhh_hhhh_hhhh_hhhh_0000_0000 0000_0000_xxxx_xxxx_xxxx_xxxx 0000_0000_0000_0000_0yyy_yyyy It can be seen that some of the bits overlap. In the overlapping bits, there should be no conflicting bits; only one of the address fields can have valid value and the other fields should have zero. For instance, in Leopard, while testing CAN memory the OR function would look like 0000_0000_1010_0000_0000_0000 0000_0000_0000_00xx_xxx0_0000_0000_0000_0000_000y_yyyy In the above function, bits [23:12] corresponds to peripheral addressing, bits [9:2] corresponds to X address and bits [1:0] corresponds to Y address. There is no conflicting overlap. Similarly, for other memories there should be no conflicting overlaps. When read in debug mode this value corresponds to the address of the memory location on which the memory test was last done. This register is used to store bits (7:0) of the absolute address.

| Bits | Name | Description |
|------|----------------|-------------------------------------|
| 7:0 | abs_addr1[7:0] | Bits (7:0) of the absolute address. |

1.3.1329 P3BA_ABSADDR2

ABSADDR2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_ABSADDR2: 0x4005030D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | abs_addr2 | | | | | | | |

Register used to store bits (15:8) of the absolute address.

| Bits | Name | Description |
|------|----------------|--------------------------------------|
| 7:0 | abs_addr2[7:0] | Bits (15:8) of the absolute address. |

1.3.1330 P3BA_ABSADDR3

ABSADDR3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_ABSADDR3: 0x4005030E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | abs_addr3 | | | | | | | |

Register used to store bits (23:16) of the absolute address.

| Bits | Name | Description |
|------|----------------|---------------------------------------|
| 7:0 | abs_addr3[7:0] | Bits (23:16) of the absolute address. |

1.3.1331 P3BA_ABSADDR4

ABSADDR4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_ABSADDR4: 0x4005030F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | abs_addr4 | | | | | | | |

Register used to store bits (31:24) of the absolute address.

| Bits | Name | Description |
|------|----------------|---------------------------------------|
| 7:0 | abs_addr4[7:0] | Bits (31:24) of the absolute address. |

1.3.1332 P3BA_DATCFG1

DATCFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATCFG1: 0x40050310

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | data_invert_mask | | | | | | | |

This register is used to store data inversion address mask. The data invert mask is an address pattern used to invert the data. The logic used to generate data invert signal is $\text{masked_addr} = \text{data_invert_mask}[7:0] \& \text{mstr_haddr}[7:0]$; $\text{data_invert} = \text{^(masked_addr)}$; -- reduction XOR of masked_addr. Based on this data invert signal and the current opcode (regular or inverted), the data is either inverted or is used uninverted.

| Bits | Name | Description |
|------|-----------------------|----------------------------|
| 7:0 | data_invert_mask[7:0] | The 8 bit data invert mask |

1.3.1333 P3BA_DATCFG2

DATCFG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATCFG2: 0x40050311

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|--------------|---|----------|
| SW Access:Reset | NA:00000 | | | | | R/W:00 | | R/W:0 |
| HW Access | NA | | | | | R | | R |
| Name | | | | | | data_pattern | | data_ovr |

This register contains the data override bit and data pattern. When a memory test is initiated, this bit is used either to replicate the data pattern into the data register or to override the data pattern and preserve the explicitly written contents of the data register. The data pattern is the basic 2-bit pattern which, if data_ovr is not set, is replicated to generate data.

| Bits | Name | Description |
|------|-------------------|---|
| 2:1 | data_pattern[1:0] | Basic 2-bit data pattern. |
| 0 | data_ovr | 1'b0: State machine enters INIT state and data pattern bits are replicated in the data_reg. 1'b1: State machine skips INIT state and the contents of the data_reg are preserved. |

1.3.1334 P3BA_CMP_RSLT1

CMP_RSLT1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_CMP_RSLT1: 0x40050314

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | comp_rslt1 | | | | | | | |

The compare result (cmp_rslt) is the XOR'd result of registered hrdata and the expected data during master mode. The comparison is done only when a read operation is performed. This register contains bits (7:0) of the cmp_rslt.

| Bits | Name | Description |
|------|-----------------|-----------------------------|
| 7:0 | comp_rslt1[7:0] | Bits(7:0) of the comp_rslt. |

1.3.1335 P3BA_CMP_RSLT2

CMP_RSLT2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_CMP_RSLT2: 0x40050315

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | comp_rslt2 | | | | | | | |

This register contains bits (15:8) of the comp_rslt.

| Bits | Name | Description |
|------|-----------------|------------------------------|
| 7:0 | comp_rslt2[7:0] | Bits(15:8) of the comp_rslt. |

1.3.1336 P3BA_CMP_RSLT3

CMP_RSLT3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_CMP_RSLT3: 0x40050316

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | comp_rslt3 | | | | | | | |

This register contains bits (23:16) of the comp_rslt.

| Bits | Name | Description |
|------|-----------------|-------------------------------|
| 7:0 | comp_rslt3[7:0] | Bits(23:16) of the comp_rslt. |

1.3.1337 P3BA_CMP_RSLT4

CMP_RSLT4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_CMP_RSLT4: 0x40050317

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | comp_rslt4 | | | | | | | |

This register contains bits (31:24) of the cmp_rslt.

| Bits | Name | Description |
|------|-----------------|-------------------------------|
| 7:0 | comp_rslt4[7:0] | Bits(31:24) of the comp_rslt. |

1.3.1338 P3BA_DATA_REG1

DATA_REG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATA_REG1: 0x40050318

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_reg1 | | | | | | | |

The data register (data_reg) stores the data that is used to write into the target memory. Data can directly be written into the register (and preserved during a memory test by setting data_ovr bit to 1'b1) or can be generated, when a memory test is initiated from the data_pattern, by setting data_ovr bit to 1'b0. This register contains bits (7:0) of the data_reg.

| Bits | Name | Description |
|------|----------------|-------------------------|
| 7:0 | data_reg1[7:0] | Bits (7:0) of the data. |

1.3.1339 P3BA_DATA_REG2

DATA_REG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATA_REG2: 0x40050319

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_reg2 | | | | | | | |

This register contains bits (15:8) of the data_reg.

| Bits | Name | Description |
|------|----------------|--------------------------|
| 7:0 | data_reg2[7:0] | Bits (15:8) of the data. |

1.3.1340 P3BA_DATA_REG3

DATA_REG3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATA_REG3: 0x4005031A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_reg3 | | | | | | | |

This register contains bits (23:16) of the data_reg.

| Bits | Name | Description |
|------|----------------|---------------------------|
| 7:0 | data_reg3[7:0] | Bits (23:16) of the data. |

1.3.1341 P3BA_DATA_REG4

DATA_REG4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATA_REG4: 0x4005031B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data_reg4 | | | | | | | |

This register contains bits (31:24) of the data_reg.

| Bits | Name | Description |
|------|----------------|---------------------------|
| 7:0 | data_reg4[7:0] | Bits (31:24) of the data. |

1.3.1342 P3BA_EXP_DATA1

EXP_DATA1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_EXP_DATA1: 0x4005031C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | exp_data1 | | | | | | | |

The expected data (exp_data) is used to check if the data read from the target memory is correct. The expected data is generated from the data register and other factors including, mstr_hsize, bits24_true, data_invert_mask, abs_addr and opcode. This register contains bits (7:0) of exp_rslt.

| Bits | Name | Description |
|------|----------------|-----------------------------|
| 7:0 | exp_data1[7:0] | Bits (7:0) of the exp_data. |

1.3.1343 P3BA_EXP_DATA2

EXP_DATA2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_EXP_DATA2: 0x4005031D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | exp_data2 | | | | | | | |

This register contains bits (15:8) of exp_rslt.

| Bits | Name | Description |
|------|----------------|------------------------------|
| 7:0 | exp_data2[7:0] | Bits (15:8) of the exp_data. |

1.3.1344 P3BA_EXP_DATA3

EXP_DATA3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_EXP_DATA3: 0x4005031E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | exp_data3 | | | | | | | |

This register contains bits (23:16) of exp_rslt.

| Bits | Name | Description |
|------|----------------|-------------------------------|
| 7:0 | exp_data3[7:0] | Bits (23:16) of the exp_data. |

1.3.1345 P3BA_EXP_DATA4

EXP_DATA4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_EXP_DATA4: 0x4005031F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | exp_data4 | | | | | | | |

This register contains bits (31:24) of exp_rslt.

| Bits | Name | Description |
|------|----------------|-------------------------------|
| 7:0 | exp_data4[7:0] | Bits (31:24) of the exp_data. |

1.3.1346 P3BA_MSTR_HRDATA1

MSTR_HRDATA1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_MSTR_HRDATA1: 0x40050320

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | mstr_hrdata1 | | | | | | | |

When a target memory location is read, the data is returned on the hrdata port on the master AHB interface. This data is registered as master hrdata (mstr_hrdata). This data is compared with exp_data to check if the read data is correct. This register contains bits (7:0) of the mstr_hrdata.

| Bits | Name | Description |
|------|-------------------|--------------------------------|
| 7:0 | mstr_hrdata1[7:0] | Bits (7:0) of the mstr_hrdata. |

1.3.1347 P3BA_MSTR_HRDATA2

MSTR_HRDATA2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_MSTR_HRDATA2: 0x40050321

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | mstr_hrdata2 | | | | | | | |

This register contains bits (15:8) of the mstr_hrdata.

| Bits | Name | Description |
|------|-------------------|---------------------------------|
| 7:0 | mstr_hrdata2[7:0] | Bits (15:8) of the mstr_hrdata. |

1.3.1348 P3BA_MSTR_HRDATA3

MSTR_HRDATA3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_MSTR_HRDATA3: 0x40050322

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | mstr_hrdata3 | | | | | | | |

This register contains bits (23:16) of the mstr_hrdata.

| Bits | Name | Description |
|------|-------------------|----------------------------------|
| 7:0 | mstr_hrdata3[7:0] | Bits (23:16) of the mstr_hrdata. |

1.3.1349 P3BA_MSTR_HRDATA4

MSTR_HRDATA4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_MSTR_HRDATA4: 0x40050323

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | mstr_hrdata4 | | | | | | | |

This register contains bits (31:24) of the mstr_hrdata.

| Bits | Name | Description |
|------|-------------------|----------------------------------|
| 7:0 | mstr_hrdata4[7:0] | Bits (31:24) of the mstr_hrdata. |

1.3.1350 P3BA_BIST_EN

BIST_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_BIST_EN: 0x40050324

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|------------|---------|
| SW Access:Reset | NA:00000 | | | | | R/W:1 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R/W | R/W | R/W |
| Name | | | | | | passing | init_compl | bist_go |

This register is used to store the values for system control and initialization status bit. The `bist_go` bit, when set to 1'b1, initiates a memory test. When `data_ovr` bit is not set and when memory test is initiated, data initialization state is entered. During this state the `data_reg` is updated with `data_pattern` bits and the initialization complete (`init_compl`) bit is set. The passing bit is used to track the pass status of the memory test. Before starting a memory test the bit has to be set to 1'b1 by the software.

| Bits | Name | Description |
|------|------------|--|
| 2 | passing | This bit has to be set to 1'b1 before starting a memory test. During and at the end of a memory test if passing bit is 1'b0: A failure was encountered during the memory test. 1'b1: The memory test passed. |
| 1 | init_compl | 1'b0: When <code>data_ovr</code> bit is set the init state is skipped. The <code>init_compl</code> bit is not set. 1'b1: When <code>data_ovr</code> bit is set the state machine enters init state, replicates data pattern bits in the <code>data_reg</code> and sets <code>init_compl</code> to 1'b1 |
| 0 | bist_go | 1'b0: The block is in slave mode. The slave AHB interface is active. The master AHB interface is inactive. 1'b1: The block enters master mode and a memory test is initiated. The master AHB interface is active. The slave AHB interface is inactive. The default bus master (a microcontroller) is stalled. |

1.3.1351 P3BA_PHUB_MASTER_SSR

PHUB_MASTER_SSR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_PHUB_MASTER_SSR: 0x40050325

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|-------------|------------|---|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:00 | |
| HW Access | NA | | | | | R | R | |
| Name | | | | | | bits24_true | mstr_hsize | |

This register contains the mstr_hsize and bits24_true. The master AHB interface hsize (mstr_hsize) is used to specify the memory access data width. This should be equal to or less than the data width of the target memory. For example, the USB block has a data width of 16 bits then the Bist Assist block can perform a 16 bit memory access or an 8 bit memory access, but not a 32 bit memory access. The bits24_true is used to identify if the target memory is a 24 bit memory.

| Bits | Name | Description |
|------|-----------------|---|
| 2 | bits24_true | This bit is valid only when mstr_hsize is 2'b10. 1'b0: The target memory is a 32 bit memory. 1'b1: The target memory is a 24 bit memory. The MS byte of the data in all memory transactions are ignored |
| 1:0 | mstr_hsize[1:0] | This field is used to identify the size of the spoke for synchronization with PHUB. |

1.3.1352 P3BA_SEQCFG1

SEQCFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_SEQCFG1: 0x40050326

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|----------|---|---|----------|---|---|---------------|
| SW Access:Reset | NA:0 | R/W:000 | | | R/W:000 | | | R/W:1 |
| HW Access | NA | R | | | R | | | R |
| Name | | opcode_2 | | | opcode_1 | | | pre_addresses |

This register is used to store the first two opcodes in the test sequence and the pre_address bit. The two opcodes will perform the first two operations in the state machine after the memory test is initiated. When the pre address bit is set, a single read is executed on the address corresponding to x_roll, y_roll and results ignored, immediately before executing the programmed sequence starting at the address corresponding to x_start, y_start. This provides full address transition coverage.

| Bits | Name | Description |
|------|---------------|---|
| 6:4 | opcode_2[2:0] | second opcode See Table 1-913. |
| 3:1 | opcode_1[2:0] | first opcode See Table 1-913. |
| 0 | pre_address | 1'b0: Pre address state is skipped. Sequence starts from address corresponding to x_address, y_address. 1'b1: Pre address state is entered and a single read on the address corresponding to x_roll, y_roll. |

Table 1-913. Bit field encoding: opcode_enum

| Value | Name | Description |
|--------|----------|---|
| 3'b000 | NOOP | Execute Wait State |
| 3'b011 | RDATA | Execute Read and compare with data |
| 3'b100 | RDATABAR | Execute Read and compare with inverted data |
| 3'b001 | WDATA | Execute Write with data |
| 3'b010 | WDATABAR | Execute Write with inverted data |
| 3'b101 | EXCLUDE | Do not execute anything. Skip opcode. |

1.3.1353 P3BA_SEQCFG2

SEQCFG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_SEQCFG2: 0x40050327

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------|----------|---|---|----------|---|---|
| SW Access:Reset | NA:0 | R/W:0 | R/W:000 | | | R/W:000 | | |
| HW Access | NA | R | R | | | R | | |
| Name | | bist_stop | opcode_4 | | | opcode_3 | | |

This register is used to store the last two opcodes in the test sequence and bist_stop bit. The two opcodes will perform the last two operations in the state machine after the memory test is initiated. The bit stop bit is used to enter the debug mode when a fail is encountered.

| Bits | Name | Description |
|------|---------------|--|
| 6 | bist_stop | 1'b0: The state machine does not stop when a fail is encountered. 1'b1: The state machine stops and enters debug mode when a fail is encountered. |
| 5:3 | opcode_4[2:0] | fourth opcode See Table 1-914. |
| 2:0 | opcode_3[2:0] | third opcode See Table 1-914. |

Table 1-914. Bit field encoding: opcode_enum

| Value | Name | Description |
|--------|----------|---|
| 3'b000 | NOOP | Execute Wait State |
| 3'b011 | RDATA | Execute Read and compare with data |
| 3'b100 | RDATABAR | Execute Read and compare with inverted data |
| 3'b001 | WDATA | Execute Write with data |
| 3'b010 | WDATABAR | Execute Write with inverted data |
| 3'b101 | EXCLUDE | Do not execute anything. Skip opcode. |

1.3.1354 P3BA_Y_CURR

Y_CURR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_Y_CURR: 0x40050328

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-----------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R:0000000 | | | | | | |
| HW Access | NA | R/W | | | | | | |
| Name | | y_curr | | | | | | |

This register is used to store the current Y address value of the target memory. When read in debug mode it corresponds to the column address of the memory location on which the memory test was last done.

| Bits | Name | Description |
|------|-------------|--|
| 6:0 | y_curr[6:0] | This is the current value of Y address. Counter |

1.3.1355 P3BA_X_CURR1

X_CURR1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_X_CURR1: 0x40050329

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | x_curr1 | | | | | | | |

This register is used to store the current X address value of the target memory. When read in debug mode it corresponds to the row address of the memory location on which the memory test was last done. This register is used to store bits [7:0] of the current X address value of the target memory.

| Bits | Name | Description |
|------|--------------|---------------------------------|
| 7:0 | x_curr1[7:0] | Bits (7:0) of x_curr Counter |

1.3.1356 P3BA_X_CURR2

X_CURR2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_X_CURR2: 0x4005032A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | x_curr2 | | | | | | | |

Register is used to store bits [15:8] of the current X address value of the target memory.

| Bits | Name | Description |
|------|--------------|----------------------------------|
| 7:0 | x_curr2[7:0] | Bits (15:8) of x_curr Counter |

1.3.1357 PANTHER_STCALIB_CFG

SYSTICK Calibration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_STCALIB_CFG: 0x40080000

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | TENMS | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | TENMS | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | TENMS | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------|-------|----------|----|----|----|----|----|
| SW Access:Reset | R/W:0 | R/W:0 | R:000000 | | | | | |
| HW Access | R | R | R | | | | | |
| Name | NOREF | SKEW | RESERVED | | | | | |

Note that this register is driven to the NVIC.SYSTICK_CAL register. This register is used to adjust the SYSTICK timer to be exactly 10ms. Note that software should only write to this register during boot and immediately after the clock frequency has been determined for the CPU and the SYSTICK timer reference input. See Chapter 14 of The Definitive Guide to the ARM Cortex-M3.

| Bits | Name | Description |
|-------|---------------|--|
| 31 | NOREF | NOREF is set to 1 when there is no reference clock. Software should use the CPU clock. |
| 30 | SKEW | When SKEW is set to 1, the calibration value is not exactly 10 milliseconds due to the clock frequency. The accuracy of the timer may not be suitable for Real-Time applications. IF the clock period is not an integral number of 10ms then this bit should be set. |
| 29:24 | RESERVED[5:0] | Reserved |
| 23:0 | TENMS[23:0] | Calibration value for the Ten Millisecond timer. This value is normally copied into the RELOAD register by software to achieve 10ms. |

1.3.1358 PANTHER_WAITPIPE

Wait State Pipeline

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_WAITPIPE: 0x40080004

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---------|-------------------|------------|--------|
| SW Access:Reset | R:0000 | | | | R:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | R | | | | R | R | R | R |
| Name | RESERVED | | | | RSERVED | CM3_SYSTCK_SRCSEL | NMI_SRCSEL | BYPASS |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |

Clearing the BYPASS bit institutes a pipeline stage that enables high frequency clock operation. The pipeline should be enabled when the CPU frequency is > 48 MHz. All transactions through the PHUB will incur a 1 cycle wait-state when the pipeline is enabled.

| Bits | Name | Description |
|------|-------------------|---|
| 31:4 | RESERVED[27:0] | Reserved |
| 3 | RSERVED | NA |
| 2 | CM3_SYSTCK_SRCSEL | CM3 SYSTCK clock source selection. 1= DSI clock (connected to dsi_01_out_p_13). 0= 100KHz Slow Clock |
| 1 | NMI_SRCSEL | NMI SOURCE SELECTION. 1=Selects DSI_01_OUT_P_14 as NMI source. 0=Tied-off. Default tied-off. |

1.3.1358 PANTHER_WAITPIPE (continued)

| | | |
|---|--------|--|
| 0 | BYPASS | Wait-state pipeline for high frequency operation. 1=Bypass the pipeline registers: Allowed when CPU frequency \leq 48 MHz 0=Enable pipeline registers: Required when CPU frequency $>$ 48 MHz Note: Once BYPASS bit is cleared or set, make sure at least 2 NOP instructions are executed |
|---|--------|--|

1.3.1359 PANTHER_TRACE_CFG

Debug Trace Configuration

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_TRACE_CFG: 0x40080008

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---|----------------|--------------|
| SW Access:Reset | R:000000 | | | | | | R/W:0 | R/W:0 |
| HW Access | R | | | | | | R | R |
| Name | RESERVED | | | | | | TRACE_M ODE | SWV_MOD E |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |

Enable the Serial Wire Viewer (SWV) mode. Only 1 of the following 2 modes should enabled at a time. If both modes are enabled, then the TRACE mode is output.

| Bits | Name | Description |
|------|----------------|---|
| 31:2 | RESERVED[29:0] | Reserved |
| 1 | TRACE_MODE | Trace Mode. 1=Trace Mode enable. Send Trace Data to GPIO pins P2.7-P2.4. Send TRACECLK to P2.3. 0=Normal operation. Trace disabled. |
| 0 | SWV_MODE | SWV Mode. 1= SWV Mode enable.SWV Data sent onto GPIO pin P2.3. 0= Normal operation.SWV Mode disabled. |

1.3.1360 PANTHER_DBG_CFG

Embedded Trace Overflow Stall

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_DBG_CFG: 0x4008000C

| | | | | | | | | |
|-----------------|------------|-----------|-----------|-----------|-----------|-----------|-------------------------------|---------------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:000000 | | | | | | R/W:0 | R/W:1 |
| HW Access | R | | | | | | R | R |
| Name | RESERVED | | | | | | BOOT_CM3 SYSRST_B YPASS | EMTOF- LOW |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |

Prevent the ETM FIFO from overflowing by stalling the CPU until the FIFO has enough room for more trace data.

| Bits | Name | Description |
|------|---------------------------|---|
| 31:2 | RESERVED[29:0] | Reserved |
| 1 | BOOT_CM3SYSRST_BY PASS | CM3 system reset configuration during boot process 0 --> no effect 1 --> bypasses the CM3 system reset during boot. |
| 0 | EMTOFLOW | The CM3 has built in Embedded Trace logic which compresses the trace data, so it can be transferred in real-time. However, this compression can cause the FIFO in the ETM logic to overflow. When the ETM fifo fills, this bit can be used to either cause the CPU to stall until there is enough room for more data in the FIFO, or to simply loose data and not stall the CPU. 0=CPU will free-run even if the ETM FIFO is full. Trace data will be lost. 1=CPU will stall when the ETM FIFO is full. |

1.3.1361 PANTHER_CM3_LCKRST_STAT

Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_CM3_LCKRST_STAT: 0x40080018

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---|--------------------|--------------------|
| SW Access:Reset | R:000000 | | | | | | RC:0 | RC:0 |
| HW Access | R | | | | | | R/W | R/W |
| Name | RESERVED | | | | | | CM3LOCK UP_STAT | CM3SYSRS T_STAT |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RESERVED | | | | | | | |

This configuration register is used for PVT controller bit fields. The only bit used right now is bit [0].

| Bits | Name | Description |
|------|----------------|---|
| 31:2 | RESERVED[29:0] | Reserved |
| 1 | CM3LOCKUP_STAT | This bit is used to indicate whether CM3 CPU got locked while executing instructions. 1= 1 indicates CM3 CPU got locked-up. 0= 0 Indicates there is no lockup of CM3 CPU |
| 0 | CM3SYSRST_STAT | This bit is used to indicate whether any system reset was requested by CM3. 1= 1 indicates CM3 requested a system reset, will be cleared on reading the register. 0= 0 Indicates there is no system reset request from CM3. |

1.3.1362 PANTHER_DEVICE_ID

Device Identification

Reset: N/A

Register : Address

PANTHER_DEVICE_ID: 0x4008001C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | W | | | | | | | |
| Name | dev_id | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | W | | | | | | | |
| Name | dev_id | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | W | | | | | | | |
| Name | dev_id | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | W | | | | | | | |
| Name | dev_id | | | | | | | |

This register stores the device identification number also known as the JTAG ID.

| Bits | Name | Description |
|------|--------------|---|
| 31:0 | dev_id[31:0] | Stores the device identification number also known as the JTAG ID |

1.3.1363 FLSECC_DATA[0..32767]

DATA

Reset: N/A

Register : Address

FLSECC_DATA: 0x48000000-0x48007FFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|------------------|
| 7:0 | data[7:0] | (no description) |

@0x49000000 + [0..127 * 0x1]

1.3.1364 FLSHID_RSVD[0..127]

RSVD

Reset: N/A

Register : Address

FLSHID_RSVD: 0x49000000-0x4900007F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|------------------|
| 7:0 | RSVD[7:0] | (no description) |

1.3.1365 FLSHID_CUST_MDATA[0..127]

Customer Meta Data

Reset: N/A

Register : Address

FLSHID_CUST_MDATA: 0x49000080-0x490000FF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cust_mdata | | | | | | | |

Contains customer meta data such as information on the programmer used and the build number of the Cypress tool used. See Flash chapter in the IROS for more information on the use of this field and a breakdown of the individual bytes

| Bits | Name | Description |
|------|-----------------|--------------------|
| 7:0 | cust_mdata[7:0] | Customer Meta Data |



0x49000100

1.3.1366 FLSHID_CUST_TABLES_Y_LOC

Y location

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_Y_LOC: 0x49000100

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | y_loc | | | | | | | |

Y location of die on the wafer

| Bits | Name | Description |
|------|------------|---|
| 7:0 | y_loc[7:0] | Y location of die on the wafer (row number) |

1.3.1367 FLSHID_CUST_TABLES_X_LOC

X location

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_X_LOC: 0x49000101

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | x_loc | | | | | | | |

X location of die on the wafer

| Bits | Name | Description |
|------|------------|--|
| 7:0 | x_loc[7:0] | X location of die on the wafer (column number) |



0x49000102

1.3.1368 FLSHID_CUST_TABLES_WAFER_NUM

Wafer Number

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_WAFER_NUM: 0x49000102

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | wafer_num | | | | | | | |

Wafer Number

| Bits | Name | Description |
|------|----------------|-----------------------|
| 7:0 | wafer_num[7:0] | Wafer Number: 1 to 24 |

1.3.1369 FLSHID_CUST_TABLES_LOT_LSB

Lot Number LSB

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_LOT_LSB: 0x49000103

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | lot_Isb | | | | | | | |

Lot Number LSB

| Bits | Name | Description |
|------|--------------|-------------------------------|
| 7:0 | lot_Isb[7:0] | LSB of lot number/wafer start |



0x49000104

1.3.1370 FLSHID_CUST_TABLES_LOT_MSB

Lot Number MSB

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_LOT_MSB: 0x49000104

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | lot_msb | | | | | | | |

Lot Number MSB

| Bits | Name | Description |
|------|--------------|-------------------------------|
| 7:0 | lot_msb[7:0] | MSB of lot number/wafer start |

1.3.1371 FLSHID_CUST_TABLES_WRK_WK

Work Week

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_WRK_WK: 0x49000105

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | work_week | | | | | | | |

Work week

| Bits | Name | Description |
|------|----------------|--------------------|
| 7:0 | work_week[7:0] | Work week: 1 to 53 |



0x49000106

1.3.1372 FLSHID_CUST_TABLES_FAB_YR

Fab/Yr

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_FAB_YR: 0x49000106

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|---|--------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | fab | | | | year | | | |

Fab ID and Year Produced

| Bits | Name | Description |
|------|-----------|--------------------|
| 7:4 | fab[3:0] | Fab Number: 4 or 5 |
| 3:0 | year[3:0] | Year: 0 to 9 |

1.3.1373 FLSHID_CUST_TABLES_MINOR

Minor Part Number

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_MINOR: 0x49000107

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | minor | | | | | | | |

Marketing part number - minor

| Bits | Name | Description |
|------|------------|---|
| 7:0 | minor[7:0] | Marketing part number - minor: 000 to 999 |



0x49000108

1.3.1374 FLSHID_CUST_TABLES_IMO_3MHZ

IMO Trim - 3 MHz

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_IMO_3MHZ: 0x49000108

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | imo_3mhz | | | | | | | |

IMO Frequency Trim - 3 MHz

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | imo_3mhz[7:0] | IMO Frequency Trim - 3 MHz: trim value to write to register IMO.TR1 to trim for 3 MHz setting |

1.3.1375 FLSHID_CUST_TABLES_IMO_6MHZ

IMO Trim - 6 MHz

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_IMO_6MHZ: 0x49000109

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | imo_6mhz | | | | | | | |

IMO Frequency Trim - 6 MHz

| Bits | Name | Description |
|------|---------------|---|
| 7:0 | imo_6mhz[7:0] | IMO Frequency Trim - 6 MHz: trim value to write to register IMO.TR1 to trim for 6 MHz setting |



0x4900010a

1.3.1376 FLSHID_CUST_TABLES_IMO_12MHZ

IMO Trim - 12 MHz

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_IMO_12MHZ: 0x4900010A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | imo_12mhz | | | | | | | |

IMO Frequency Trim - 12 MHz

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | imo_12mhz[7:0] | IMO Frequency Trim - 12 MHz: trim value to write to register IMO.TR1 to trim for 12 MHz setting |

1.3.1377 FLSHID_CUST_TABLES_IMO_24MHZ

IMO Trim - 24 MHz

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_IMO_24MHZ: 0x4900010B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | imo_24mhz | | | | | | | |

IMO Frequency Trim - 24 MHz

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | imo_24mhz[7:0] | IMO Frequency Trim - 24 MHz: trim value to write to register IMO.TR1 to trim for 24 MHz setting |



0x4900010c

1.3.1378 FLSHID_CUST_TABLES_IMO_67MHZ

IMO Trim - 67 MHz

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_IMO_67MHZ: 0x4900010C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | imo_67mhz | | | | | | | |

IMO Frequency Trim - 67 MHz

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | imo_67mhz[7:0] | IMO Frequency Trim - 67 MHz: trim value to write to register IMO.TR1 to trim for 67 MHz setting |

1.3.1379 FLSHID_CUST_TABLES_IMO_80MHZ

IMO Trim - 80 MHz

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_IMO_80MHZ: 0x4900010D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | imo_80mhz | | | | | | | |

IMO Frequency Trim - 80 MHz

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | imo_80mhz[7:0] | IMO Frequency Trim - 80 MHz: trim value to write to register IMO.TR1 to trim for 80 MHz setting |



0x4900010e

1.3.1380 FLSHID_CUST_TABLES_IMO_92MHZ

IMO Trim - 92 MHz

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_IMO_92MHZ: 0x4900010E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | imo_92mhz | | | | | | | |

IMO Frequency Trim - 92 MHz

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | imo_92mhz[7:0] | IMO Frequency Trim - 92 MHz: trim value to write to register IMO.TR1 to trim for 92 MHz setting |

1.3.1381 FLSHID_CUST_TABLES_IMO_USB

IMO Trim - USB Mode

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_IMO_USB: 0x4900010F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | imo_usb | | | | | | | |

IMO Frequency Trim - USB Mode

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | imo_usb[7:0] | IMO Frequency Trim - USB Mode: trim value to write to register IMO.TR1 to trim for USB mode setting |



0x49000110

1.3.1382 FLSHID_CUST_TABLES_CMP0_TR0_HS

CMP0_TR0 High Speed

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_CMP0_TR0_HS: 0x49000110

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cmp0_tr0_hs | | | | | | | |

Trim for CMP0_TR0 for offset high speed mode (mode 1)

| Bits | Name | Description |
|------|------------------|---|
| 7:0 | cmp0_tr0_hs[7:0] | Trim for CMP0_TR0 for offset high speed mode (mode 1) |

1.3.1383 FLSHID_CUST_TABLES_CMP1_TR0_HS

CMP1_TR0 High Speed

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_CMP1_TR0_HS: 0x49000111

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cmp1_tr0_hs | | | | | | | |

Trim for CMP1_TR0 for offset high speed mode (mode 1)

| Bits | Name | Description |
|------|------------------|---|
| 7:0 | cmp1_tr0_hs[7:0] | Trim for CMP1_TR0 for offset high speed mode (mode 1) |



0x49000112

1.3.1384 FLSHID_CUST_TABLES_CMP2_TR0_HS

CMP2_TR0 High Speed

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_CMP2_TR0_HS: 0x49000112

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cmp2_tr0_hs | | | | | | | |

Trim for CMP2_TR0 for offset high speed mode (mode 1)

| Bits | Name | Description |
|------|------------------|---|
| 7:0 | cmp2_tr0_hs[7:0] | Trim for CMP2_TR0 for offset high speed mode (mode 1) |

1.3.1385 FLSHID_CUST_TABLES_CMP3_TR0_HS

CMP3_TR0 High Speed

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_CMP3_TR0_HS: 0x49000113

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cmp3_tr0_hs | | | | | | | |

Trim for CMP3_TR0 for offset high speed mode (mode 1)

| Bits | Name | Description |
|------|------------------|---|
| 7:0 | cmp3_tr0_hs[7:0] | Trim for CMP3_TR0 for offset high speed mode (mode 1) |



0x49000114

1.3.1386 FLSHID_CUST_TABLES_CMP0_TR1_HS

CMP0_TR1 High Speed

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_CMP0_TR1_HS: 0x49000114

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cmp0_tr1_hs | | | | | | | |

Trim for CMP0_TR1 for offset high speed mode (mode 1)

| Bits | Name | Description |
|------|------------------|---|
| 7:0 | cmp0_tr1_hs[7:0] | Trim for CMP0_TR1 for offset high speed mode (mode 1) |

1.3.1387 FLSHID_CUST_TABLES_CMP1_TR1_HS

CMP1_TR1 High Speed

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_CMP1_TR1_HS: 0x49000115

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cmp1_tr1_hs | | | | | | | |

Trim for CMP1_TR1 for offset high speed mode (mode 1)

| Bits | Name | Description |
|------|------------------|---|
| 7:0 | cmp1_tr1_hs[7:0] | Trim for CMP1_TR1 for offset high speed mode (mode 1) |



0x49000116

1.3.1388 FLSHID_CUST_TABLES_CMP2_TR1_HS

CMP2_TR1 High Speed

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_CMP2_TR1_HS: 0x49000116

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cmp2_tr1_hs | | | | | | | |

Trim for CMP2_TR1 for offset high speed mode (mode 1)

| Bits | Name | Description |
|------|------------------|---|
| 7:0 | cmp2_tr1_hs[7:0] | Trim for CMP2_TR1 for offset high speed mode (mode 1) |

1.3.1389 FLSHID_CUST_TABLES_CMP3_TR1_HS

CMP3_TR1 High Speed

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_CMP3_TR1_HS: 0x49000117

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | cmp3_tr1_hs | | | | | | | |

Trim for CMP3_TR1 for offset high speed mode (mode 1)

| Bits | Name | Description |
|------|------------------|---|
| 7:0 | cmp3_tr1_hs[7:0] | Trim for CMP3_TR1 for offset high speed mode (mode 1) |



0x49000118

1.3.1390 FLSHID_CUST_TABLES_DEC_M1

Decimator Trim - Mode 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DEC_M1: 0x49000118

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dec_tr_m1 | | | | | | | |

Decimator Trim - Mode 1

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | dec_tr_m1[7:0] | Decimator Trim - Mode 1: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed. |

1.3.1391 FLSHID_CUST_TABLES_DEC_M2

Decimator Trim - mode 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DEC_M2: 0x49000119

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dec_tr_m2 | | | | | | | |

Decimator Trim - mode 2

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | dec_tr_m2[7:0] | Decimator Trim - mode 2: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed. |



0x4900011a

1.3.1392 FLSHID_CUST_TABLES_DEC_M3

Decimator Trim - mode 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DEC_M3: 0x4900011A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dec_tr_m3 | | | | | | | |

Decimator Trim - mode 3

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | dec_tr_m3[7:0] | Decimator Trim - mode 3: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed. |

1.3.1393 FLSHID_CUST_TABLES_DEC_M4

Decimator Trim - mode 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DEC_M4: 0x4900011B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dec_tr_m4 | | | | | | | |

Decimator Trim - mode 4

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | dec_tr_m4[7:0] | Decimator Trim - mode 4: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed. |



0x4900011c

1.3.1394 FLSHID_CUST_TABLES_DEC_M5

Decimator Trim - mode 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DEC_M5: 0x4900011C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dec_tr_m5 | | | | | | | |

Decimator Trim - mode 5

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | dec_tr_m5[7:0] | Decimator Trim - mode 5: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed. |

1.3.1395 FLSHID_CUST_TABLES_DEC_M6

Decimator Trim - mode 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DEC_M6: 0x4900011D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dec_tr_m6 | | | | | | | |

Decimator Trim - mode 6

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | dec_tr_m6[7:0] | Decimator Trim - mode 6: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed. |



0x4900011e

1.3.1396 FLSHID_CUST_TABLES_DEC_M7

Decimator Trim - Mode 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DEC_M7: 0x4900011E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dec_tr_m7 | | | | | | | |

Decimator Trim - Mode 7

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | dec_tr_m7[7:0] | Decimator Trim - Mode 7: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed. |

1.3.1397 FLSHID_CUST_TABLES_DEC_M8

Decimator Trim - Mode 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DEC_M8: 0x4900011F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dec_tr_m8 | | | | | | | |

Decimator Trim - Mode 8

| Bits | Name | Description |
|------|----------------|---|
| 7:0 | dec_tr_m8[7:0] | Decimator Trim - Mode 8: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed. |



0x49000120

1.3.1398 FLSHID_CUST_TABLES_DAC0_M1

DAC0_TR Trim - Mode 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC0_M1: 0x49000120

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac0_m1 | | | | | | | |

DAC0_TR Trim - Mode 1

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac0_m1[7:0] | DAC0_TR Trim - Mode 1 |

1.3.1399 FLSHID_CUST_TABLES_DAC0_M2

DAC0_TR Trim - mode 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC0_M2: 0x49000121

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac0_m2 | | | | | | | |

DAC0_TR Trim - mode 2

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac0_m2[7:0] | DAC0_TR Trim - mode 2 |



0x49000122

1.3.1400 FLSHID_CUST_TABLES_DAC0_M3

DAC0_TR Trim - mode 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC0_M3: 0x49000122

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac0_m3 | | | | | | | |

DAC0_TR Trim - mode 3

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac0_m3[7:0] | DAC0_TR Trim - mode 3 |

1.3.1401 FLSHID_CUST_TABLES_DAC0_M4

DAC0_TR Trim - mode 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC0_M4: 0x49000123

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac0_m4 | | | | | | | |

DAC0_TR Trim - mode 4

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac0_m4[7:0] | DAC0_TR Trim - mode 4 |



0x49000124

1.3.1402 FLSHID_CUST_TABLES_DAC0_M5

DAC0_TR Trim - mode 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC0_M5: 0x49000124

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac0_m5 | | | | | | | |

DAC0_TR Trim - mode 5

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac0_m5[7:0] | DAC0_TR Trim - mode 5 |

1.3.1403 FLSHID_CUST_TABLES_DAC0_M6

DAC0_TR Trim - mode 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC0_M6: 0x49000125

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac0_m6 | | | | | | | |

DAC0_TR Trim - mode 6

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac0_m6[7:0] | DAC0_TR Trim - mode 6 |



0x49000126

1.3.1404 FLSHID_CUST_TABLES_DAC0_M7

DAC0_TR Trim - mode 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC0_M7: 0x49000126

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac0_m7 | | | | | | | |

DAC0_TR Trim - mode 7

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac0_m7[7:0] | DAC0_TR Trim - mode 7 |

1.3.1405 FLSHID_CUST_TABLES_DAC0_M8

DAC0_TR Trim - mode 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC0_M8: 0x49000127

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac0_m8 | | | | | | | |

DAC0_TR Trim - mode 8

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac0_m8[7:0] | DAC0_TR Trim - mode 8 |



0x49000128

1.3.1406 FLSHID_CUST_TABLES_DAC2_M1

DAC2_TR Trim - Mode 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC2_M1: 0x49000128

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac2_m1 | | | | | | | |

DAC2_TR Trim - Mode 1

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac2_m1[7:0] | DAC2_TR Trim - Mode 1 |

1.3.1407 FLSHID_CUST_TABLES_DAC2_M2

DAC2_TR Trim - mode 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC2_M2: 0x49000129

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac2_m2 | | | | | | | |

DAC2_TR Trim - mode 2

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac2_m2[7:0] | DAC2_TR Trim - mode 2 |



0x4900012a

1.3.1408 FLSHID_CUST_TABLES_DAC2_M3

DAC2_TR Trim - mode 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC2_M3: 0x4900012A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac2_m3 | | | | | | | |

DAC2_TR Trim - mode 3

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac2_m3[7:0] | DAC2_TR Trim - mode 3 |

1.3.1409 FLSHID_CUST_TABLES_DAC2_M4

DAC2_TR Trim - mode 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC2_M4: 0x4900012B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac2_m4 | | | | | | | |

DAC2_TR Trim - mode 4

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac2_m4[7:0] | DAC2_TR Trim - mode 4 |



0x4900012c

1.3.1410 FLSHID_CUST_TABLES_DAC2_M5

DAC2_TR Trim - mode 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC2_M5: 0x4900012C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac2_m5 | | | | | | | |

DAC2_TR Trim - mode 5

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac2_m5[7:0] | DAC2_TR Trim - mode 5 |

1.3.1411 FLSHID_CUST_TABLES_DAC2_M6

DAC2_TR Trim - mode 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC2_M6: 0x4900012D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac2_m6 | | | | | | | |

DAC2_TR Trim - mode 6

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac2_m6[7:0] | DAC2_TR Trim - mode 6 |



0x4900012e

1.3.1412 FLSHID_CUST_TABLES_DAC2_M7

DAC2_TR Trim - mode 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC2_M7: 0x4900012E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac2_m7 | | | | | | | |

DAC2_TR Trim - mode 7

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac2_m7[7:0] | DAC2_TR Trim - mode 7 |

1.3.1413 FLSHID_CUST_TABLES_DAC2_M8

DAC2_TR Trim - mode 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC2_M8: 0x4900012F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac2_m8 | | | | | | | |

DAC2_TR Trim - mode 8

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac2_m8[7:0] | DAC2_TR Trim - mode 8 |



0x49000130

1.3.1414 FLSHID_CUST_TABLES_DAC1_M1

DAC1_TR Trim - Mode 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC1_M1: 0x49000130

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac1_m1 | | | | | | | |

DAC1_TR Trim - Mode 1

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac1_m1[7:0] | DAC1_TR Trim - Mode 1 |

1.3.1415 FLSHID_CUST_TABLES_DAC1_M2

DAC1_TR Trim - mode 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC1_M2: 0x49000131

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac1_m2 | | | | | | | |

DAC1_TR Trim - mode 2

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac1_m2[7:0] | DAC1_TR Trim - mode 2 |



0x49000132

1.3.1416 FLSHID_CUST_TABLES_DAC1_M3

DAC1_TR Trim - mode 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC1_M3: 0x49000132

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac1_m3 | | | | | | | |

DAC1_TR Trim - mode 3

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac1_m3[7:0] | DAC1_TR Trim - mode 3 |

1.3.1417 FLSHID_CUST_TABLES_DAC1_M4

DAC1_TR Trim - mode 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC1_M4: 0x49000133

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac1_m4 | | | | | | | |

DAC1_TR Trim - mode 4

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac1_m4[7:0] | DAC1_TR Trim - mode 4 |



0x49000134

1.3.1418 FLSHID_CUST_TABLES_DAC1_M5

DAC1_TR Trim - mode 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC1_M5: 0x49000134

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac1_m5 | | | | | | | |

DAC1_TR Trim - mode 5

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac1_m5[7:0] | DAC1_TR Trim - mode 5 |

1.3.1419 FLSHID_CUST_TABLES_DAC1_M6

DAC1_TR Trim - mode 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC1_M6: 0x49000135

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac1_m6 | | | | | | | |

DAC1_TR Trim - mode 6

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac1_m6[7:0] | DAC1_TR Trim - mode 6 |



0x49000136

1.3.1420 FLSHID_CUST_TABLES_DAC1_M7

DAC1_TR Trim - mode 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC1_M7: 0x49000136

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac1_m7 | | | | | | | |

DAC1_TR Trim - mode 7

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac1_m7[7:0] | DAC1_TR Trim - mode 7 |

1.3.1421 FLSHID_CUST_TABLES_DAC1_M8

DAC1_TR Trim - mode 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC1_M8: 0x49000137

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac1_m8 | | | | | | | |

DAC1_TR Trim - mode 8

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac1_m8[7:0] | DAC1_TR Trim - mode 8 |



0x49000138

1.3.1422 FLSHID_CUST_TABLES_DAC3_M1

DAC3_TR Trim - Mode 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC3_M1: 0x49000138

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac3_m1 | | | | | | | |

DAC3_TR Trim - Mode 1

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac3_m1[7:0] | DAC3_TR Trim - Mode 1 |

1.3.1423 FLSHID_CUST_TABLES_DAC3_M2

DAC3_TR Trim - mode 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC3_M2: 0x49000139

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac3_m2 | | | | | | | |

DAC3_TR Trim - mode 2

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac3_m2[7:0] | DAC3_TR Trim - mode 2 |



0x4900013a

1.3.1424 FLSHID_CUST_TABLES_DAC3_M3

DAC3_TR Trim - mode 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC3_M3: 0x4900013A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac3_m3 | | | | | | | |

DAC3_TR Trim - mode 3

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac3_m3[7:0] | DAC3_TR Trim - mode 3 |

1.3.1425 FLSHID_CUST_TABLES_DAC3_M4

DAC3_TR Trim - mode 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC3_M4: 0x4900013B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac3_m4 | | | | | | | |

DAC3_TR Trim - mode 4

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac3_m4[7:0] | DAC3_TR Trim - mode 4 |



0x4900013c

1.3.1426 FLSHID_CUST_TABLES_DAC3_M5

DAC3_TR Trim - mode 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC3_M5: 0x4900013C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac3_m5 | | | | | | | |

DAC3_TR Trim - mode 5

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac3_m5[7:0] | DAC3_TR Trim - mode 5 |

1.3.1427 FLSHID_CUST_TABLES_DAC3_M6

DAC3_TR Trim - mode 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC3_M6: 0x4900013D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac3_m6 | | | | | | | |

DAC3_TR Trim - mode 6

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac3_m6[7:0] | DAC3_TR Trim - mode 6 |



0x4900013e

1.3.1428 FLSHID_CUST_TABLES_DAC3_M7

DAC3_TR Trim - mode 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC3_M7: 0x4900013E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac3_m7 | | | | | | | |

DAC3_TR Trim - mode 7

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac3_m7[7:0] | DAC3_TR Trim - mode 7 |

1.3.1429 FLSHID_CUST_TABLES_DAC3_M8

DAC3_TR Trim - mode 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_DAC3_M8: 0x4900013F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | dac3_m8 | | | | | | | |

DAC3_TR Trim - mode 8

| Bits | Name | Description |
|------|--------------|-----------------------|
| 7:0 | dac3_m8[7:0] | DAC3_TR Trim - mode 8 |

@0x49000140 + [0..31 * 0x1]

1.3.1430 FLSHID_PETE_DATA[0..31]

PE/TE Data

Reset: N/A

Register : Address

FLSHID_PETE_DATA: 0x49000140-0x4900015F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | pete_data | | | | | | | |

(no description)

The manufacturing process for a PSoC device generates die unique data that needs to be stored in a nonvolatile location to support tracking through the manufacturing process and potential failure analysis of returned parts. This data is stored here. See Flash chapter in the IROS for more information on the use of this field and a breakdown of the individual bytes

| Bits | Name | Description |
|------|----------------|-------------|
| 7:0 | pete_data[7:0] | PE/TE Data |

1.3.1431 FLSHID_SPC_PARAMS[0..31]

SPC Parameters

Reset: N/A

Register : Address

FLSHID_SPC_PARAMS: 0x49000160-0x4900017F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | spc_params | | | | | | | |

(no description)

Parameters used by the SPC to implement its commands. Data is die specific and determined at sort.

| Bits | Name | Description |
|------|-----------------|----------------|
| 7:0 | spc_params[7:0] | SPC Parameters |



0x49000180

1.3.1432 FLSHID_MFG_CFG_WNDG_CFG0

MLOGIC_WNDG_CFG0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_WNDG_CFG0: 0x49000180

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11100000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1433 FLSHID_MFG_CFG_WNDG_CFG1

MLOGIC_WNDG_CFG1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_WNDG_CFG1: 0x49000182

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11100001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x49000184

1.3.1434 FLSHID_MFG_CFG_PWRSYS_BG_TR PWRSYS_BG_TR Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_BG_TR: 0x49000184

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10001000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1435 FLSHID_MFG_CFG_RESET_TR

RESET_TR Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_RESET_TR: 0x49000186

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11111110 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x49000188

1.3.1436 FLSHID_MFG_CFG_IMO_TR1

IMO_TR1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_IMO_TR1: 0x49000188

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10100001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

IMO Trim for 48 MHz frequency setting

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1437 FLSHID_MFG_CFG_IMO_GAIN

IMO_GAIN Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_IMO_GAIN: 0x4900018A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10100010 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x4900018c

1.3.1438 FLSHID_MFG_CFG_IMO_TR2

IMO_TR2 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_IMO_TR2: 0x4900018C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10100100 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1439 FLSHID_MFG_CFG_IMO_C36M

IMO_C36M Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_IMO_C36M: 0x4900018E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10100011 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x49000190

1.3.1440 FLSHID_MFG_CFG_PWRSYS_BREF_TR PWRSYS_BREF_TR Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_BREF_TR: 0x49000190

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10000111 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1441 FLSHID_MFG_CFG_PWRSYS_BUZZ_TR

PWRSYS_BUZZ_TR Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_BUZZ_TR: 0x49000192

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10000100 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x49000194

1.3.1442 FLSHID_MFG_CFG_PWRSYS_I2C_TR PWRSYS_I2C_TR Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_I2C_TR: 0x49000194

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10000010 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1443 FLSHID_MFG_CFG_PWRSYS_HIB_TR0

PWRSYS_HIB_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_HIB_TR0: 0x49000196

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x49000198

1.3.1444 FLSHID_MFG_CFG_PWRSYS_HIB_TR1

PWRSYS_HIB_TR1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_HIB_TR1: 0x49000198

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10000001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1445 FLSHID_MFG_CFG_PWRSYS_SLP_TR

PWRSYS_SLP_TR Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_SLP_TR: 0x4900019A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10000011 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

0x4900019c

1.3.1446 FLSHID_MFG_CFG_ILO_TR0

ILO_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_ILO_TR0: 0x4900019C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10010000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1447 FLSHID_MFG_CFG_ILO_TR1

ILO_TR1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_ILO_TR1: 0x4900019E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10010001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

0x490001a0

1.3.1448 FLSHID_MFG_CFG_X32_TR X32_TR Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_X32_TR: 0x490001A0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10011000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1449 FLSHID_MFG_CFG_XMHZ_TR

XMHZ_TR Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_XMHZ_TR: 0x490001A2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10101000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x490001a4

1.3.1450 FLSHID_MFG_CFG_OPAMP0_TR0 OPAMP0_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_OPAMP0_TR0: 0x490001A4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00100000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1451 FLSHID_MFG_CFG_OPAMP1_TR0

OPAMP1_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_OPAMP1_TR0: 0x490001A6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00100010 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x490001a8

1.3.1452 FLSHID_MFG_CFG_OPAMP2_TR0 OPAMP2_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_OPAMP2_TR0: 0x490001A8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00100100 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1453 FLSHID_MFG_CFG_OPAMP3_TR0

OPAMP3_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_OPAMP3_TR0: 0x490001AA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00100110 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x490001ac

1.3.1454 FLSHID_MFG_CFG_CMP0_TR0

CMP0_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_CMP0_TR0: 0x490001AC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00110000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

Comparator Trim for Offset Low Speed Mode (Mode 0)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1455 FLSHID_MFG_CFG_CMP1_TR0

CMP1_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_CMP1_TR0: 0x490001AE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00110010 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

Comparator Trim for Offset Low Speed Mode (Mode 0)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

0x490001b0

1.3.1456 FLSHID_MFG_CFG_CMP2_TR0 CMP2_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_CMP2_TR0: 0x490001B0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00110100 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

Comparator Trim for Offset Low Speed Mode (Mode 0)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1457 FLSHID_MFG_CFG_CMP3_TR0

CMP3_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_CMP3_TR0: 0x490001B2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00110110 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

Comparator Trim for Offset Low Speed Mode (Mode 0)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x490001b4

1.3.1458 FLSHID_MFG_CFG_CMP0_TR1

CMP0_TR1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_CMP0_TR1: 0x490001B4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00110001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

Comparator Trim for Offset Low Speed Mode (Mode 0)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1459 FLSHID_MFG_CFG_CMP1_TR1

CMP1_TR1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_CMP1_TR1: 0x490001B6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00110011 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

Comparator Trim for Offset Low Speed Mode (Mode 0)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x490001b8

1.3.1460 FLSHID_MFG_CFG_CMP2_TR1 CMP2_TR1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_CMP2_TR1: 0x490001B8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00110101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

Comparator Trim for Offset Low Speed Mode (Mode 0)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1461 FLSHID_MFG_CFG_CMP3_TR1

CMP3_TR1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_CMP3_TR1: 0x490001BA

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00110111 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

Comparator Trim for Offset Low Speed Mode (Mode 0)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

0x490001bc

1.3.1462 FLSHID_MFG_CFG_IPOR_CR0

IPOR_CR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_IPOR_CR0: 0x490001BC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11110000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1463 FLSHID_MFG_CFG_IPOR_CR1

IPOR_CR1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_IPOR_CR1: 0x490001BE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11110001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x490001c0

1.3.1464 FLSHID_MFG_CFG_IPOR_CR2

IPOR_CR2 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_IPOR_CR2: 0x490001C0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11110010 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1465 FLSHID_MFG_CFG_IPOR_CR3

IPOR_CR3 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_IPOR_CR3: 0x490001C2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11110011 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x490001c4

1.3.1466 FLSHID_MFG_CFG_DLY

DLY Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_DLY: 0x490001C4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

This addr-data pair maps indirectly to register CLKDIST_DLY0 through register DLY to allow the bootloader access the the CLKDIST_DLY0 register.

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1467 FLSHID_MFG_CFG_RESERVED[0..3]

Reserved

Reset: N/A

Register : Address

FLSHID_MFG_CFG_RESERVED0: 0x490001C6

FLSHID_MFG_CFG_RESERVED1: 0x490001C8

FLSHID_MFG_CFG_RESERVED2: 0x490001CA

FLSHID_MFG_CFG_RESERVED3: 0x490001CC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | | | | | | | | |

(no description)

| Bits | Name | Description |
|------|------------|-------------|
| 15:0 | RSVD[15:0] | reserved |



0x490001ce

1.3.1468 FLSHID_MFG_CFG_BG_XOVER_INL_TRIM

Bandgap Crossover Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_BG_XOVER_INL_TRIM: 0x490001CE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:11100010 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

Used to trim registers BG_DFT0 and BG_DFT1 in User Mode

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1469 FLSHID_MFG_CFG_RSVD[0..15]

Reserved

Reset: N/A

Register : Address

FLSHID_MFG_CFG_RSVD0: 0x490001D0
 FLSHID_MFG_CFG_RSVD1: 0x490001D2
 FLSHID_MFG_CFG_RSVD2: 0x490001D4
 FLSHID_MFG_CFG_RSVD3: 0x490001D6
 FLSHID_MFG_CFG_RSVD4: 0x490001D8
 FLSHID_MFG_CFG_RSVD5: 0x490001DA
 FLSHID_MFG_CFG_RSVD6: 0x490001DC
 FLSHID_MFG_CFG_RSVD7: 0x490001DE
 FLSHID_MFG_CFG_RSVD8: 0x490001E0
 FLSHID_MFG_CFG_RSVD9: 0x490001E2
 FLSHID_MFG_CFG_RSVD10: 0x490001E4
 FLSHID_MFG_CFG_RSVD11: 0x490001E6
 FLSHID_MFG_CFG_RSVD12: 0x490001E8
 FLSHID_MFG_CFG_RSVD13: 0x490001EA
 FLSHID_MFG_CFG_RSVD14: 0x490001EC
 FLSHID_MFG_CFG_RSVD15: 0x490001EE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | | | | | | | | |

(no description)

| Bits | Name | Description |
|------|------------|-------------|
| 15:0 | RSVD[15:0] | reserved |



0x490001f0

1.3.1470 FLSHID_MFG_CFG_PWRSYS_WAKE_TR0

PWRSYS_WAKE_TR0 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_WAKE_TR0: 0x490001F0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10000101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1471 FLSHID_MFG_CFG_PWRSYS_WAKE_TR1

PWRSYS_WAKE_TR1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_WAKE_TR1: 0x490001F2

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10000110 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |



0x490001f4

1.3.1472 FLSHID_MFG_CFG_PWRSYS_WAKE_TR2

PWRSYS_WAKE_TR2 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_WAKE_TR2: 0x490001F4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10001001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

1.3.1473 FLSHID_MFG_CFG_PWRSYS_WAKE_TR3

PWRSYS_WAKE_TR3 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_PWRSYS_WAKE_TR3: 0x490001F6

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10001010 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | addr | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---------------------------------|
| 15:8 | data[7:0] | Data byte to write to address |
| 7:0 | addr[7:0] | Address offset to add to 0x4600 |

@0x490001f8 + [0..2 * 0x2]

1.3.1474 FLSHID_MFG_CFG_RSVD_2[0..2]

Reserved

Reset: N/A

Register : Address

FLSHID_MFG_CFG_RSVD_20: 0x490001F8
 FLSHID_MFG_CFG_RSVD_21: 0x490001FA
 FLSHID_MFG_CFG_RSVD_22: 0x490001FC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | | | | | | | | |

(no description)

| Bits | Name | Description |
|------|------------|-------------|
| 15:0 | RSVD[15:0] | reserved |

1.3.1475 FLSHID_MFG_CFG_CHKSM

Boot Checksum

Reset: N/A

Register : Address

FLSHID_MFG_CFG_CHKSM: 0x490001FE

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | checksum | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | checksum | | | | | | | |

16-bit checksum used to verify data contents in the rest of the manufacturing configuration data at chip boot.

| Bits | Name | Description |
|------|----------------|---------------|
| 15:0 | checksum[15:0] | Boot Checksum |

1.3.1476 EXTMEM_DATA[0..8388607]

DATA

Reset: N/A

Register : Address

EXTMEM_DATA: 0x60000000-0x607FFFFF

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | data | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|------------------|
| 7:0 | data[7:0] | (no description) |

1.3.1477 ITM_TRACE_EN

ITM Trace Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_TRACE_EN: 0xE0000E00

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | STIMENA | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | STIMENA | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | STIMENA | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | STIMENA | | | | | | | |

Use the Trace Enable Register to generate trace data by writing to the corresponding stimulus port.

| Bits | Name | Description |
|------|---------------|--|
| 31:0 | STIMENA[31:0] | Bit mask to enable tracing on ITM stimulus ports. One bit per stimulus port. |

1.3.1478 ITM_TRACE_PRIVILEGE

ITM Trace Privilege Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_TRACE_PRIVILEGE: 0xE0000E40

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R/W | | | |
| Name | | | | | PRIVMASK | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the ITM Trace Privilege Register to enable an operating system to control which stimulus ports are accessible by user code.

| Bits | Name | Description |
|------|---------------|--|
| 3:0 | PRIVMASK[3:0] | Bit mask to enable tracing on ITM stimulus ports: bit [0] = stimulus ports [7:0] bit [1] = stimulus ports [15:8] bit [2] = stimulus ports [23:16] bit [3] = stimulus ports [31:24] |

1.3.1479 ITM_TRACE_CTRL

ITM Trace Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_TRACE_CTRL: 0xE0000E80

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|--------|--------|---------|-------|--------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R/W | R/W | R/W | R/W | R/W |
| Name | | | | SWOENA | DWTENA | SYNCENA | TSENA | ITMENA |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-----------|----|----|----|----|----|------------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R/W | |
| Name | | | | | | | TSPrescale | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------|-------------|----|----|----|----|----|----|
| SW Access:Reset | R/W:0 | R/W:0000000 | | | | | | |
| HW Access | R/W | R/W | | | | | | |
| Name | BUSY | ATBID | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use this register to configure and control ITM transfers.

| Bits | Name | Description |
|-------|-----------------|---|
| 23 | BUSY | Set when ITM events present and being drained |
| 22:16 | ATBID[6:0] | ATB ID for CoreSight system. |
| 9:8 | TSPrescale[1:0] | Timestamp prescaler: 0b00 = no prescaling 0b01 = divide by 4 0b10 = divide by 16 0b11 = divide by 64. |
| 4 | SWOENA | Enable SWV behavior - count on TPIUEMIT and TPIUBAUD. |
| 3 | DWTENA | Enables the DWT stimulus. |
| 2 | SYNCENA | Enables sync packets for TPIU. |
| 1 | TSENA | Enables differential timestamps. Differential timestamps are emitted when a packet is written to the FIFO with a non-zero timestamp counter, and when the timestamp counter overflows. Timestamps are emitted during idle times after a fixed number of cycles. This provides a time reference for packets and inter-packet gaps. |

1.3.1479 ITM_TRACE_CTRL (continued)

| | | |
|---|--------|---|
| 0 | ITMENA | Enable ITM. This is the master enable, and must be set before ITM Stimulus and Trace Enable registers can be written. |
|---|--------|---|

1.3.1480 ITM_LOCK_ACCESS

ITM Lock Access Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_LOCK_ACCESS: 0xE0000FB0

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | lock_access | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | lock_access | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | lock_access | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | lock_access | | | | | | | |

Use this register to prevent write accesses to the Control Register.

| Bits | Name | Description |
|------|-------------------|---|
| 31:0 | lock_access[31:0] | A privileged write of 0xC5ACCE55 enables more write access to Control Register 0xE00::0xFFC. An invalid write removes write access. |

1.3.1481 ITM_LOCK_STATUS

ITM Lock Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_LOCK_STATUS: 0xE0000FB4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|---------|--------|---------|
| SW Access:Reset | NA:00000 | | | | | R:0 | R:0 | R:0 |
| HW Access | NA | | | | | R/W | R/W | R/W |
| Name | | | | | | ByteAcc | Access | Present |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use this register to enable write accesses to the Control Register.

| Bits | Name | Description |
|------|---------|--|
| 2 | ByteAcc | You cannot implement 8-bit lock accesses. |
| 1 | Access | Write access to component is blocked. All writes are ignored, reads are permitted. |
| 0 | Present | Indicates that a lock mechanism exists for this component. |

1.3.1482 ITM_PID4

ITM Peripheral Identification Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID4: 0xE000FD0

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000100 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID4 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID4[7:0] | Peripheral Identification Register 4 |

1.3.1483 ITM_PID5

ITM Peripheral Identification Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID5: 0xE000FD4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID5 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID5[7:0] | Peripheral Identification Register 5 |

1.3.1484 ITM_PID6

ITM Peripheral Identification Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID6: 0xE000FD8

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID6 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID6[7:0] | Peripheral Identification Register 6 |

1.3.1485 ITM_PID7

ITM Peripheral Identification Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID7: 0xE000FDC

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID7 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID7[7:0] | Peripheral Identification Register 7 |

1.3.1486 ITM_PID0

ITM Peripheral Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID0: 0xE000FE0

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID0[7:0] | Peripheral Identification Register 0 |

1.3.1487 ITM_PID1

ITM Peripheral Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID1: 0xE000FE4

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:10110000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID1 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID1[7:0] | Peripheral Identification Register 1 |

1.3.1488 ITM_PID2

ITM Peripheral Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID2: 0xE000FE8

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00111011 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID2 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID2[7:0] | Peripheral Identification Register 2 |

1.3.1489 ITM_PID3

ITM Peripheral Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID3: 0xE000FEC

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID3 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID3[7:0] | Peripheral Identification Register 3 |

1.3.1490 ITM_CID0

ITM Component Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_CID0: 0xE0000FF0

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00001101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID0[7:0] | Component Identification Register 0 |

1.3.1491 ITM_CID1

ITM Component Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_CID1: 0xE000FF4

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:11100000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID1 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID1[7:0] | Component Identification Register 1 |

1.3.1492 ITM_CID2

ITM Component Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_CID2: 0xE000FF8

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID2 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID2[7:0] | Component Identification Register 2 |

1.3.1493 ITM_CID3

ITM Component Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_CID3: 0xE000FFC

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:10110001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID3 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID3[7:0] | Component Identification Register 3 |

1.3.1494 DWT_CTRL

DWT Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_CTRL: 0xE0001000

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|------------|---|---|------------|---|
| SW Access:Reset | R/W:000 | | | R/W:0000 | | | R/W:0 | |
| HW Access | R/W | | | R/W | | | R/W | |
| Name | POSTCNT | | | POSTPRESET | | | CYCCNTE-NA | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------|----|----|------------------|---------|----|--------|---------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:00 | | R/W:0 | R/W:0 |
| HW Access | NA | | | R/W | R/W | | R/W | R/W |
| Name | | | | PCSAM- PLEENA | SYNCTAP | | CYCTAP | POSTCNT |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------|----------|-----------------|-----------------|------------------|----------------|----------------|----------------|
| SW Access:Reset | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | | CYCEVTEN | FOLDEVTE- NA | LSJUEVTE- NA | SLEEPE- VTENA | EXCEVTE- NA | CPIEVTE- NA | EXCTRCE- NA |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|----|----|---------|----|----|----|
| SW Access:Reset | R:0100 | | | | NA:0000 | | | |
| HW Access | R/W | | | | NA | | | |
| Name | NUMCOMP | | | | | | | |

Use the DWT Control Register to enable the DWT unit.

| Bits | Name | Description |
|-------|--------------|--|
| 31:28 | NUMCOMP[3:0] | Number of comparators field. This read-only field contains b0100 to indicate four comparators. |
| 22 | CYCEVTEN | Enables Cycle count event. Emits an event when the POSTCNT counter triggers it. See CYCTAP (bit [9]) and POSTPRESET, bits [4:1], for details. 1 = Cycle count events enabled 0 = Cycle count events disabled. This event is only emitted if PCSAMPLENA, bit [12], is disabled. PCSAMPLENA overrides the setting of this bit. Reset clears the CYCEVTENA bit. |
| 21 | FOLDEVTE-NA | Enables Folded instruction count event. Emits an event when DWT_FOLDCNT overflows (every 256 cycles of folded instructions). A folded instruction is one that does not incur even one cycle to execute. For example, an IT instruction is folded away and so does not use one cycle. 1 = Folded instruction count events enabled. 0 = Folded instruction count events disabled. Reset clears the FOLDEVTE-NA bit. |

1.3.1494 DWT_CTRL (continued)

| | | |
|-------|--------------|---|
| 20 | LSUEVTENA | Enables LSU count event. Emits an event when DWT_LSUCNT overflows (every 256 cycles of LSU operation). LSU counts include all LSU costs after the initial cycle for the instruction. 1 = LSU count events enabled. 0 = LSU count events disabled. Reset clears the LSUEVTENA bit. |
| 19 | SLEEPEVTENA | Enables Sleep count event. Emits an event when DWT_SLEEP CNT overflows (every 256 cycles that the processor is sleeping). 1 = Sleep count events enabled. 0 = Sleep count events disabled. Reset clears the SLEEPEVTENA bit. |
| 18 | EXCEVTENA | Enables Interrupt overhead event. Emits an event when DWT_EXCCNT overflows (every 256 cycles of interrupt overhead). 1 = Interrupt overhead event enabled. 0 = Interrupt overhead event disabled. Reset clears the EXCEVTENA bit. |
| 17 | CPIEVTENA | Enables CPI count event. Emits an event when DWT_CPICNT overflows (every 256 cycles of multi-cycle instructions). 1 = CPI counter events enabled. 0 = CPI counter events disabled. Reset clears the CPIEVTENA bit. |
| 16 | EXCTRCENA | Enables Interrupt event tracing: 1 = interrupt event trace enabled 0 = interrupt event trace disabled. Reset clears the EXCEVTENA bit. |
| 12 | PCSAMPLEENA | Enables PC Sampling event. A PC sample event is emitted when the POSTCNT counter triggers it. See CYCTAP, bit [9], and POSTPRESET, bits [4:1], for details. Enabling this bit overrides CYCEVTENA (bit [20]). 1 = PC Sampling event enabled. 0 = PC Sampling event disabled. Reset clears the PCSAMPLEENA bit. |
| 11:10 | SYNCTAP[1:0] | Feeds a synchronization pulse to the ITM SYNCENA control. The value selected here picks the rate (approximately 1/second or less) by selecting a tap on the DWT_CYCCNT register. To use synchronization (heartbeat and hot-connect synchronization), CYCCNTENA must be set to 1, SYNCTAP must be set to one of its values, and SYNCENA must be set to 1. 0b00 = Disabled. No synch counting. 0b01 = Tap at CYCCNT bit 24. 0b10 = Tap at CYCCNT bit 26. 0b11 = Tap at CYCCNT bit 28. |
| 9 | CYCTAP | Selects a tap on the DWT_CYCCNT register. These are spaced at bits [6] and [10]: CYCTAP = 0 selects bit [6] to tap CYCTAP = 1 selects bit [10] to tap. When the selected bit in the CYCCNT register changes from 0 to 1 or 1 to 0, it emits into the POSTCNT, bits [8:5], post-scalar counter. That counter then counts down. On a bit change when post-scalar is 0, it triggers an event for PC sampling or CYCEVTCNT. |
| 8:5 | POSTCNT[3:0] | Post-scalar counter for CYCTAP. When the selected tapped bit changes from 0 to 1 or 1 to 0, the post scalar counter is down-counted when not 0. If 0, it triggers an event for PCSAMPLEENA or CYCEVTENA use. It also reloads with the value from POSTPRESET (bits [4:1]). |

1.3.1494 DWT_CTRL (continued)

| | | |
|-----|-----------------|---|
| 4:1 | POSTPRESET[3:0] | Reload value for POSTCNT, bits [8:5], post-scalar counter. If this value is 0, events are triggered on each tap change (a power of 2, such as $1 \ll 6$ or $1 \ll 10$). If this field has a non-0 value, this forms a count-down value, to be reloaded into POSTCNT each time it reaches 0. For example, a value 1 in this register means an event is formed every other tap change. |
| 0 | CYCCNTENA | Enable the CYCCNT counter. If not enabled, the counter does not count and no event is generated for PS sampling or CYCCNTENA. In normal use, the debugger must initialize the CYCCNT counter to 0. |

1.3.1495 DWT_CYCLE_COUNT

DWT Current PC Sampler Cycle Count Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_CYCLE_COUNT: 0xE0001004

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CYCCNT | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CYCCNT | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CYCCNT | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CYCCNT | | | | | | | |

Use the DWT Current PC Sampler Cycle Count Register to count the number of core cycles. This count can measure elapsed execution time.

| Bits | Name | Description |
|------|--------------|--|
| 31:0 | CYCCNT[31:0] | Current PC Sampler Cycle Counter count value. When enabled, this counter counts the number of core cycles, except when the core is halted. CYCCNT is a free running counter, counting upwards. It wraps around to 0 on overflow. The debugger must initialize this to 0 when first enabling. |

1.3.1496 DWT_CPI_COUNT

DWT CPI Count Register

Reset: N/A

Register : Address

DWT_CPI_COUNT: 0xE0001008

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CPICNT | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the DWT CPI Count Register to count the total number of instruction cycles beyond the first cycle.

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | CPICNT[7:0] | Current CPI counter value. Increments on the additional cycles (the first cycle is not counted) required to execute all instructions except those recorded by DWT_LSUCNT. This counter also increments on all instruction fetch stalls. If CPIEVTENA is set, an event is emitted when the counter overflows. Clears to 0 on enabling. |

1.3.1497 DWT_EXC_OVHD_COUNT

DWT Exception Overhead Count Register

Reset: N/A

Register : Address

DWT_EXC_OVHD_COUNT: 0xE000100C

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | EXCCNT | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the DWT Exception Overhead Count Register to count the total cycles spent in interrupt processing.

| Bits | Name | Description |
|------|-------------|---|
| 7:0 | EXCCNT[7:0] | Current interrupt overhead counter value. Counts the total cycles spent in interrupt processing (for example entry stacking, return unstacking, pre-emption). An event is emitted on counter overflow (every 256 cycles). This counter initializes to 0 when enabled. Clears to 0 on enabling. |

1.3.1498 DWT_SLEEP_COUNT

DWT Sleep Count Register

Reset: N/A

Register : Address

DWT_SLEEP_COUNT: 0xE0001010

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | SLEPCNT | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the DWT Sleep Count Register to count the total number of cycles during which the processor is sleeping.

| Bits | Name | Description |
|------|--------------|--|
| 7:0 | SLEPCNT[7:0] | Sleep counter. Counts the number of cycles during which the processor is sleeping. An event is emitted on counter overflow (every 256 cycles). This counter initializes to 0 when enabled. |

1.3.1499 DWT_LSU_COUNT

DWT LSU Count Register

Reset: N/A

Register : Address

DWT_LSU_COUNT: 0xE0001014

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | LSUCNT | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the DWT LSU Count Register to count the total number of cycles during which the processor is processing an LSU operation beyond the first cycle.

| Bits | Name | Description |
|------|-------------|--|
| 7:0 | LSUCNT[7:0] | <p>LSU counter. This counts the total number of cycles that the processor is processing an LSU operation. The initial execution cost of the instruction is not counted.</p> <p>For example, an LDR that takes two cycles to complete increments this counter one cycle. Equivalently, an LDR that stalls for two cycles (and so takes four cycles), increments this counter three times. An event is emitted on counter overflow (every 256 cycles).</p> <p>Clears to 0 on enabling.</p> |

1.3.1500 DWT_FOLD_COUNT

DWT Fold Count Register

Reset: N/A

Register : Address

DWT_FOLD_COUNT: 0xE0001018

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | FOLDCNT | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the DWT Fold Count Register to count the total number of folded instructions. This counts 1 for each instruction that takes 0 cycles.

| Bits | Name | Description |
|------|--------------|---|
| 7:0 | FOLDCNT[7:0] | This counts the total number folded instructions. This counter initializes to 0 when enabled. |

1.3.1501 DWT_PC_SAMPLE

DWT Program Counter Sample Register

Reset: N/A

Register : Address

DWT_PC_SAMPLE: 0xE000101C

| | | | | | | | | |
|-----------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | EIASAMPLE | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | EIASAMPLE | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | EIASAMPLE | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | EIASAMPLE | | | | | | | |

Use the DWT Program Counter Sample Register (PCSR) to enable coarse-grained software profiling using a debug agent, without changing the currently executing code. If the core is not in debug state, the value returned is the instruction address of a recently executed instruction. If the core is in debug state, the value returned is 0xFFFFFFFF.

| Bits | Name | Description |
|------|-----------------|--|
| 31:0 | EIASAMPLE[31:0] | Execution instruction address sample, or 0xFFFFFFFF if the core is halted. |

1.3.1502 DWT_COMP_0

DWT Comparator Registers

Reset: N/A

Register : Address

DWT_COMP_0: 0xE0001020

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

Use the DWT Comparator Registers 0-3 to write the values that trigger watchpoint events.

| Bits | Name | Description |
|------|------------|---|
| 31:0 | COMP[31:0] | Data value to compare against PC and the data address as given by DWT_FUNCTIONx. DWT_COMP0 can also compare against the value of the PC Sampler Counter (DWT_CYCCNT). DWT_COMP1 can also compare against data values so that data matching can be performed (DATAVMATCH). |

1.3.1503 DWT_MASK_0

DWT Mask Registers

Reset: N/A

Register : Address

DWT_MASK_0: 0xE0001024

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:UUUU | | | |
| HW Access | NA | | | | R/W | | | |
| Name | | | | | MASK | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the DWT Mask Registers 0-3 to apply a mask to data addresses when matching against COMP.

| Bits | Name | Description |
|------|-----------|---|
| 3:0 | MASK[3:0] | Mask on data address when matching against COMP. This is the size of the ignore mask. So, ~0< However, the actual comparison is slightly more complex to enable matching an address wherever it appears on a bus. So, if COMP is 3, this matches a word access of 0, because 3 would be within the word. |

1.3.1504 DWT_FUNCTION_0

DWT Function registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_FUNCTION_0: 0xE0001028

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|------|------------|------|----------|---|---|---|
| SW Access:Reset | R/W:0 | NA:0 | R/W:0 | NA:0 | R/W:0000 | | | |
| HW Access | R/W | NA | R/W | NA | R/W | | | |
| Name | CYC-MATCH | | EMI-TRANGE | | FUNCTION | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-----------|----|----|----|----|----|---------|------|
| SW Access:Reset | NA:000000 | | | | | | R:0 | NA:0 |
| HW Access | NA | | | | | | R/W | NA |
| Name | | | | | | | LNK1ENA | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|---------|
| SW Access:Reset | NA:00000000 | | | | | | | RC:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | MATCHED |

Use the DWT Function Registers 0-3 to control the operation of the comparator. Each comparator can: Match against either the PC or the data address. This is controlled by CYCMATCH. This function is only available for comparator 0 (DWT_COMP0). Perform data value comparisons if associated address comparators have performed an address match. This function is only available for comparator 1 (DWT_COMP1). Emit data or PC couples, trigger the ETM, or generate a watchpoint depending on the operation defined by FUNCTION.

| Bits | Name | Description |
|------|-----------|---|
| 24 | MATCHED | This bit is set when the comparator matches, and indicates that the operation defined by FUNCTION has occurred since this bit was last read. This bit is cleared on read. |
| 9 | LNK1ENA | Read-only: 0 = DATAVADDR1 not supported 1 = DATAVADDR1 supported (enabled). |
| 7 | CYCMATCH | Only available in comparator 0. When set, this comparator compares against the clock cycle counter. |
| 5 | EMITRANGE | Emit range field. Reserved to permit emitting offset when range match occurs. Reset clears the EMITRANGE bit. PC sampling is not supported when EMITRANGE is enabled. EMITRANGE only applies for: FUNCTION = b0001, b0010, and b0011. |



0xe0001028

1.3.1504 DWT_FUNCTION_0 (continued)

3:0 FUNCTION[3:0] Function settings of the DWT Function Registers.

1.3.1505 DWT_COMP_1

DWT Comparator Registers

Reset: N/A

Register : Address

DWT_COMP_1: 0xE0001030

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

Use the DWT Comparator Registers 0-3 to write the values that trigger watchpoint events.

| Bits | Name | Description |
|------|------------|---|
| 31:0 | COMP[31:0] | Data value to compare against PC and the data address as given by DWT_FUNCTIONx. DWT_COMP0 can also compare against the value of the PC Sampler Counter (DWT_CYCCNT). DWT_COMP1 can also compare against data values so that data matching can be performed (DATAVMATCH). |

1.3.1506 DWT_MASK_1

DWT Mask Registers

Reset: N/A

Register : Address

DWT_MASK_1: 0xE0001034

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:UUUU | | | |
| HW Access | NA | | | | R/W | | | |
| Name | | | | | MASK | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the DWT Mask Registers 0-3 to apply a mask to data addresses when matching against COMP.

| Bits | Name | Description |
|------|-----------|---|
| 3:0 | MASK[3:0] | Mask on data address when matching against COMP. This is the size of the ignore mask. So, ~0< However, the actual comparison is slightly more complex to enable matching an address wherever it appears on a bus. So, if COMP is 3, this matches a word access of 0, because 3 would be within the word. |

1.3.1507 DWT_FUNCTION_1

DWT Function registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_FUNCTION_1: 0xE0001038

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|------|----------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | NA:0 | R/W:0000 | | | |
| HW Access | NA | | R/W | NA | R/W | | | |
| Name | | | EMI-TRANGE | | FUNCTION | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|------------|----|-----------|----|---------|-------------|
| SW Access:Reset | NA:00 | | R/W:00 | | R/W:00 | | R:1 | R/W:0 |
| HW Access | NA | | R/W | | R/W | | R/W | R/W |
| Name | | | DATAVADDR0 | | DATAVSIZE | | LNK1ENA | DATAV-MATCH |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-----------|----|----|----|----|----|------------|----|
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R/W | |
| Name | | | | | | | DATAVADDR1 | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|---------|
| SW Access:Reset | NA:0000000 | | | | | | | RC:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | MATCHED |

Use the DWT Function Registers 0-3 to control the operation of the comparator. Each comparator can: Match against either the PC or the data address. This is controlled by CYCMATCH. This function is only available for comparator 0 (DWT_COMP0). Perform data value comparisons if associated address comparators have performed an address match. This function is only available for comparator 1 (DWT_COMP1). Emit data or PC couples, trigger the ETM, or generate a watchpoint depending on the operation defined by FUNCTION.

| Bits | Name | Description |
|-------|-----------------|---|
| 24 | MATCHED | This bit is set when the comparator matches, and indicates that the operation defined by FUNCTION has occurred since this bit was last read. This bit is cleared on read. |
| 17:16 | DATAVADDR1[1:0] | Identity of a second linked address comparator for data value matching when DATAVMATCH == 1 and LNK1ENA == 1. |
| 13:12 | DATAVADDR0[1:0] | Identity of a linked address comparator for data value matching when DATAVMATCH == 1. |
| 11:10 | DATAVSIZE[1:0] | Defines the size of the data in the COMP register that is to be matched: 00 = byte 01 = halfword 10 = word 11 = Unpredictable. |

1.3.1507 DWT_FUNCTION_1 (continued)

| | | |
|-----|---------------|--|
| 9 | LNK1ENA | Read-only: 0 = DATAVADDR1 not supported 1 = DATAVADDR1 supported (enabled). |
| 8 | DATAVMATCH | This bit is only available in comparator 1. When DATAVMATCH is set, this comparator performs data value compares. The comparators given by DATAVADDR0 and DATAVADDR1 provide the address for the data comparison. If DATAVMATCH is set in DWT_FUNCTION1, the FUNCTION setting for the comparators given by DATAVADDR0 and DATAVADDR1 are overridden and those comparators only provide the address match for the data comparison. |
| 5 | EMITRANGE | Emit range field. Reserved to permit emitting offset when range match occurs. Reset clears the EMITRANGE bit. PC sampling is not supported when EMITRANGE is enabled. EMITRANGE only applies for: FUNCTION = b0001, b0010, and b0011. |
| 3:0 | FUNCTION[3:0] | Function settings of the DWT Function Registers. |

1.3.1508 DWT_COMP_2

DWT Comparator Registers

Reset: N/A

Register : Address

DWT_COMP_2: 0xE0001040

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

Use the DWT Comparator Registers 0-3 to write the values that trigger watchpoint events.

| Bits | Name | Description |
|------|------------|---|
| 31:0 | COMP[31:0] | Data value to compare against PC and the data address as given by DWT_FUNCTIONx. DWT_COMP0 can also compare against the value of the PC Sampler Counter (DWT_CYCCNT). DWT_COMP1 can also compare against data values so that data matching can be performed (DATAVMATCH). |

1.3.1509 DWT_MASK_2

DWT Mask Registers

Reset: N/A

Register : Address

DWT_MASK_2: 0xE0001044

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:UUUU | | | |
| HW Access | NA | | | | R/W | | | |
| Name | | | | | MASK | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the DWT Mask Registers 0-3 to apply a mask to data addresses when matching against COMP.

| Bits | Name | Description |
|------|-----------|---|
| 3:0 | MASK[3:0] | Mask on data address when matching against COMP. This is the size of the ignore mask. So, ~0< However, the actual comparison is slightly more complex to enable matching an address wherever it appears on a bus. So, if COMP is 3, this matches a word access of 0, because 3 would be within the word. |

1.3.1510 DWT_FUNCTION_2

DWT Function registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_FUNCTION_2: 0xE0001048

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|------------|------|----------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | NA:0 | R/W:0000 | | | |
| HW Access | NA | | R/W | NA | R/W | | | |
| Name | | | EMI-TRANGE | | FUNCTION | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-----------|----|----|----|----|----|---------|------|
| SW Access:Reset | NA:000000 | | | | | | R:0 | NA:0 |
| HW Access | NA | | | | | | R/W | NA |
| Name | | | | | | | LNK1ENA | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|---------|
| SW Access:Reset | NA:00000000 | | | | | | | RC:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | MATCHED |

Use the DWT Function Registers 0-3 to control the operation of the comparator. Each comparator can: Match against either the PC or the data address. This is controlled by CYCMATCH. This function is only available for comparator 0 (DWT_COMP0). Perform data value comparisons if associated address comparators have performed an address match. This function is only available for comparator 1 (DWT_COMP1). Emit data or PC couples, trigger the ETM, or generate a watchpoint depending on the operation defined by FUNCTION.

| Bits | Name | Description |
|------|---------------|---|
| 24 | MATCHED | This bit is set when the comparator matches, and indicates that the operation defined by FUNCTION has occurred since this bit was last read. This bit is cleared on read. |
| 9 | LNK1ENA | Read-only: 0 = DATAVADDR1 not supported 1 = DATAVADDR1 supported (enabled). |
| 5 | EMITRANGE | Emit range field. Reserved to permit emitting offset when range match occurs. Reset clears the EMITRANGE bit. PC sampling is not supported when EMITRANGE is enabled. EMITRANGE only applies for: FUNCTION = b0001, b0010, and b0011. |
| 3:0 | FUNCTION[3:0] | Function settings of the DWT Function Registers. |

1.3.1511 DWT_COMP_3

DWT Comparator Registers

Reset: N/A

Register : Address

DWT_COMP_3: 0xE0001050

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

Use the DWT Comparator Registers 0-3 to write the values that trigger watchpoint events.

| Bits | Name | Description |
|------|------------|---|
| 31:0 | COMP[31:0] | Data value to compare against PC and the data address as given by DWT_FUNCTIONx. DWT_COMP0 can also compare against the value of the PC Sampler Counter (DWT_CYCCNT). DWT_COMP1 can also compare against data values so that data matching can be performed (DATAVMATCH). |

1.3.1512 DWT_MASK_3

DWT Mask Registers

Reset: N/A

Register : Address

DWT_MASK_3: 0xE0001054

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:UUUU | | | |
| HW Access | NA | | | | R/W | | | |
| Name | | | | | MASK | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the DWT Mask Registers 0-3 to apply a mask to data addresses when matching against COMP.

| Bits | Name | Description |
|------|-----------|---|
| 3:0 | MASK[3:0] | Mask on data address when matching against COMP. This is the size of the ignore mask. So, ~0< However, the actual comparison is slightly more complex to enable matching an address wherever it appears on a bus. So, if COMP is 3, this matches a word access of 0, because 3 would be within the word. |

1.3.1513 DWT_FUNCTION_3

DWT Function registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_FUNCTION_3: 0xE0001058

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|---|----------------|------|----------|---|---|---|
| SW Access:Reset | NA:00 | | R/W:0 | NA:0 | R/W:0000 | | | |
| HW Access | NA | | R/W | NA | R/W | | | |
| Name | | | EMI- TRANGE | | FUNCTION | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-----------|----|----|----|----|----|---------|------|
| SW Access:Reset | NA:000000 | | | | | | R:0 | NA:0 |
| HW Access | NA | | | | | | R/W | NA |
| Name | | | | | | | LNK1ENA | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|---------|
| SW Access:Reset | NA:00000000 | | | | | | | RC:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | MATCHED |

Use the DWT Function Registers 0-3 to control the operation of the comparator. Each comparator can: Match against either the PC or the data address. This is controlled by CYCMATCH. This function is only available for comparator 0 (DWT_COMP0). Perform data value comparisons if associated address comparators have performed an address match. This function is only available for comparator 1 (DWT_COMP1). Emit data or PC couples, trigger the ETM, or generate a watchpoint depending on the operation defined by FUNCTION.

| Bits | Name | Description |
|------|---------------|---|
| 24 | MATCHED | This bit is set when the comparator matches, and indicates that the operation defined by FUNCTION has occurred since this bit was last read. This bit is cleared on read. |
| 9 | LNK1ENA | Read-only: 0 = DATAVADDR1 not supported 1 = DATAVADDR1 supported (enabled). |
| 5 | EMITRANGE | Emit range field. Reserved to permit emitting offset when range match occurs. Reset clears the EMITRANGE bit. PC sampling is not supported when EMITRANGE is enabled. EMITRANGE only applies for: FUNCTION = b0001, b0010, and b0011. |
| 3:0 | FUNCTION[3:0] | Function settings of the DWT Function Registers. |

1.3.1514 FPB_CTRL

Flash Patch Control Register

Reset: Reset Signals Listed Below

Register : Address

FPB_CTRL: 0xE0002000

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:0110 | | | | NA:00 | | W:U | R/W:0 |
| HW Access | R | | | | NA | | R | R/W |
| Name | NUM_CODE1 | | | | | | KEY | ENABLE |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:0 | R:000 | | | R:0010 | | | |
| HW Access | NA | R | | | R | | | |
| Name | | NUM_CODE2 | | | NUM_LIT | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the Flash Patch Control Register to enable the flash patch block.

| Bits | Name | Description |
|-------|----------------|--|
| 14:12 | NUM_CODE2[2:0] | Number of full banks of code comparators, sixteen comparators per bank. Where less than sixteen code comparators are provided, the bank count is zero, and the number present indicated by NUM_CODE. This read only field contains 3'b000 to indicate 0 banks for Cortex-M3 processor. |
| 11:8 | NUM_LIT[3:0] | Number of literal slots field. This read only field contains b0010 to indicate that there are two literal slots. |
| 7:4 | NUM_CODE1[3:0] | Number of code slots field. This read only field contains b0110 to indicate that there are six code slots. |
| 1 | KEY | Key field. To write to the Flash Patch Control Register, you must write a 1 to this write-only bit. |
| 0 | ENABLE | Flash patch unit enable bit: 1 = flash patch unit enabled 0 = flash patch unit disabled. Reset clears the ENABLE bit. Note: If the TIEOFF_FPEN define is uncommented in CM3Defs.v during implementation, it is not possible to set ENABLE. |

1.3.1514 FPB_CTRL (continued)

Reset Table

| resetsignal | field(s) |
|--|---|
| N/A | KEY |
| System reset for retention flops [reset_all_retention] | ENABLE, NUM_CODE1[3:0], NUM_LIT[3:0], NUM_CODE2[2:0] |

1.3.1515 FPB_REMAP

Flash Patch Remap Register

Reset: N/A

Register : Address

FPB_REMAP: 0xE0002004

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R/W | | | NA | | | | |
| Name | REMAP | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | REMAP | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | REMAP | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------|----|----|-----------|----|----|----|----|
| SW Access:Reset | NA:000 | | | R/W:UUUUU | | | | |
| HW Access | NA | | | R/W | | | | |
| Name | | | | REMAP | | | | |

Use the Flash Patch Remap Register to provide the location in System space where a matched address is remapped. The REMAP address is 8-word aligned, with one word allocated to each of the eight FPB comparators.

| Bits | Name | Description |
|------|-------------|---------------------------|
| 28:5 | REMAP[23:0] | Remap base address field. |

0xe0002008

1.3.1516 FPB_FP_COMP_0

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_0: 0xE0002008

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|------|--------|
| SW Access:Reset | R/W:UUUUUU | | | | | | NA:0 | R/W:0 |
| HW Access | R/W | | | | | | NA | R/W |
| Name | COMP | | | | | | | ENABLE |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|------|------------|----|----|----|----|
| SW Access:Reset | R/W:UU | | NA:0 | R/W:UUUUUU | | | | |
| HW Access | R/W | | NA | R/W | | | | |
| Name | REPLACE | | | COMP | | | | |

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

| Bits | Name | Description |
|-------|--------------|---|
| 31:30 | REPLACE[1:0] | This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting. |
| 28:2 | COMP[26:0] | Comparison address. |
| 0 | ENABLE | Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit. |

1.3.1516 FPB_FP_COMP_0 (continued)

Reset Table

| resetsignal | field(s) |
|---|---------------------------|
| N/A | COMP[26:0], RE-PLACE[1:0] |
| System reset for retention flops [reset_all_retention] | ENABLE |

0xe000200c

1.3.1517 FPB_FP_COMP_1

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_1: 0xE000200C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|------|--------|
| SW Access:Reset | R/W:UUUUUU | | | | | | NA:0 | R/W:0 |
| HW Access | R/W | | | | | | NA | R/W |
| Name | COMP | | | | | | | ENABLE |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|------|------------|----|----|----|----|
| SW Access:Reset | R/W:UU | | NA:0 | R/W:UUUUUU | | | | |
| HW Access | R/W | | NA | R/W | | | | |
| Name | REPLACE | | | COMP | | | | |

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

| Bits | Name | Description |
|-------|--------------|---|
| 31:30 | REPLACE[1:0] | This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting. |
| 28:2 | COMP[26:0] | Comparison address. |
| 0 | ENABLE | Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit. |

1.3.1517 FPB_FP_COMP_1 (continued)

Reset Table

| resetsignal | field(s) |
|--|-------------------------------|
| N/A | COMP[26:0], RE- PLACE[1:0] |
| System reset for retention flops [reset_all_retention] | ENABLE |

0xe0002010

1.3.1518 FPB_FP_COMP_2

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_2: 0xE0002010

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|------|--------|
| SW Access:Reset | R/W:UUUUUU | | | | | | NA:0 | R/W:0 |
| HW Access | R/W | | | | | | NA | R/W |
| Name | COMP | | | | | | | ENABLE |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|------|------------|----|----|----|----|
| SW Access:Reset | R/W:UU | | NA:0 | R/W:UUUUUU | | | | |
| HW Access | R/W | | NA | R/W | | | | |
| Name | REPLACE | | | COMP | | | | |

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

| Bits | Name | Description |
|-------|--------------|---|
| 31:30 | REPLACE[1:0] | This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting. |
| 28:2 | COMP[26:0] | Comparison address. |
| 0 | ENABLE | Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit. |

1.3.1518 FPB_FP_COMP_2 (continued)

Reset Table

| resetsignal | field(s) |
|--|-------------------------------|
| N/A | COMP[26:0], RE- PLACE[1:0] |
| System reset for reten- tion flops [reset_all_retention] | ENABLE |

0xe0002014

1.3.1519 FPB_FP_COMP_3

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_3: 0xE0002014

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|------|--------|
| SW Access:Reset | R/W:UUUUUU | | | | | | NA:0 | R/W:0 |
| HW Access | R/W | | | | | | NA | R/W |
| Name | COMP | | | | | | | ENABLE |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|------|------------|----|----|----|----|
| SW Access:Reset | R/W:UU | | NA:0 | R/W:UUUUUU | | | | |
| HW Access | R/W | | NA | R/W | | | | |
| Name | REPLACE | | | COMP | | | | |

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

| Bits | Name | Description |
|-------|--------------|---|
| 31:30 | REPLACE[1:0] | This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting. |
| 28:2 | COMP[26:0] | Comparison address. |
| 0 | ENABLE | Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit. |

1.3.1519 FPB_FP_COMP_3 (continued)

Reset Table

| resetsignal | field(s) |
|--|---------------------------|
| N/A | COMP[26:0], RE-PLACE[1:0] |
| System reset for retention flops [reset_all_retention] | ENABLE |

0xe0002018

1.3.1520 FPB_FP_COMP_4

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_4: 0xE0002018

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|------|--------|
| SW Access:Reset | R/W:UUUUUU | | | | | | NA:0 | R/W:0 |
| HW Access | R/W | | | | | | NA | R/W |
| Name | COMP | | | | | | | ENABLE |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|------|------------|----|----|----|----|
| SW Access:Reset | R/W:UU | | NA:0 | R/W:UUUUUU | | | | |
| HW Access | R/W | | NA | R/W | | | | |
| Name | REPLACE | | | COMP | | | | |

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

| Bits | Name | Description |
|-------|--------------|---|
| 31:30 | REPLACE[1:0] | This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting. |
| 28:2 | COMP[26:0] | Comparison address. |
| 0 | ENABLE | Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit. |

1.3.1520 FPB_FP_COMP_4 (continued)

Reset Table

| resetsignal | field(s) |
|--|---------------------------|
| N/A | COMP[26:0], RE-PLACE[1:0] |
| System reset for retention flops [reset_all_retention] | ENABLE |

1.3.1521 FPB_FP_COMP_5

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_5: 0xE000201C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|------|--------|
| SW Access:Reset | R/W:UUUUUU | | | | | | NA:0 | R/W:0 |
| HW Access | R/W | | | | | | NA | R/W |
| Name | COMP | | | | | | | ENABLE |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|------|------------|----|----|----|----|
| SW Access:Reset | R/W:UU | | NA:0 | R/W:UUUUUU | | | | |
| HW Access | R/W | | NA | R/W | | | | |
| Name | REPLACE | | | COMP | | | | |

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

| Bits | Name | Description |
|-------|--------------|---|
| 31:30 | REPLACE[1:0] | This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting. |
| 28:2 | COMP[26:0] | Comparison address. |
| 0 | ENABLE | Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit. |

1.3.1521 FPB_FP_COMP_5 (continued)

Reset Table

| resetsignal | field(s) |
|--|-------------------------------|
| N/A | COMP[26:0], RE- PLACE[1:0] |
| System reset for retention flops [reset_all_retention] | ENABLE |

0xe0002020

1.3.1522 FPB_FP_COMP_6

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_6: 0xE0002020

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|------|--------|
| SW Access:Reset | R/W:UUUUUU | | | | | | NA:0 | R/W:0 |
| HW Access | R/W | | | | | | NA | R/W |
| Name | COMP | | | | | | | ENABLE |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|------|------------|----|----|----|----|
| SW Access:Reset | R/W:UU | | NA:0 | R/W:UUUUUU | | | | |
| HW Access | R/W | | NA | R/W | | | | |
| Name | REPLACE | | | COMP | | | | |

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

| Bits | Name | Description |
|-------|--------------|---|
| 31:30 | REPLACE[1:0] | This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting. |
| 28:2 | COMP[26:0] | Comparison address. |
| 0 | ENABLE | Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit. |

1.3.1522 FPB_FP_COMP_6 (continued)

Reset Table

| resetsignal | field(s) |
|---|-------------------------------|
| N/A | COMP[26:0], RE- PLACE[1:0] |
| System reset for retention flops [reset_all_retention] | ENABLE |

1.3.1523 FPB_FP_COMP_7

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_7: 0xE0002024

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|------|--------|
| SW Access:Reset | R/W:UUUUUU | | | | | | NA:0 | R/W:0 |
| HW Access | R/W | | | | | | NA | R/W |
| Name | COMP | | | | | | | ENABLE |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | COMP | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|------|------------|----|----|----|----|
| SW Access:Reset | R/W:UU | | NA:0 | R/W:UUUUUU | | | | |
| HW Access | R/W | | NA | R/W | | | | |
| Name | REPLACE | | | COMP | | | | |

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

| Bits | Name | Description |
|-------|--------------|---|
| 31:30 | REPLACE[1:0] | This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting. |
| 28:2 | COMP[26:0] | Comparison address. |
| 0 | ENABLE | Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit. |

1.3.1523 FPB_FP_COMP_7 (continued)

Reset Table

| resetsignal | field(s) |
|---|-------------------------------|
| N/A | COMP[26:0], RE- PLACE[1:0] |
| System reset for retention flops [reset_all_retention] | ENABLE |

0xe0002fd0

1.3.1524 FPB_PID4

FPB Peripheral Identification Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID4: 0xE0002FD0

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000100 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID4 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID4[7:0] | Peripheral Identification Register 4 |

1.3.1525 FPB_PID5

FPB Peripheral Identification Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID5: 0xE0002FD4

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID5 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID5[7:0] | Peripheral Identification Register 5 |

0xe0002fd8

1.3.1526 FPB_PID6

FPB Peripheral Identification Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID6: 0xE0002FD8

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID6 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID6[7:0] | Peripheral Identification Register 6 |

1.3.1527 FPB_PID7

FPB Peripheral Identification Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID7: 0xE0002FDC

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID7 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID7[7:0] | Peripheral Identification Register 7 |

0xe0002fe0

1.3.1528 FPB_PID0

FPB Peripheral Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID0: 0xE0002FE0

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000011 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID0[7:0] | Peripheral Identification Register 0 |

1.3.1529 FPB_PID1

FPB Peripheral Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID1: 0xE0002FE4

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:10110000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID1 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID1[7:0] | Peripheral Identification Register 1 |

0xe0002fe8

1.3.1530 FPB_PID2

FPB Peripheral Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID2: 0xE0002FE8

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00101011 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID2 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID2[7:0] | Peripheral Identification Register 2 |

1.3.1531 FPB_PID3

FPB Peripheral Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID3: 0xE0002FEC

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID3 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID3[7:0] | Peripheral Identification Register 3 |

0xe0002ff0

1.3.1532 FPB_CID0

FPB Component Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_CID0: 0xE0002FF0

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00001101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID0[7:0] | Component Identification Register 0 |

1.3.1533 FPB_CID1

FPB Component Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_CID1: 0xE0002FF4

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:11100000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID1 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID1[7:0] | Component Identification Register 1 |

0xe0002ff8

1.3.1534 FPB_CID2

FPB Component Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_CID2: 0xE0002FF8

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID2 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID2[7:0] | Component Identification Register 2 |

1.3.1535 FPB_CID3

FPB Component Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_CID3: 0xE0002FFC

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:10110001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID3 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register mirrors the PID/CID contents of the ROM memory table

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID3[7:0] | Component Identification Register 3 |

1.3.1536 NVIC_INT_CTL_TYPE

Interrupt Controller Type Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_INT_CTL_TYPE: 0xE000E004

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-------------|---|---|---|---|
| SW Access:Reset | NA:000 | | | R:00000 | | | | |
| HW Access | NA | | | W | | | | |
| Name | | | | INTLINESNUM | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Read the Interrupt Controller Type Register to see the number of interrupt lines that the NVIC supports.

| Bits | Name | Description |
|------|------------------|--|
| 4:0 | INTLINESNUM[4:0] | Total number of interrupt lines in groups of 32: b00000 = 0...32 b00001 = 33...64 b00010 = 65...96 b00011 = 97...128 b00100 = 129...160 b00101 = 161...192 b00110 = 193...224 b00111 = 225...256 |

1.3.1537 NVIC_SYSTICK_CTL

SYSTICK Control and Status register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYSTICK_CTL: 0xE000E010

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|--------|---------|-------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | CLKSRC | TICKINT | ENB |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|---------|
| SW Access:Reset | NA:0000000 | | | | | | | RC:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | CNTFLAG |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

SYSTICK Ten milliSecond software timer control and status register.

| Bits | Name | Description |
|------|---------|---|
| 16 | CNTFLAG | CNTFLAG is set when the CURRENT value of the SYSTICK timer is zero. It is automatically cleared when read. Note that CNTFLAG is cleared when the debugger reads it only if the MasterType bit in the AHB-AP Control Register is set to 0. Otherwise the CNTFLAG is not changed by a debugger read. |
| 2 | CLKSRC | 0=External Clock Source 1=CPU Clock Note that the External Clock Source must be at least 2.5 times slower than the CPU Clock or operation will be unpredictable. If no external clock source is provided, the input is held at 1 and the SYSTICK timer will count as the same as if the CPU Clock was used. |
| 1 | TICKINT | 0=Disable the Systick Interrupt handler 1=Enable the Systick Interrupt Handler. When the CNTFLAG is set an interrupt will be generated if the TICKINT bit is enabled (1). |
| 0 | ENB | 0=Disable the timer 1=Enable the SYSTICK Timer When the SYSTICK timer is enabled, the counter runs until it reaches 0. When it reaches 0, it will set the COUNTFLAG and load the RELOAD value into the counter and continue counting. |

0xe000e014

1.3.1538 NVIC_SYSTICK_RELOAD

SYSTICK Reload value

Reset: N/A

Register : Address

NVIC_SYSTICK_RELOAD: 0xE000E014

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RELOAD | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RELOAD | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R | | | | | | | |
| Name | RELOAD | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

RELOAD is copied into the CURRENT register when it counts down to 0. RELOAD is the number of clocks between each setting of the CNTFLAG in the SYSTICK_CTL register. Note that a value of 0 will not cause an interrupt or CNTFLAG to be set.

| Bits | Name | Description |
|------|--------------|---|
| 23:0 | RELOAD[23:0] | Value loaded into the SYSTICK CURRENT value register when it counts down 0. |

1.3.1539 NVIC_SYSTICK_CURRENT

SYSTICK Counter

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYSTICK_CURRENT: 0xE000E018

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CURRENT | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CURRENT | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CURRENT | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Current value of the SYSTICK Counter. Note that writing any value to this register will clear it to zero. Clearing to zero will set CNTFLAG and reload the counter with the RELOAD value.

| Bits | Name | Description |
|------|---------------|---------------------------------------|
| 23:0 | CURRENT[23:0] | Current value of the SYSTICK Counter. |

1.3.1540 NVIC_SYSTICK_CAL

SYSTICK Calibration register

Reset: N/A

Register : Address

NVIC_SYSTICK_CAL: 0xE000E01C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|------|-----------|----|----|----|----|----|
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | TENMS | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | TENMS | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | TENMS | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R:U | R:U | NA:000000 | | | | | |
| HW Access | R/W | R/W | NA | | | | | |
| Name | NOREF | SKEW | | | | | | |

Used to adjust the SYSTICK timer to be exactly 10ms. See Chapter 14 of The Definitive Guide to the ARM Cortex-M3.

| Bits | Name | Description |
|------|-------------|---|
| 31 | NOREF | NOREF is set to 1 when there is no reference clock. |
| 30 | SKEW | When SKEW is set to 1, the calibration value is not exactly 10 milliseconds due to the clock frequency. The accuracy of the timer may not be suitable for Real-Time applications. |
| 23:0 | TENMS[23:0] | Calibration value for the Ten Millisecond timer. |

1.3.1541 NVIC_SETENA0

Interrupt Enable Set 0-31

Reset: N/A

Register : Address

NVIC_SETENA0: 0xE000E100

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | SETENA0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----|----|----|----|----|---|---|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | SETENA0 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | SETENA0 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | SETENA0 | | | | | | | |

Set Enable external interrupts 0-31. Writing a 1 to any bit in this register sets the interrupt enable for the respective interrupt. Writing a 0 does nothing. To clear the bit, write a 1 to the Interrupt Clear enable register. Reading this register will read the current status of the interrupt enable. Setting and clearing the interrupt enables is done in 2 different registers to make it easier to set/clear individual bits. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 31:0 | SETENA0[31:0] | Writing a 1 enables the respective interrupt. IE: bit 0 will enable IRQ0, Bit 1 will enable IRQ1 ... Bit 31 will enable IRQ31. Writing 0 has no effect. |

1.3.1542 NVIC_CLRENA0

Interrupt Enable Clear 0-31

Reset: N/A

Register : Address

NVIC_CLRENA0: 0xE000E180

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CLRENA0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CLRENA0 | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CLRENA0 | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CLRENA0 | | | | | | | |

Clear Enable external interrupts 0-31. Writing a 1 to any bit in this register clears the interrupt enable for the respective interrupt. Writing a 0 does nothing. Reading this register will read the current status of the interrupt enable. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 31:0 | CLRENA0[31:0] | Writing a 1 disables the respective interrupt. IE: bit 0 will disable IRQ0, Bit 1 will disable IRQ1 ... Bit 31 will disable IRQ31. Writing 0 has no effect. |

1.3.1543 NVIC_SETPEND0

Interrupt Pending Set 0-31

Reset: N/A

Register : Address

NVIC_SETPEND0: 0xE000E200

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | SETPEND0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | SETPEND0 | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | SETPEND0 | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | SETPEND0 | | | | | | | |

Set Pending external interrupts 0-31. Writing a 1 to any bit in this register sets the interrupt pending bit for the respective interrupt. Writing a 0 does nothing. Reading this register will read the current status of the interrupt pending bits. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|----------------|---|
| 31:0 | SETPEND0[31:0] | Writing a 1 sets the respective interrupt pending bit. IE: bit 0 will set IRQ0, Bit 1 will set IRQ1 ... Bit 31 will set IRQ31. Writing 0 has no effect. |

1.3.1544 NVIC_CLRPEND0

Interrupt Pending Clear 0-31

Reset: N/A

Register : Address

NVIC_CLRPEND0: 0xE000E280

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CLRPEND0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CLRPEND0 | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CLRPEND0 | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CLRPEND0 | | | | | | | |

Clear Pending external interrupts 0-31. Writing a 1 to any bit in this register clears the interrupt pending bit for the respective interrupt. Writing a 0 does nothing. Reading this register will read the current status of the interrupt pending bits. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|----------------|---|
| 31:0 | CLRPEND0[31:0] | Writing a 1 clears the respective interrupt pending bit. IE: bit 0 will clear IRQ0, Bit 1 will clear IRQ1 ... Bit 31 will clear IRQ31. Writing 0 has no effect. |

1.3.1545 NVIC_ACTIVE0

Active Interrupts 0-31

Reset: N/A

Register : Address

NVIC_ACTIVE0: 0xE000E300

| | | | | | | | | |
|-----------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ACTIVE0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ACTIVE0 | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ACTIVE0 | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ACTIVE0 | | | | | | | |

Each bit of this register corresponds to an interrupt 0-31. If the bit is a 1, then that interrupt is active. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|----------------------------|
| 31:0 | ACTIVE0[31:0] | Active interrupt register. |

1.3.1546 NVIC_PRI_0

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_0: 0xE000E400

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1547 NVIC_PRI_1

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_1: 0xE000E401

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1548 NVIC_PRI_2

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_2: 0xE000E402

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1549 NVIC_PRI_3

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_3: 0xE000E403

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1550 NVIC_PRI_4

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_4: 0xE000E404

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1551 NVIC_PRI_5

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_5: 0xE000E405

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1552 NVIC_PRI_6

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_6: 0xE000E406

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1553 NVIC_PRI_7

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_7: 0xE000E407

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1554 NVIC_PRI_8

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_8: 0xE000E408

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1555 NVIC_PRI_9

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_9: 0xE000E409

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1556 NVIC_PRI_10

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_10: 0xE000E40A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1557 NVIC_PRI_11

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_11: 0xE000E40B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1558 NVIC_PRI_12

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_12: 0xE000E40C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1559 NVIC_PRI_13

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_13: 0xE000E40D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1560 NVIC_PRI_14

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_14: 0xE000E40E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1561 NVIC_PRI_15

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_15: 0xE000E40F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1562 NVIC_PRI_16

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_16: 0xE000E410

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1563 NVIC_PRI_17

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_17: 0xE000E411

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1564 NVIC_PRI_18

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_18: 0xE000E412

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1565 NVIC_PRI_19

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_19: 0xE000E413

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1566 NVIC_PRI_20

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_20: 0xE000E414

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1567 NVIC_PRI_21

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_21: 0xE000E415

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1568 NVIC_PRI_22

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_22: 0xE000E416

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1569 NVIC_PRI_23

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_23: 0xE000E417

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1570 NVIC_PRI_24

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_24: 0xE000E418

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1571 NVIC_PRI_25

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_25: 0xE000E419

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1572 NVIC_PRI_26

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_26: 0xE000E41A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1573 NVIC_PRI_27

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_27: 0xE000E41B

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1574 NVIC_PRI_28

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_28: 0xE000E41C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1575 NVIC_PRI_29

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_29: 0xE000E41D

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1576 NVIC_PRI_30

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_30: 0xE000E41E

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1577 NVIC_PRI_31

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_31: 0xE000E41F

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:UUU | | | NA:00000 | | | | |
| HW Access | R | | | NA | | | | |
| Name | PRIORITY | | | | | | | |

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|---------------|---|
| 7:5 | PRIORITY[2:0] | There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte. 0 is the highest priority and 7 is the lowest. |

1.3.1578 NVIC_CPUID_BASE

CPU ID Base Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_CPUID_BASE: 0xE00ED00

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|---|----------|---|---|---|
| SW Access:Reset | R:0011 | | | | R:0001 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PARTNO | | | | REVISION | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:11000010 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PARTNO | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|---------|----|----|----|----------|----|----|----|
| SW Access:Reset | R:0010 | | | | R:1111 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | VARIANT | | | | Constant | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:01000001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | IMPLEMENTER | | | | | | | |

Read the CPU ID Base Register to determine: o the ID number of the processor core o the version number of the processor core o the implementation details of the processor core.

| Bits | Name | Description |
|-------|------------------|---|
| 31:24 | IMPLEMENTER[7:0] | Implementer code. ARM is 0x41 |
| 23:20 | VARIANT[3:0] | Implementation defined variant number. |
| 19:16 | Constant[3:0] | Reads as 0xF |
| 15:4 | PARTNO[11:0] | Number of processor within family: [11:10] b11 = Cortex family [9:8] b00 = version [7:6] b00 = reserved [5:4] b10 = M (v7-M) [3:0] X = family member. Cortex-M3 family is b0011. |
| 3:0 | REVISION[3:0] | Implementation defined revision number. |

1.3.1579 NVIC_INTR_CTRL_STATE

Interrupt Control State Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_INTR_CTRL_STATE: 0xE000ED04

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | VECTACTIVE | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|------------|-------|---|------------|
| SW Access:Reset | R:0000 | | | | R:0 | NA:00 | | R:0 |
| HW Access | R/W | | | | R/W | NA | | R/W |
| Name | VECTPENDING | | | | RETTO-BASE | | | VECTACTIVE |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|-------------|-------------|----|----|----|----|----|
| SW Access:Reset | R:0 | R:0 | R:000000 | | | | | |
| HW Access | R/W | R/W | R/W | | | | | |
| Name | ISRPRE-EMPT | ISRPEND-ING | VECTPENDING | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|-------|----|------------|------------|------------|------------|------|
| SW Access:Reset | R/W:0 | NA:00 | | R/W:0 | W:0 | R/W:0 | W:0 | NA:0 |
| HW Access | R/W | NA | | R/W | R/W | R/W | R/W | NA |
| Name | NMIPEND-SET | | | PENDSV-SET | PENDSV-CLR | PENDST-SET | PENDST-CLR | |

Use the Interrupt Control State Register to:

- o set a pending Non-Maskable Interrupt (NMI)
- o set or clear a pending SVC
- o set or clear a pending SysTick
- o check for pending exceptions
- o check the vector number of the highest priority pended exception
- o check the vector number of the active exception.

| Bits | Name | Description |
|------|------------|--|
| 31 | NMIPENDSET | On writes, makes the NMI exception active. On reads, indicates the state of the exception: 0 = On writes, has no effect. On reads, NMI is inactive. 1 = On writes, make the NMI exception active. On reads, NMI is active. Because NMI is higher priority than other exceptions, if the processor is not already executing the NMI handler, it enters the NMI exception handler as soon as it recognizes the write to this bit. |
| 28 | PENDSVSET | Set pending pendSV bit: 1 = set pending pendSV 0 = do not set pending pendSV. |
| 27 | PENDSVCLR | Clear pending pendSV bit: 1 = clear pending pendSV 0 = do not clear pending pendSV. |

1.3.1579 NVIC_INTR_CTRL_STATE (continued)

| | | |
|-------|------------------|---|
| 26 | PENDSTSET | Set a pending SysTick bit 1 = set pending SysTick 0 = do not set pending SysTick. |
| 25 | PENDSTCLR | Clear pending SysTick bit: 1 = clear pending SysTick 0 = do not clear pending SysTick. |
| 23 | ISRPREEMPT | You must only use this at debug time. It indicates that a pending interrupt becomes active in the next running cycle. If C_MASKINTS is clear in the Debug Halting Control and Status Register, the interrupt is serviced. |
| 22 | ISRPENDING | Interrupt pending flag. Excludes NMI and Faults: 1 = interrupt pending 0 = interrupt not pending. |
| 21:12 | VECTPENDING[9:0] | Pending ISR number field. VECTPENDING contains the interrupt number of the highest priority pending ISR. |
| 11 | RETTOBASE | This bit is 1 when the set of all active exceptions minus the IPSR_current_exception yields the empty set. |
| 8:0 | VECTACTIVE[8:0] | Active ISR number field. VECTACTIVE contains the interrupt number of the currently running ISR, including NMI and Hard Fault. A shared handler can use VECTACTIVE to determine which interrupt invoked it. You can subtract 16 from the VECTACTIVE field to index into the Interrupt Clear/Set Enable, Interrupt Clear Pending/SetPending and Interrupt Priority Registers. INTISR[0] has vector number 16. Reset clears the VECTACTIVE field. |

1.3.1580 NVIC_VECT_OFFSET

Interrupt Vector Table Offset

Reset: N/A

Register : Address

NVIC_VECT_OFFSET: 0xE000ED08

| | | | | | | | | |
|-----------------|--------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:U | NA:0000000 | | | | | | |
| HW Access | R/W | NA | | | | | | |
| Name | TBLOFF | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | TBLOFF | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | TBLOFF | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00 | | R/W:U | R/W:UUUUU | | | | |
| HW Access | NA | | R/W | R/W | | | | |
| Name | | | TBLBASE | TBLOFF | | | | |

Relocates the Interrupt Vector table (IVT) to SRAM. The default Interrupt Vector Table is at 0x0000_0000 (see description in FLASH). This register allows the Vector Table to be relocated so that the interrupt vectors can be changed by the application. Typically the Interrupt Vector Table is relocated to SRAM in Code Space (below 0x2000_0000) for maximum interrupt performance. Note that the IVT can be placed above 0x2000_0000 but you lose the parallelism of stacking registers and fetching the interrupt vector at the same time if the IVT is located above 0x2000_0000. Typically the IVT should be located at the bottom of SRAM in CODE space - 0x1ffn_0000 where n will depend on the amount of SRAM available. See Chapter 7 of The Definitive Guide to the ARM Cortex-M3 for more details.

| Bits | Name | Description |
|------|--------------|--|
| 29 | TBLBASE | Bit 29 of the vector table offset: 0=Table Base in Code. 1=Table Base in RAM. Maximum interrupt performance is achieved when this bit is 0. |
| 28:7 | TBLOFF[21:0] | Offset of the Interrupt Vector Table. Note that this must be on a power-of-2 boundary large enough for the number of interrupt vectors (typically a 1K byte boundary). |

1.3.1581 NVIC_APPLN_INTR

Application Interrupt and Reset Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_APPLN_INTR: 0xE000ED0C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|------------------|--------------------|----------------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R/W | R/W | R/W |
| Name | | | | | | SYSRESE- TREQ | VECTCL- RACTIVE | VECTRE- SET |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|----------------|---------|----|----|----|----------|---|---|
| SW Access:Reset | R/W:0 | NA:0000 | | | | R/W:000 | | |
| HW Access | R/W | NA | | | | R/W | | |
| Name | ENDIAN- ESS | | | | | PRIGROUP | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | VECTKEY | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------------|----|----|----|----|----|----|----|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | VECTKEY | | | | | | | |

Use the Application Interrupt and Reset Control Register to: o determine data endianness o clear all active state information for debug or to recover from a hard failure o execute a system reset o alter the priority grouping position (binary point).

| Bits | Name | Description |
|-------|---------------|---|
| 31:16 | VECTKEY[15:0] | Register key. Writing to this register requires 0x5FA in the VECTKEY field. Otherwise the write value is ignored. |
| 15 | ENDIANESS | Data endianness bit: 1 = big endian 0 = little endian. ENDIANESS is sampled from the BIGEND input port during reset. You cannot change ENDIANESS outside of reset. |

1.3.1581 NVIC_APPLN_INTR (continued)

| | | |
|------|---------------|--|
| 10:8 | PRIGROUP[2:0] | <p>Interrupt priority grouping field:</p> <p>PRIGROUP Split of pre-emption priority from subpriority</p> <p>0 7.1 indicates seven bits of pre-emption priority, one bit of subpriority</p> <p>1 6.2 indicates six bits of pre-emption priority, two bits of subpriority</p> <p>2 5.3 indicates five bits of pre-emption priority, three bits of subpriority</p> <p>3 4.4 indicates four bits of pre-emption priority, four bits of subpriority</p> <p>4 3.5 indicates three bits of pre-emption priority, five bits of subpriority</p> <p>5 2.6 indicates two bits of pre-emption priority, six bits of subpriority</p> <p>6 1.7 indicates one bit of pre-emption priority, seven bits of subpriority</p> <p>7 0.8 indicates no pre-emption priority, eight bits of subpriority.</p> <p>PRIGROUP field is a binary point position indicator for creating subpriorities for exceptions that share the same pre-emption level. It divides the PRI_n field in the Interrupt Priority Register into a pre-emption level and a subpriority level. The binary point is a left-of value. This means that the PRIGROUP value represents a point starting at the left of the Least Significant Bit (LSB). This is bit [0] of 7:0. The lowest value might not be 0 depending on the number of bits allocated for priorities, and implementation choices.</p> |
| 2 | SYSRESETREQ | <p>Causes a signal to be asserted to the outer system that indicates a reset is requested. Intended to force a large system reset of all major components except for debug. Setting this bit does not prevent Halting Debug from running.</p> |
| 1 | VECTCLRACTIVE | <p>Clear active vector bit:</p> <p>1 = clear all state information for active NMI, fault, and interrupts</p> <p>0 = do not clear.</p> <p>It is the responsibility of the application to reinitialize the stack. The VECTCLRACTIVE bit is for returning to a known state during debug. The VECTCLRACTIVE bit self-clears. IPSR is not cleared by this operation. So, if used by an application, it must only be used at the base level of activation, or within a system handler whose active bit can be set.</p> |
| 0 | VECTRESET | <p>System Reset bit. Resets the system, with the exception of debug components:</p> <p>1 = reset system</p> <p>0 = do not reset system.</p> <p>The VECTRESET bit self-clears. Reset clears the VECTRESET bit. For debugging, only write this bit when the core is halted.</p> |

1.3.1582 NVIC_SYSTEM_CONTROL

System Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYSTEM_CONTROL: 0xE00ED10

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|----------------|------|----------------|------------------|------|
| SW Access:Reset | NA:000 | | | R/W:0 | NA:0 | R/W:0 | R/W:0 | NA:0 |
| HW Access | NA | | | R/W | NA | R/W | R/W | NA |
| Name | | | | SEVON- PEND | | SLEEP- DEEP | SLEEPON- EXIT | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the System Control Register for power-management functions: o signal to the system when the processor can enter a low power state o control how the processor enters and exits low power states.

| Bits | Name | Description |
|------|-------------|--|
| 4 | SEVONPEND | When enabled, this causes WFE to wake up when an interrupt moves from inactive to pended. Otherwise, WFE only wakes up from an event signal, external and SEV instruction generated. The event input, RXEV, is registered even when not waiting for an event, and so effects the next WFE. |
| 2 | SLEEPDEEP | Sleep deep bit: 1 = indicates to the system that Cortex-M3 clock can be stopped. Setting this bit causes the SLEEPDEEP port to be asserted when the processor can be stopped. 0 = not OK to turn off system clock. |
| 1 | SLEEPONEXIT | Sleep on exit when returning from Handler mode to Thread mode: 1 = sleep on ISR exit. 0 = do not sleep when returning to Thread mode. Enables interrupt driven applications to avoid returning to empty main application. |

1.3.1583 NVIC_CFG_CONTROL

Configuration Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_CFG_CONTROL: 0xE000ED14

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|-----------|-------------|------|---------------|-------------------|
| SW Access:Reset | NA:000 | | | R/W:0 | R/W:0 | NA:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | R/W | R/W | NA | R/W | R/W |
| Name | | | | DIV_0_TRP | UNALIGN_TRP | | USERSET-MPEND | NONE-BASETHRD ENA |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-----------|----|----|----|----|----|----------|------------|
| SW Access:Reset | NA:000000 | | | | | | R/W:1 | R/W:0 |
| HW Access | NA | | | | | | R/W | R/W |
| Name | | | | | | | STKALIGN | BFHFN-MIGN |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the Configuration Control Register to: enable NMI, Hard Fault and FAULTMASK to ignore bus fault trap divide by zero, and unaligned accesses enable user access to the Software Trigger Exception Register control entry to Thread Mode.

| Bits | Name | Description |
|------|-----------|--|
| 9 | STKALIGN | 1 = on exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. 0 = only 4-byte alignment is guaranteed for the SP used prior to the exception on exception entry. |
| 8 | BFHFNMIGN | When enabled, this causes handlers running at priority -1 and -2 (Hard Fault, NMI, and FAULTMASK escalated handlers) to ignore Data Bus faults caused by load and store instructions. When disabled, these bus faults cause a lock-up. You must only use this enable with extreme caution. All data bus faults are ignored - you must only use it when the handler and its data are in absolutely safe memory. Its normal use is to probe system devices and bridges to detect control path problems and fix them. |
| 4 | DIV_0_TRP | Trap on Divide by 0. This enables faulting/halting when an attempt is made to divide by 0. |

1.3.1583 NVIC_CFG_CONTROL (continued)

| | | |
|---|-----------------|--|
| 3 | UNALIGN_TRP | Trap for unaligned access. This enables faulting/halting on any unaligned half or full word access. Unaligned load-store multiples always fault. |
| 1 | USERSETMPEND | If written as 1, enables user code to write the Software Trigger Interrupt register to trigger (pend) a Main exception, which is one associated with the Main stack pointer. |
| 0 | NONEBASETHRDENA | When 0, default, It is only possible to enter Thread mode when returning from the last exception. When set to 1, Thread mode can be entered from any level in Handler mode by controlled return value. |

1.3.1584 NVIC_SYS_Prio_HANDLER_4_7

System Handler Priority Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYS_Prio_HANDLER_4_7: 0xE000ED18

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:000 | | | NA:00000 | | | | |
| HW Access | R/W | | | NA | | | | |
| Name | PRI_N | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|---------|----|----|----------|----|----|---|---|
| SW Access:Reset | R/W:000 | | | NA:00000 | | | | |
| HW Access | R/W | | | NA | | | | |
| Name | PRI_N1 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|---------|----|----|----------|----|----|----|----|
| SW Access:Reset | R/W:000 | | | NA:00000 | | | | |
| HW Access | R/W | | | NA | | | | |
| Name | PRI_N2 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the three System Handler Priority Registers to prioritize the following system handlers: o memory manage o bus fault o usage fault o debug monitor o SVC o SysTick o PendSV. System handlers are a special class of exception handler that can have their priority set to any of the priority levels. Most can be masked on (enabled) or off (disabled). When disabled, the fault is always treated as a Hard Fault.

| Bits | Name | Description |
|-------|-------------|--|
| 23:21 | PRI_N2[2:0] | Priority of system handler 6 - Usage Fault |
| 15:13 | PRI_N1[2:0] | Priority of system handler 5 - Bus Fault |
| 7:5 | PRI_N[2:0] | Priority of system handler 4 - Mem Manage |



0xe00ed1c

1.3.1585 NVIC_SYS_Prio_Handler_8_11

System Handler Priority Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYS_Prio_Handler_8_11: 0xE00ED1C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|---|---|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|----|----------|----|----|----|----|
| SW Access:Reset | R/W:000 | | | NA:00000 | | | | |
| HW Access | R/W | | | NA | | | | |
| Name | PRI_N3 | | | | | | | |

Use the three System Handler Priority Registers to prioritize the following system handlers: o memory manage o bus fault o usage fault o debug monitor o SVC o SysTick o PendSV. System handlers are a special class of exception handler that can have their priority set to any of the priority levels. Most can be masked on (enabled) or off (disabled). When disabled, the fault is always treated as a Hard Fault.

| Bits | Name | Description |
|-------|-------------|---|
| 31:29 | PRI_N3[2:0] | Priority of system handler 11 - SVCcall |

1.3.1586 NVIC_SYS_PRIO_HANDLER_12_15

System Handler Priority Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYS_PRIO_HANDLER_12_15: 0xE000ED20

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|----------|---|---|---|---|
| SW Access:Reset | R/W:000 | | | NA:00000 | | | | |
| HW Access | R/W | | | NA | | | | |
| Name | PRI_N | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|---------|----|----|----------|----|----|----|----|
| SW Access:Reset | R/W:000 | | | NA:00000 | | | | |
| HW Access | R/W | | | NA | | | | |
| Name | PRI_N2 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|---------|----|----|----------|----|----|----|----|
| SW Access:Reset | R/W:000 | | | NA:00000 | | | | |
| HW Access | R/W | | | NA | | | | |
| Name | PRI_N3 | | | | | | | |

Use the three System Handler Priority Registers to prioritize the following system handlers: o memory manage o bus fault o usage fault o debug monitor o SVC o SysTick o PendSV. System handlers are a special class of exception handler that can have their priority set to any of the priority levels. Most can be masked on (enabled) or off (disabled). When disabled, the fault is always treated as a Hard Fault.

| Bits | Name | Description |
|-------|-------------|--|
| 31:29 | PRI_N3[2:0] | Priority of system handler 15 - SysTick. |
| 23:21 | PRI_N2[2:0] | Priority of system handler 14 - PendSV. |
| 7:5 | PRI_N[2:0] | Priority of system handler 12 - Debug Monitor. |

1.3.1587 NVIC_SYS_HANDLER_CSR

System Handler Control and State Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYS_HANDLER_CSR: 0xE000ED24

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|--------|---|---|--------------|------|--------------|--------------|
| SW Access:Reset | R/W:0 | NA:000 | | | R/W:0 | NA:0 | R/W:0 | R/W:0 |
| HW Access | R/W | NA | | | R/W | NA | R/W | R/W |
| Name | SVCAL-LACT | | | | USGFAULT-ACT | | BUSFAULT-ACT | MEMFAUL-TACT |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|----------------|-----------------|----------------|-------------|------------|------|-------------|
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:0 | R/W:0 |
| HW Access | R/W | R/W | R/W | R/W | R/W | R/W | NA | R/W |
| Name | SVCALL-PENDE | BUSFAULT-PENDE | MEM-FAULT-PENDE | USGFAULT-PENDE | SYSTICK-ACT | PENDS-VACT | | MONITO-RACT |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|----------|----|----|----|----|--------------|--------------|--------------|
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R/W | R/W | R/W |
| Name | | | | | | USGFAULT-ENA | BUSFAULT-ENA | MEM-FAULTENA |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the System Handler Control and State Register to:

- o enable or disable the system handlers
- o determine the pending status of bus fault, mem manage fault, and SVC
- o determine the active status of the system handlers.
- o If a fault condition occurs while its fault handler is disabled, the fault escalates to a Hard Fault.

| Bits | Name | Description |
|------|---------------|--|
| 18 | USGFAULTENA | Enable for UsageFault. Set to 0 to disable, else 1 for enabled. |
| 17 | BUSFAULTENA | Enable for BusFault. Set to 0 to disable, else 1 for enabled. |
| 16 | MEMFAULTENA | Enable for MemManage fault. Set to 0 to disable, else 1 for enabled. |
| 15 | SVCALLPENDE | Reads as 1 if SVCcall is pending. |
| 14 | BUSFAULTPENDE | Reads as 1 if BusFault is pending. |
| 13 | MEMFAULTPENDE | Reads as 1 if MemManage is pending. |
| 12 | USGFAULTPENDE | Read as 1 if usage fault is pending. |

1.3.1587 NVIC_SYS_HANDLER_CSR (continued)

| | | |
|----|-------------|--------------------------------------|
| 11 | SYSTICKACT | Reads as 1 if SysTick is active. |
| 10 | PENDSVACT | Reads as 1 if PendSV is active. |
| 8 | MONITORACT | Reads as 1 if the Monitor is active. |
| 7 | SVCALLACT | Reads as 1 if SVCAll is active. |
| 3 | USGFAULTACT | Reads as 1 if UsageFault is active. |
| 1 | BUSFAULTACT | Reads as 1 if BusFault is active. |
| 0 | MEMFAULTACT | Reads as 1 if MemManage is active. |

1.3.1588 NVIC_MEMMAN_FAULT_STATUS

Memory Manage Fault Status Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_MEMMAN_FAULT_STATUS: 0xE00ED28

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|-------|---|---------|------------|------|----------|----------|
| SW Access:Reset | R/WOC:0 | NA:00 | | R/WOC:0 | R/WOC:0 | NA:0 | R/WOC:0 | R/WOC:0 |
| HW Access | R/W | NA | | R/W | R/W | NA | R/W | R/W |
| Name | MMARVAL-ID | | | MSTKERR | MUNSTK-ERR | | DACCVIOL | IACCVIOL |

The flags in the Memory Manage Fault Status Register indicate the cause of memory access faults.

| Bits | Name | Description |
|------|-----------|--|
| 7 | MMARVALID | Memory Manage Address Register (MMAR) address valid flag: 1 = valid fault address in MMAR. A later-arriving fault, such as a bus fault, can clear a memory manage fault. 0 = no valid fault address in MMAR. If a MemManage fault occurs that is escalated to a Hard Fault because of priority, the Hard Fault handler must clear this bit. This prevents problems on return to a stacked active MemManage handler whose MMAR value has been overwritten. |
| 4 | MSTKERR | Stacking from exception has caused one or more access violations. The SP is still adjusted and the values in the context area on the stack might be incorrect. The MMAR is not written. |
| 3 | MUNSTKERR | Unstack from exception return has caused one or more access violations. This is chained to the handler, so that the original return stack is still present. SP is not adjusted from failing return and new save is not performed. The MMAR is not written. |
| 1 | DACCVIOL | Data access violation flag. Attempting to load or store at a location that does not permit the operation sets the DACCVIOL flag. The return PC points to the faulting instruction. This error loads MMAR with the address of the attempted access. |
| 0 | IACCVIOL | Instruction access violation flag. Attempting to fetch an instruction from a location that does not permit execution sets the IACCVIOL flag. This occurs on any access to an XN region, even when the MPU is disabled or not present. The return PC points to the faulting instruction. The MMAR is not written. |

1.3.1589 NVIC_BUS_FAULT_STATUS

Bus Fault Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_BUS_FAULT_STATUS: 0xE000ED29

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|-------|---|---------|----------|--------------|------------|---------|
| SW Access:Reset | R/WOC:0 | NA:00 | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | R/W | NA | | R/W | R/W | R/W | R/W | R/W |
| Name | BFARVALID | | | STKERR | UNSTKERR | IMPRECIS-ERR | PRECIS-ERR | IBUSERR |

The flags in the Bus Fault Status Register indicate the cause of bus access faults.

| Bits | Name | Description |
|------|-------------|--|
| 7 | BFARVALID | This bit is set if the Bus Fault Address Register (BFAR) contains a valid address. This is true after a bus fault where the address is known. Other faults can clear this bit, such as a MemManage fault occurring later. If a Bus fault occurs that is escalated to a Hard Fault because of priority, the Hard Fault handler must clear this bit. This prevents problems if returning to a stacked active Bus fault handler whose BFAR value has been overwritten. |
| 4 | STKERR | Stacking from exception has caused one or more bus faults. The SP is still adjusted and the values in the context area on the stack might be incorrect. The BFAR is not written. |
| 3 | UNSTKERR | Unstack from exception return has caused one or more bus faults. This is chained to the handler, so that the original return stack is still present. SP is not adjusted from failing return and new save is not performed. The BFAR is not written. |
| 2 | IMPRECISERR | Imprecise data bus error. It is a BusFault, but the Return PC is not related to the causing instruction. This is not a synchronous fault. So, if detected when the priority of the current activation is higher than the Bus Fault, it only pends. Bus fault activates when returning to a lower priority activation. If a precise fault occurs before returning to a lower priority exception, the handler detects both IMPRECISERR set and one of the precise fault status bits set at the same time. The BFAR is not written. |
| 1 | PRECISERR | Precise data bus error return. |
| 0 | IBUSERR | Instruction bus error flag: 1 = instruction bus error 0 = no instruction bus error. The IBUSERR flag is set by a prefetch error. The fault stops on the instruction, so if the error occurs under a branch shadow, no fault occurs. The BFAR is not written. |

1.3.1590 NVIC_USAGE_FAULT_STATUS

Usage Fault Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_USAGE_FAULT_STATUS: 0xE00ED2A

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------|---------|----------|------------|
| SW Access:Reset | NA:0000 | | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | NOCP | INVPC | INVSTATE | UNDEFINSTR |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-----------|----|----|----|----|----|-----------|-----------|
| SW Access:Reset | NA:000000 | | | | | | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | | | | R/W | R/W |
| Name | | | | | | | DIVBYZERO | UNALIGNED |

The flags in the Usage Fault Status Register indicate the following errors: o illegal combination of EPSR and instruction o illegal PC load o illegal processor state o instruction decode error o attempt to use a coprocessor instruction o illegal unaligned access.

| Bits | Name | Description |
|------|------------|--|
| 9 | DIVBYZERO | When DIV_0_TRP (see Configuration Control Register) is enabled and an SDIV or UDIV instruction is used with a divisor of 0, this fault occurs. The instruction is executed and the return PC points to it. If DIV_0_TRP is not set, then the divide returns a quotient of 0. |
| 8 | UNALIGNED | When UNALIGN_TRP is enabled (see Configuration Control Register), and there is an attempt to make an unaligned memory access, then this fault occurs. Unaligned LDM/STM/LDRD/STRD instructions always fault irrespective of the setting of UNALIGN_TRP. |
| 3 | NOCP | Attempt to use a coprocessor instruction. The processor does not support coprocessor instructions. |
| 2 | INVPC | Attempt to load EXC_RETURN into PC illegally. Invalid instruction, invalid context, invalid value. The return PC points to the instruction that tried to set the PC. |
| 1 | INVSTATE | Invalid combination of EPSR and instruction, for reasons other than UNDEFINED instruction. Return PC points to faulting instruction, with the invalid state. |
| 0 | UNDEFINSTR | The UNDEFINSTR flag is set when the processor attempts to execute an undefined instruction. This is an instruction that the processor cannot decode. The return PC points to the undefined instruction. |

1.3.1591 NVIC_HARD_FAULT_STATUS

Hard Fault Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_HARD_FAULT_STATUS: 0xE000ED2C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|---------|------|
| SW Access:Reset | NA:000000 | | | | | | R/WOC:0 | NA:0 |
| HW Access | NA | | | | | | R/W | NA |
| Name | | | | | | | VECTTB | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|----------|---------|-----------|----|----|----|----|----|
| SW Access:Reset | R/WOC:0 | R/WOC:0 | NA:000000 | | | | | |
| HW Access | R/W | R/W | NA | | | | | |
| Name | DEBUGEVT | FORCED | | | | | | |

Use the Hard Fault Status Register (HFSR) to obtain information about events that activate the Hard Fault handler.

| Bits | Name | Description |
|------|----------|--|
| 31 | DEBUGEVT | This bit is set if there is a fault related to debug. This is only possible when halting debug is not enabled. For monitor enabled debug, it only happens for BKPT when the current priority is higher than the monitor. When both halting and monitor debug are disabled, it only happens for debug events that are not ignored (minimally, BKPT). The Debug Fault Status Register is updated. |
| 30 | FORCED | Hard Fault activated because a Configurable Fault was received and cannot activate because of priority or because the Configurable Fault is disabled. The Hard Fault handler then has to read the other fault status registers to determine cause. |
| 1 | VECTTB | This bit is set if there is a fault because of vector table read on exception processing (Bus Fault). This case is always a Hard Fault. The return PC points to the pre-empted instruction. |



0xe000ed30

1.3.1592 NVIC_DEBUG_FAULT_STATUS

Debug Fault Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_DEBUG_FAULT_STATUS: 0xE000ED30

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|----------|---------|---------|---------|---------|
| SW Access:Reset | NA:000 | | | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 | R/WOC:0 |
| HW Access | NA | | | R/W | R/W | R/W | R/W | R/W |
| Name | | | | EXTERNAL | VCATCH | DWTTRAP | BKPT | HALTED |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the Debug Fault Status Register to monitor: o external debug requests o vector catches o data watchpoint match o BKPT instruction execution o alt requests. Multiple flags in the Debug Fault Status Register can be set when multiple fault conditions occur. The register is read/write clear. This means that it can be read normally. Writing a 1 to a bit clears that bit.

| Bits | Name | Description |
|------|----------|---|
| 4 | EXTERNAL | External debug request flag: 1 = EDBGRRQ signal asserted 0 = EDBGRRQ signal not asserted. The processor stops on next instruction boundary. |
| 3 | VCATCH | Vector catch flag: 1 = vector catch occurred 0 = no vector catch occurred. When the VCATCH flag is set, a flag in one of the local fault status registers is also set to indicate the type of fault. |
| 2 | DWTTRAP | Data Watchpoint and Trace (DWT) flag: 1 = DWT match 0 = no DWT match. The processor stops at the current instruction or at the next instruction. |

1.3.1592 NVIC_DEBUG_FAULT_STATUS (continued)

| | | |
|---|--------|---|
| 1 | BKPT | <p>BKPT flag: 1 = BKPT instruction execution 0 = no BKPT instruction execution. The BKPT flag is set by a BKPT instruction in flash patch code, and also by normal code. Return PC points to breakpoint containing instruction.</p> |
| 0 | HALTED | <p>Halt request flag: 1 = halt requested by NVIC, including step. The processor is halted on the next instruction. 0 = no halt request.</p> |

0xe00ed34

1.3.1593 NVIC_MEMMAN_FAULT_ADD

Memory Manage Fault Address Register

Reset: N/A

Register : Address

NVIC_MEMMAN_FAULT_ADD: 0xE00ED34

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ADDRESS | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ADDRESS | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ADDRESS | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ADDRESS | | | | | | | |

Use the Memory Manage Fault Address Register to read the address of the location that caused a Memory Manage Fault.

| Bits | Name | Description |
|------|---------------|---|
| 31:0 | ADDRESS[31:0] | Mem Manage fault address field. ADDRESS is the data address of a faulted load or store attempt. When an unaligned access faults, the address is the actual address that faulted. Because an access can be split into multiple parts, each aligned, this address can be any offset in the range of the requested size. Flags in the Memory Manage Fault Status Register indicate the cause of the fault. |

1.3.1594 NVIC_BUS_FAULT_ADD

Bus Fault Address Register

Reset: N/A

Register : Address

NVIC_BUS_FAULT_ADD: 0xE000ED38

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ADDRESS | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ADDRESS | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ADDRESS | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | ADDRESS | | | | | | | |

Use the Bus Fault Address Register to read the address of the location that generated a Bus Fault.

| Bits | Name | Description |
|------|---------------|--|
| 31:0 | ADDRESS[31:0] | Bus fault address field. ADDRESS is the data address of a faulted load or store attempt. When an unaligned access faults, the address is the address requested by the instruction, even if that is not the address that faulted. Flags in the Bus Fault Status Register indicate the cause of the fault. |

1.3.1595 CORE_DBG_DBG_HLT_CS

Debug Halting Control and Status register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CORE_DBG_DBG_HLT_CS: 0xE000EDF0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|----|-----------------|------|-----------------|---------|----------------|-----------------|
| SW Access:Reset | NA:00 | | R/W:0 | NA:0 | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | R | NA | R | R | R | R |
| Name | | | C_SNAPST ALL | | C_MASKIN TSK | C_STEP | C_HALT | C_DEBUGE N |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:0000 | | | | R:0 | R:0 | R:0 | R:0 |
| HW Access | NA | | | | R/W | R/W | R/W | R/W |
| Name | | | | | S_LOCKUP | S_SLEEP | S_HALT | S_REGRDY G |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:000000 | | | | | | R:0 | R:0 |
| HW Access | NA | | | | | | R/W | R/W |
| Name | | | | | | | S_RESET_ ST | S_RETIRE_ ST |

The purpose of the Debug Halting Control and Status Register (DHCSR) is to: o provide status information about the state of the processor o enable core debug o halt and step the processor. NOTE: Bits[31:16] have a separate write path. Debug Key. 0xA05F must be written whenever this register is written. Reads back as status bits [25:16]. If not written as Key, the write operation is ignored and no bits are written into the register.

| Bits | Name | Description |
|------|-------------|---|
| 25 | S_RESET_ST | Indicates that the core has been reset, or is now being reset, since the last time this bit was read. This is a sticky bit that clears on read. So, reading twice and getting 1 then 0 means it was reset in the past. Reading twice and getting 1 both times means that it is being reset now (held in reset still). |
| 24 | S_RETIRE_ST | Indicates that an instruction has completed since last read. This is a sticky bit that clears on read. This determines if the core is stalled on a load/store or fetch. |
| 19 | S_LOCKUP | Reads as one if the core is running (not halted) and a lockup condition is present. |
| 18 | S_SLEEP | Indicates that the core is sleeping (WFI, WFE or SLEEP-ON-EXIT). Must use C_HALT to gain control or wait for interrupt to wake-up. |

1.3.1595 CORE_DBG_DBG_HLT_CS (continued)

| | | |
|----|-------------|---|
| 17 | S_HALT | The core is in debug state when S_HALT is set. |
| 16 | S_REGRDYG | Register Read/Write on the Debug Core Register Selector register is available. Last transfer is complete. |
| 5 | C_SNAPSTALL | <p>If the core is stalled on a load/store operation the stall ceases and the instruction is forced to complete. This enables Halting debug to gain control of the core. It can only be set if:</p> <p>C_DEBUGEN = 1 C_HALT = 1</p> <p>The core reads S_RETIRE_ST as 0. This indicates that no instruction has advanced. This prevents misuse. The bus state is Unpredictable when this is used. S_RETIRE can detect core stalls on load/store operations.</p> |
| 3 | C_MASKINTSK | Mask interrupts when stepping or running in halted debug. Does not affect NMI, which is not maskable. Must only be modified when the processor is halted (S_HALT == 1). |
| 2 | C_STEP | Steps the core in halted debug. When C_DEBUGEN = 0, this bit has no effect. Must only be modified when the processor is halted (S_HALT == 1). |
| 1 | C_HALT | Halts the core. This bit is set automatically when the core Halts. For example Breakpoint. This bit clears on core reset. This bit can only be written if C_DEBUGEN is 1, otherwise it is ignored. When setting this bit to 1, C_DEBUGEN must also be written to 1 in the same value (value[1:0] is 2'b11). The core can halt itself, but only if C_DEBUGEN is already 1 and only if it writes with b11). |
| 0 | C_DEBUGEN | Enables debug. This can only be written by AHB-AP and not by the core. It is ignored when written by the core, which cannot set or clear it. The core must write a 1 to it when writing C_HALT to halt itself. |

1.3.1596 CORE_DBG_DBG_REG_SEL

Debug Core Register Selector Register

Reset: N/A

Register : Address

CORE_DBG_DBG_REG_SEL: 0xE00EDF4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|---------|---|---|---|---|
| SW Access:Reset | NA:000 | | | W:UUUUU | | | | |
| HW Access | NA | | | R/W | | | | |
| Name | | | | REGSEL | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|--------|
| SW Access:Reset | NA:0000000 | | | | | | | W:U |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | REGWnR |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The purpose of the Debug Core Register Selector Register (DCRSR) is to select the processor register to transfer data to or from. This write-only register generates a handshake to the core to transfer data to or from Debug Core Register Data Register and the selected register. Until this core transaction is complete, bit[16], S_REGRDY, of the DHCSR is 0. NOTE: o Writes to this register in any size but word are Unpredictable. o PSR registers are fully accessible this way, whereas some read as 0 when using MSR instructions. o All bits can be written, but some combinations cause a fault when execution is resumed. o IT might be written and behaves as though in an IT block. o ICI can be written, though invalid values or when not used on an LDM/STM causes a fault, as would on return from exception. changing ICI from a value to 0 causes the underlying LDM/STM to start, not continue.

| Bits | Name | Description |
|------|--------|-----------------------|
| 16 | REGWnR | Write = 1 Read = 0 |

1.3.1596 CORE_DBG_DBG_REG_SEL (continued)

| | | |
|-----|-------------|--|
| 4:0 | REGSEL[4:0] | 5'b00000 = R0 5'b00001 = R1 ... 5'b01111 = DebugReturnAddress() 5'b10000 = xPSR/Flags, Execution Number, and state information 5'b10001 = MSP (Main SP) 5'b10010 = PSP (Process SP) 5'b10011 = RAZ/WI All unused values reserved |
|-----|-------------|--|

1.3.1597 CORE_DBG_DBG_REG_DATA

Debug Core Register Data Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CORE_DBG_DBG_REG_DATA: 0xE000EDF8

| | | | | | | | | |
|-----------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DATA | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DATA | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DATA | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | DATA | | | | | | | |

The purpose of the Debug Core Register Data Register (DCRDR) is to hold data for reading and writing registers to and from the processor. This is the data value written to the register selected by the DCRSR. When the processor receives a request from the DCRS, this register is read or written by the processor using a normal load-store unit operation. If core register transfers are not being performed, software-based debug monitors can use this register for communication in non-halting debug.

| Bits | Name | Description |
|------|------------|------------------|
| 31:0 | DATA[31:0] | (no description) |

1.3.1598 CORE_DBG_EXC_MON_CTL

Debug Exception and Monitor Control register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CORE_DBG_EXC_MON_CTL: 0xE00EDFC

| | | | | | | | | |
|-----------------|----------------|---------------|----------------|---------------|-----------|-----------------|---------------|------------------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R/W:0 | R/W:0 | R/W:0 | R/W:0 | NA:000 | | | R/W:0 |
| HW Access | R | R | R | R | NA | | | R |
| Name | VC_STATE RR | VC_CHKER R | VC_NOCP RRC | VC_MMER RM | | | | VC_CORE RESET |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000 | | | | | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | | R | R | R |
| Name | | | | | | VC_HARDE RRR | VC_INTER R | VC_BUSER R |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R/W:0 | R/W:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | MON_REQ | MON_STEP | MON_PEN D | MON_EN |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | TRCENA |

The purpose of the Debug Exception and Monitor Control Register (DEMCR) is:

- o Vector catching. That is, to cause debug entry when a specified vector is committed for execution.
- o Debug monitor control.

| Bits | Name | Description |
|------|---------|--|
| 24 | TRCENA | This bit must be set to 1 to enable use of the trace and debug blocks: <ul style="list-style-type: none"> o Data Watchpoint and Trace (DWT) o Instrumentation Trace Macrocell (ITM) o Embedded Trace Macrocell (ETM) o Trace Port Interface Unit (TPIU). This enables control of power usage unless tracing is required. The application can enable this, for ITM use, or use by a debugger. |
| 19 | MON_REQ | This enables the monitor to identify how it wakes up: <ul style="list-style-type: none"> 1 = woken up by MON_PEND 0 = woken up by debug exception. |

1.3.1598 CORE_DBG_EXC_MON_CTL (continued)

| | | |
|----|--------------|--|
| 18 | MON_STEP | When MON_EN = 1, this steps the core. When MON_EN = 0, this bit is ignored. This is the equivalent to C_STEP. Interrupts are only stepped according to the priority of the monitor and settings of PRIMASK, FAULTMASK, or BASEPRI. |
| 17 | MON_PEND | Pend the monitor to activate when priority permits. This can wake up the monitor through the AHB-AP port. It is the equivalent to C_HALT for Monitor debug. This register does not reset on a system reset. It is only reset by a power-on reset. Software in the reset handler or later, or by the DAP must enable the debug monitor. |
| 16 | MON_EN | Enable the debug monitor. When enabled, the System handler priority register controls its priority level. If disabled, then all debug events go to Hard fault. C_DEBUGEN in the Debug Halting Control and Statue register overrides this bit. Vector catching is semi-synchronous. When a matching event is seen, a Halt is requested. Because the processor can only halt on an instruction boundary, it must wait until the next instruction boundary. As a result, it stops on the first instruction of the exception handler. However, two special cases exist when a vector catch has triggered: <ul style="list-style-type: none"> o If a fault is taken during vectoring, vector read or stack push error, the halt occurs on the corresponding fault handler, for the vector error or stack push. o If a late arriving interrupt comes in during vectoring, it is not taken. That is, an implementation that supports the late arrival optimization must suppress it in this case. |
| 10 | VC_HARDERRR | Debug trap on Hard Fault. |
| 9 | VC_INTERR | Debug Trap on interrupt/exception service errors. These are a subset of other faults and catches before BUSERR or HARDERR. |
| 8 | VC_BUSERR | Debug Trap on normal Bus error. |
| 7 | VC_STATERR | Debug trap on Usage Fault state errors. |
| 6 | VC_CHKERR | Debug trap on Usage Fault enabled checking errors. |
| 5 | VC_NOCPERRC | Debug trap on Usage Fault access to Coprocessor which is not present or marked as not present in CAR register. |
| 4 | VC_MMERRM | Debug trap on Memory Management faults. |
| 0 | VC_CORERESET | Reset Vector Catch. Halt running system if Core reset occurs. |

1.3.1599 TPIU_SUPPORTED_SYNC_PRT_SZ

Supported Sync Port Sizes Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_SUPPORTED_SYNC_PRT_SZ: 0xE0040000

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------------------|---|---|---|--------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R:1011 | | | |
| HW Access | NA | | | | R | | | |
| Name | SUPPORTED_SYNC_PRT_SZ | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register is read/write. Each bit location represents a single port size that is supported on the device, that is, 4, 2 or 1 in bit locations [3:0]. If the bit is set then that port size is permitted. By default the RTL is designed to support all port sizes, set to 0x0000000B. This register is constrained by the input tie-off MAXPORTSIZE. The external tie-off, MAXPORTSIZE, must be set during finalization of the ASIC to reflect the actual number of TRACEDATA signals wired to physical pins. This is to ensure that tools do not attempt to select a port width that an attached TPA cannot capture. The value on MAXPORTSIZE causes bits within the Supported Port Size register that represent wider widths to be clear, that is, unsupported.

| Bits | Name | Description |
|------|----------------------------|-------------|
| 3:0 | SUPPORTED_SYNC_PRT_SZ[3:0] | Port size |

1.3.1600 TPIU_CURRENT_SYNC_PRT_SZ

Current Sync Port Size Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_CURRENT_SYNC_PRT_SZ: 0xE0040004

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------------------|---|---|---|----------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0001 | | | |
| HW Access | NA | | | | R | | | |
| Name | CURRENT_SYNC_PRT_SZ | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

This register is read/write. The Current Sync Port Size Register has the same format as the Supported Sync Port Sizes Register but only one bit is set, and all others must be zero. Writing values with more than one bit set, or setting a bit that is not indicated as supported is not supported and causes Unpredictable behavior. It is more convenient to use the same format as the Supported Sync Port Sizes Register because it saves on having to decode the sizes later on in the device, and also maintains the format from the other register bank for checking for valid assignments. On reset this defaults to the smallest possible port size, 1 bit, and so reads as 0x00000001.

| Bits | Name | Description |
|------|--------------------------|-------------|
| 3:0 | CURRENT_SYNC_PRT_SZ[3:0] | Port size |

1.3.1601 TPIU_ASYNC_CLK_PRESCALER

Async Clock Prescaler Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_ASYNC_CLK_PRESCALER: 0xE0040010

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|---|---|---|---|---|
| SW Access:Reset | R/W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | PRESCALER | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------|----|----|-----------|----|----|---|---|
| SW Access:Reset | NA:000 | | | R/W:00000 | | | | |
| HW Access | NA | | | R | | | | |
| Name | | | | PRESCALER | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the Async Clock Prescaler Register to scale the baud rate of the asynchronous output.

| Bits | Name | Description |
|------|-----------------|--|
| 12:0 | PRESCALER[12:0] | Divisor for TRACECLKIN is Prescaler + 1. |

1.3.1602 TPIU_PROTOCOL

Selected Pin Protocol Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_PROTOCOL: 0xE00400F0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|----------|---|
| SW Access:Reset | NA:000000 | | | | | | R/W:01 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | PROTOCOL | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the Selected Pin Protocol Register to select which protocol to use for trace output.

| Bits | Name | Description |
|------|---------------|--|
| 1:0 | PROTOCOL[1:0] | 00 - TracePort mode 01 - SerialWire Output (Manchester). This is the reset value. 10 - SerialWire Output (NRZ) 11 - Reserved. |

1.3.1603 TPIU_FORM_FLUSH_STAT

Formatter and Flush Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_FORM_FLUSH_STAT: 0xE0040300

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|-----------|-----------|----------|
| SW Access:Reset | NA:0000 | | | | R:1 | R:0 | R:0 | R:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | FtNonStop | TCPresent | FtStopped | FIInProg |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Formatter and Flush Status Register.

| Bits | Name | Description |
|------|-----------|-----------------------------|
| 3 | FtNonStop | Formatter cannot be stopped |
| 2 | TCPresent | This bit always reads zero |
| 1 | FtStopped | This bit always reads zero |
| 0 | FIInProg | This bit always reads zero |

1.3.1604 TPIU_FORM_FLUSH_CTRL

Formatter and Flush Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_FORM_FLUSH_CTRL: 0xE0040304

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|---|---|---------|------|
| SW Access:Reset | NA:000000 | | | | | | R/W:1 | NA:0 |
| HW Access | NA | | | | | | R | NA |
| Name | | | | | | | EnFCont | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|--------|
| SW Access:Reset | NA:0000000 | | | | | | | R:1 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | TrigIN |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Formatter and Flush Control Register.

| Bits | Name | Description |
|------|---------|--|
| 8 | TrigIN | Indicate a trigger on TRIGIN being asserted. This bit Reads-As-One (RAO), specifying that triggers are inserted when a trigger pin is asserted. |
| 1 | EnFCont | Continuous Formatting, no TRACECTL. This bit is set on reset. Note: If TPIU_PROTOCOL is set to select Parallel Port Mode, the formatter is automatically enabled. If you then select one of the SWO modes, TPIU_FORM_FLUSH_CTRL reverts to its previously programmed value. |

1.3.1605 TPIU_TRIGGER

Integration test of the TRIGGER input.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_TRIGGER: 0xE0040EE8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|-------------|
| SW Access:Reset | NA:0000000 | | | | | | | R:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | TRIGGER_VAL |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Integration test of the TRIGGER input.

| Bits | Name | Description |
|------|-------------|--|
| 0 | TRIGGER_VAL | When read, this bit returns the TRIGGER input. |

1.3.1606 TPIU_ITETMDATA

Integration ETM Data

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_ITETMDATA: 0xE0040EEC

| | | | | | | | | |
|-----------------|------------|-----------|-------------|---------------|-----------|-------------|---------------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ETM_Data0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ETM_Data1 | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ETM_Data2 | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00 | | R:0 | R:00 | | R:0 | R:00 | |
| HW Access | NA | | R | R | | R | R | |
| Name | | | ITM_ATVALID | ITM_ByteCount | | ETM_ATVALID | ETM_ByteCount | |

Trace data integration testing. You must set bit [1] of TPIU_ITCTRL to use this register.

| Bits | Name | Description |
|-------|--------------------|---|
| 29 | ITM_ATVALID | Returns the value of the ITM ATVALID signal. |
| 28:27 | ITM_ByteCount[1:0] | Number of bytes of ITM trace data since last read of Integration ITM Data Register. |
| 26 | ETM_ATVALID | Returns the value of the ETM ATVALID signal. |
| 25:24 | ETM_ByteCount[1:0] | Number of bytes of ETM trace data since last read of Integration ETM Data Register. |
| 23:16 | ETM_Data2[7:0] | ETM trace data. The TPIU discards this data when the register is read. |
| 15:8 | ETM_Data1[7:0] | ETM trace data. The TPIU discards this data when the register is read. |
| 7:0 | ETM_Data0[7:0] | ETM trace data. The TPIU discards this data when the register is read. |

1.3.1607 TPIU_ITATBCTR2

Integration Test Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_ITATBCTR2: 0xE0040EF0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|----------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | ATREADY1 |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the Integration Test Registers to perform topology detection of the TPIU with other devices in a Cortex-M3 system. These registers enable direct control of outputs and the ability to read the value of inputs. You must set bit [1] of TPIU_ITCTRL to use this register

| Bits | Name | Description |
|------|----------|--|
| 0 | ATREADY1 | This bit reads or sets the value of ATREADY1 and ATREADY2. |

1.3.1608 TPIU_ITATBCTR0

Integration Test Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_ITATBCTR0: 0xE0040EF8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|------------|
| SW Access:Reset | NA:0000000 | | | | | | | R:0 |
| HW Access | NA | | | | | | | R/W |
| Name | | | | | | | | ATVALID1_2 |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Use the Integration Test Registers to perform topology detection of the TPIU with other devices in a Cortex-M3 system. These registers enable direct control of outputs and the ability to read the value of inputs.

| Bits | Name | Description |
|------|------------|---|
| 0 | ATVALID1_2 | This bit reads the value of ATVALIDS1 OR-ed with ATVALIDS2. |

1.3.1609 TPIU_ITITMDATA

Integration ITM Data

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_ITITMDATA: 0xE0040EFC

| | | | | | | | | |
|-----------------|------------|-----------|----------------|---------------|-----------|----------------|---------------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ITM_Data0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ITM_Data1 | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ITM_Data2 | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00 | | R:0 | R:00 | | R:0 | R:00 | |
| HW Access | NA | | R | R | | R | R | |
| Name | | | ITM_ATVALID ID | ITM_ByteCount | | ETM_ATVALID ID | ETM_ByteCount | |

Trace data integration testing. You must set bit [1] of TPIU_ITCTRL to use this register.

| Bits | Name | Description |
|-------|--------------------|---|
| 29 | ITM_ATVALID | Returns the value of the ITM ATVALID signal. |
| 28:27 | ITM_ByteCount[1:0] | Number of bytes of ITM trace data since last read of Integration ITM Data Register. |
| 26 | ETM_ATVALID | Returns the value of the ETM ATVALID signal. |
| 25:24 | ETM_ByteCount[1:0] | Number of bytes of ETM trace data since last read of Integration ETM Data Register. |
| 23:16 | ITM_Data2[7:0] | ITM trace data. The TPIU discards this data when the register is read. |
| 15:8 | ITM_Data1[7:0] | ITM trace data. The TPIU discards this data when the register is read. |
| 7:0 | ITM_Data0[7:0] | ITM trace data. The TPIU discards this data when the register is read. |

1.3.1610 TPIU_ITCTRL

Integration Mode Control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_ITCTRL: 0xE0040F00

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | NA:000000 | | | | | | R/W:00 | |
| HW Access | NA | | | | | | R | |
| Name | | | | | | | Mode | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Specifies normal or integration mode for the TPIU.

| Bits | Name | Description |
|------|-----------|--|
| 1:0 | Mode[1:0] | <p>Specifies the current mode for the TPIU:</p> <ul style="list-style-type: none"> 0b00 normal mode 0b01 integration test mode 0b10 integration data test mode 0b11 Reserved. <p>In integration data test mode, the trace output is disabled, and data can be read directly from each input port using the integration data registers.</p> |

1.3.1611 TPIU_DEVID

TPIU Provided Function Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_DEVID: 0xE0040FC8

| | | | | | | | | |
|-----------------|-------------|-----------|-------------------|-------------|--------------|--------------|---------------|------------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:10 | | R:1 | R:00001 | | | | |
| HW Access | R | | R | R | | | | |
| Name | MinBufSize | | Async-TRACE-CLKIN | NumTraceInp | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:0000 | | | | R:1 | R:1 | R:0 | R:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | AsyncS-WONRZ | AsyncS-WOMan | ParTrace-Mode | MinBufSize |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Indicates the functions provided by the TPIU for use in topology detection.

| Bits | Name | Description |
|------|-----------------|---|
| 11 | AsyncSWONRZ | Asynchronous Serial Wire Output (NRZ). This bit Reads-As-One (RAO), indicating that the output is supported. |
| 10 | AsyncSWOMan | Asynchronous Serial Wire Output (Manchester). This bit Reads-As-One (RAO), indicating that the output is supported. |
| 9 | ParTraceMode | Parallel trace port mode. This bit Reads-As-Zero (RAZ), indicating that parallel trace port mode is supported. |
| 8:6 | MinBufSize[2:0] | Minimum buffer size. Specifies the minimum TPIU buffer size: 0b010 = 4 bytes. |
| 5 | AsyncTRACECLKIN | Specifies whether TRACECLKIN can be asynchronous to CLK: 0b1 = TRACECLKIN can be asynchronous to CLK. |

1.3.1611 TPIU_DEVID (continued)

| | | |
|-----|------------------|---|
| 4:0 | NumTraceInp[4:0] | Specifies the number of trace inputs: 0b000000 = 1 input 0b000001 = 2 inputs Since our implementation includes an ETM, the value of this field is 0b00001. |
|-----|------------------|---|

1.3.1612 TPIU_DEVTYPE

TPIU Device Type Identifier Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_DEVTYPE: 0xE0040FCC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-----------|---|---|---|
| SW Access:Reset | R:0001 | | | | R:0001 | | | |
| HW Access | R | | | | R | | | |
| Name | SubType | | | | MajorType | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Device Type Identifier Register is read-only. It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

| Bits | Name | Description |
|------|----------------|-------------|
| 7:4 | SubType[3:0] | Sub type |
| 3:0 | MajorType[3:0] | Major type |

1.3.1613 TPIU_PID4

TPIU Peripheral Identification Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_PID4: 0xE0040FD0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000100 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID4 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Peripheral Identification Register 4

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID4[7:0] | Peripheral Identification Register 4 |

1.3.1614 TPIU_PID5

TPIU Peripheral Identification Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_PID5: 0xE0040FD4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID5 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Peripheral Identification Register 5

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID5[7:0] | Peripheral Identification Register 5 |

1.3.1615 TPIU_PID6

TPIU Peripheral Identification Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_PID6: 0xE0040FD8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID6 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Peripheral Identification Register 6

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID6[7:0] | Peripheral Identification Register 6 |

1.3.1616 TPIU_PID7

TPIU Peripheral Identification Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_PID7: 0xE0040FDC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID7 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Peripheral Identification Register 7

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID7[7:0] | Peripheral Identification Register 7 |

1.3.1617 TPIU_PID0

TPIU Peripheral Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_PID0: 0xE0040FE0

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00100011 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Peripheral Identification Register 0

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID0[7:0] | Peripheral Identification Register 0 |

1.3.1618 TPIU_PID1

TPIU Peripheral Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_PID1: 0xE0040FE4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10111001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID1 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Peripheral Identification Register 1

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID1[7:0] | Peripheral Identification Register 1 |

1.3.1619 TPIU_PID2

TPIU Peripheral Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_PID2: 0xE0040FE8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00111011 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID2 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Peripheral Identification Register 2

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID2[7:0] | Peripheral Identification Register 2 |

1.3.1620 TPIU_PID3

TPIU Peripheral Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_PID3: 0xE0040FEC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID3 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Peripheral Identification Register 3

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID3[7:0] | Peripheral Identification Register 3 |

1.3.1621 TPIU_CID0

TPIU Component Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_CID0: 0xE0040FF0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00001101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Component Identification Register 0

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID0[7:0] | Component Identification Register 0 |

1.3.1622 TPIU_CID1

TPIU Component Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_CID1: 0xE0040FF4

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:10010000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID1 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Component Identification Register 1

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID1[7:0] | Component Identification Register 1 |

1.3.1623 TPIU_CID2

TPIU Component Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_CID2: 0xE0040FF8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID2 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Component Identification Register 2

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID2[7:0] | Component Identification Register 2 |

1.3.1624 TPIU_CID3

TPIU Component Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_CID3: 0xE0040FFC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10110001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID3 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

TPIU Component Identification Register 3

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID3[7:0] | Component Identification Register 3 |

1.3.1625 ETM_CTL

ETM Control register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CTL: 0xE0041000

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|----------|---|---|--------|---|---|-------|
| SW Access:Reset | R/W:0 | R/W:001 | | | NA:000 | | | R/W:1 |
| HW Access | R | R | | | NA | | | R |
| Name | STALL_uP | PRT_SIZE | | | | | | PD |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------|----|---------------|------|---------|-------|----------------|---------------|
| SW Access:Reset | NA:00 | | R:0 | NA:0 | R/W:0 | R/W:1 | R/W:0 | R/W:0 |
| HW Access | NA | | R | NA | R | R | R | R |
| Name | | | PRT_MODE 2 | | PRT_SEL | PROG | DBG_RQ_C TL | BRNCH_O UT |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------|----|-----------|--------|----|----|------------|----|
| SW Access:Reset | NA:00 | | R:0 | NA:000 | | | R:00 | |
| HW Access | NA | | R | NA | | | R | |
| Name | | | PRT_SIZE3 | | | | PRT_MODE10 | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------|----|----|-----------------------|---------|----|----|----|
| SW Access:Reset | NA:000 | | | R/W:0 | NA:0000 | | | |
| HW Access | NA | | | R | NA | | | |
| Name | | | | TIMESTAMP P_ENABLE | | | | |

ETM control register controls general operation of the ETM, such as whether tracing is enabled.

| Bits | Name | Description |
|-------|------------------|---|
| 28 | TIMESTAMP_ENABLE | When set, this bit enables timestamping. An ETM reset sets this bit to 0. |
| 21 | PRT_SIZE3 | These bits are implemented but have no function. On an ETM reset this bit is 0. |
| 17:16 | PRT_MODE10[1:0] | These bits are implemented but have no function. On ETM reset these bits are cleared to 0. |
| 13 | PRT_MODE2 | This bit is implemented but has no function. On an ETM reset this bit is 0. |
| 11 | PRT_SEL | This bit controls the external ETMEN pin. The possible values are: 0 ETMEN is LOW. 1 ETMEN is HIGH. This bit must be set by the trace software tools to ensure that trace output is enabled from this ETM. ETMEN can be used to enable the trace port pins to be shared with GPIO pins under the control of logic external to the ETM. On an ETM reset this bit is 0. |

1.3.1625 ETM_CTL (continued)

| | | |
|-----|---------------|---|
| 10 | PROG | <p>When set to 1, the ETM is being programmed. On an ETM reset this bit is set to b1.</p> |
| 9 | DBGRRQ_CTL | <p>When set to 1 and the trigger event occurs, the DBGRRQ output is asserted until DBGACK is observed. This enables the ARM processor to be forced into Debug state. On an ETM reset this bit is 0.</p> |
| 8 | BRNCH_OUT | <p>When set to 1 all branch addresses are output, even if the branch was because of a direct branch instruction. Setting this bit enables reconstruction of the program flow without having access to the memory image of the code being executed. On an ETM reset this bit is 0.</p> |
| 7 | STALL_uP | <p>The FIFOFULL output can be used to stall the processor to prevent overflow. This signal is only enabled when the stall processor bit is set to 1. When this bit is 0 the FIFOFULL output remains LOW at all times and the FIFO overflows if there are too many trace packets. On an ETM reset this bit is 0. If the FIFOFULL signal is not implemented then this bit reads as zero and ignores writes.</p> |
| 6:4 | PRT_SIZE[2:0] | <p>The port size determines how many external pins are available to output the trace information. In ETMv1 and ETMv2 the port size is the number of bits in TRACEPKT. In ETMv3 the port size is the number of bits in TRACEDATA. This configuration determines how quickly the trace packets are extracted from the FIFO. From ETMv3 the port size field is 4 bits wide and bits [6:4] must be used in conjunction with bit [21], so that the port size encoding is given by bits [21, 6:4]. On an ETM reset these bits correspond to the lowest supported port width.</p> |
| 0 | PD | <p>A pin controlled by this bit enables the ETM power to be controlled externally. The external pin is often ETMPWRDOWN or inverted as ETMPWRUP. This bit must be cleared by the trace software tools at the beginning of a debug session. When this bit is set to 1, the ETM must be powered down and disabled, and then operated in a low power mode with all clocks stopped. When this bit is set to 1, writes to some registers and fields might be ignored. You can always write to the following registers and fields:</p> <ul style="list-style-type: none"> o ETM Control Register, bit [0] and bits [27:25] o Lock Access Register o Claim Tag Set Register o Claim Tag Clear Register o Operating System Lock Access Register. o When the ETM Control Register is written with this bit set to 1, bits other than bit [0] and bits [27:25] might be ignored. <p>On an ETM reset this bit is set to 1.</p> |

1.3.1626 ETM_CFG_CODE

ETM Configuration code register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CFG_CODE: 0xE0041004

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-----------|---|---|---|----------|---|---|---|
| SW Access:Reset | R:0000 | | | | R:0000 | | | |
| HW Access | R | | | | R | | | |
| Name | DATA_CMPS | | | | ADD_CMPS | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|----------|----|----|----|-----------|----|---|---|
| SW Access:Reset | R:001 | | | | R:00000 | | | |
| HW Access | R | | | | R | | | |
| Name | COUNTERS | | | | MMD_INPUT | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|--------------|---------|----|----|--------|----|-----|----|
| SW Access:Reset | R:1 | R:000 | | | R:010 | | R:0 | |
| HW Access | R | R | | | R | | R | |
| Name | FIFOFULL_LGC | EXT_OUT | | | EXT_IN | | SEQ | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|--------|--------|----|----|---------------|------------------|------------|----|
| SW Access:Reset | R:1 | NA:000 | | | R:1 | R:1 | R:00 | |
| HW Access | R | NA | | | R | R | R | |
| Name | ETM_ID | | | | COPRC_SUPPORT | TRACE_START_STOP | CTXTID_CMP | |

The ETM Configuration Code Register enables the debugger to read the IMPLEMENTATION DEFINED configuration of the ETM, giving the number of each type of resource. Where a value indicates the number of instances of a particular resource, zero indicates that there are no implemented resources of that resource type.

| Bits | Name | Description |
|-------|------------------|--|
| 31 | ETM_ID | When set to 1, this bit indicates that the ETM ID Register, 0x79, is present and defines the ETM architecture version in use. When set to 0, this bit indicates that the ETM ID Register is not present. |
| 27 | COPRC_SUPPORT | Coprocessor or memory-mapped access to registers supported. |
| 26 | TRACE_START_STOP | When set to 1, the trace start/stop block is present. |
| 25:24 | CTXTID_CMP[1:0] | Number of Context ID comparators. |
| 23 | FIFOFULL_LGC | When set to 1, the FIFOFULL logic is present. This bit is used in conjunction with bit [8] of the System Configuration Register, register 0x05, of the processor core connected to the ETM. |
| 22:20 | EXT_OUT[2:0] | Number of external outputs. |
| 19:17 | EXT_IN[2:0] | Number of external inputs. |

1.3.1626 ETM_CFG_CODE (continued)

| | | |
|-------|----------------|--|
| 16 | SEQ | When set to b1 the sequencer is present. |
| 15:13 | COUNTERS[2:0] | Number of counters. |
| 12:8 | MMD_INPUT[4:0] | Number of memory map decoder inputs. |
| 7:4 | DATA_CMPS[3:0] | Number of data value comparators. |
| 3:0 | ADD_CMPS[3:0] | Number of pairs of address comparators. |

1.3.1627 ETM_TRIG_EVENT

Trigger Event Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_TRIG_EVENT: 0xE0041008

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|-----------|---|---|---|---|---|---|
| SW Access:Reset | W:0 | W:0000000 | | | | | | |
| HW Access | R | R | | | | | | |
| Name | RSRC_B | RSRC_A | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|----|----------|----|----|----|---|---|
| SW Access:Reset | W:00 | | W:000000 | | | | | |
| HW Access | R | | R | | | | | |
| Name | FCN | | RSRC_B | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|-----|
| SW Access:Reset | NA:0000000 | | | | | | | W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | FCN |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Trigger Event Register defines the event that controls the trigger.

| Bits | Name | Description |
|-------|-------------|-------------|
| 16:14 | FCN[2:0] | Fcn. |
| 13:7 | RSRC_B[6:0] | Resource B. |
| 6:0 | RSRC_A[6:0] | Resource A. |

1.3.1628 ETM_STATUS

ETM Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_STATUS: 0xE0041010

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|------------------|-----------|-------------------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | NA:0000 | | | | R/W:0 | R/W:0 | R:0 | R:0 |
| HW Access | NA | | | | R | R | R | R |
| Name | | | | | TRIG_BIT | TRACE_ST ATUS | PROG_BIT | OVERFLO W_FLAG |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The ETM Status Register provides information about the current status of the trace and trigger logic.

| Bits | Name | Description |
|------|---------------|--|
| 3 | TRIG_BIT | Trigger bit. Set when the trigger occurs, and prevents the trigger from being output until the ETM is next programmed. |
| 2 | TRACE_STATUS | Holds the current status of the trace start/stop resource. If set to 1, it indicates that a trace on address has been matched, without a corresponding trace off address match. |
| 1 | PROG_BIT | The current effective value of the ETM Programming bit (ETM Control Register bit [10]). You must wait for this bit to go to 1 before you start to program the ETM. If you read other bits in the ETM Status Register while this bit is 0, some instructions might not have taken effect. It is recommended that you set the ETM Programming bit and wait for this bit to go to 1 before reading the overflow bit. In ETMv3.2 and later this bit remains 0 if there is any data in the FIFO. This ensures that the FIFO is empty before the ETM programming is changed. |
| 0 | OVERFLOW_FLAG | If set to 1, there is an overflow that has not yet been traced. This bit is cleared to 0 when either: o trace is restarted. o the ETM Power Down bit, bit [0] of the ETM Control Register, 0x00, is set to 1. |

1.3.1629 ETM_SYS_CFG

System Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_SYS_CFG: 0xE0041014

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|--------------|---|---|
| SW Access:Reset | NA:0000 | | | | R:1 | R:001 | | |
| HW Access | NA | | | | R | R | | |
| Name | | | | | RESERVED | MAX_PRT_SIZE | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|--------------|-------|----|----|------------------|------------------|---------------|------------------|
| SW Access:Reset | NA:0 | R:000 | | | R:1 | R:1 | R:0 | R:1 |
| HW Access | NA | R | | | R | R | R | R |
| Name | CORE_SUPPORT | | | | PRT_MODE_SUPPORT | PRT_SIZE_SUPPORT | MAX_PRT_SIZE3 | FIFOFULL_SUPPORT |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-----------|----|----|----|----|----|--------------|------|
| SW Access:Reset | NA:000000 | | | | | | R:1 | NA:0 |
| HW Access | NA | | | | | | R | NA |
| Name | | | | | | | NO_FETCH_CMP | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The System Configuration Register shows the ETM features supported by the ASIC. The contents of this register are based on inputs provided by the ASIC.

| Bits | Name | Description |
|-------|-------------------|---|
| 17 | NO_FETCH_CMP | No Fetch comparisons. The value of this bit is 1, indicating that fetch comparisons are not implemented. |
| 14:12 | CORE_SUPPORT[2:0] | Number of supported cores minus 1. The value given here is the maximum value that can be written to bits [27:25] of the ETM Control Register, 0x00. These bits must be b000 if JTAG access is supported. |
| 11 | PRT_MODE_SUPPORT | Port mode supported. Set to 1 if the currently selected port mode is supported internally or externally. |
| 10 | PRT_SIZE_SUPPORT | Port size supported. Set to 1 if the currently selected port size is supported internally or externally for the currently selected port mode. Enables more complex port sizes to be supported. |
| 9 | MAX_PRT_SIZE3 | Maximum port size[3]. This bit is used in conjunction with bits [2:0]. Its value is 0. This has no effect on the TPIU trace port. |

1.3.1629 ETM_SYS_CFG (continued)

| | | |
|-----|-------------------|--|
| 8 | FIFOFULL_SUPPORT | If set to 1, FIFOFULL is supported. This bit is used in conjunction with bit [23] of the ETM Configuration Register. |
| 3 | RESERVED | Reserved, but reads as 1 |
| 2:0 | MAX_PRT_SIZE[2:0] | Maximum port size[2:0]. This bit is used in conjunction with bit [9]. The value given here is the maximum size supported by both the ETM and the ASIC. Smaller sizes might or might not be supported. Check bit [10] for precise details of supported modes. |

1.3.1630 ETM_TRACE_ENB_EVENT

Trace Enable Event Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_TRACE_ENB_EVENT: 0xE0041020

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|-----------|---|---|---|---|---|---|
| SW Access:Reset | W:0 | W:0000000 | | | | | | |
| HW Access | R | R | | | | | | |
| Name | RSRC_B | RSRC_A | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------|----|-----------|----|----|----|---|---|
| SW Access:Reset | W:00 | | W:0000000 | | | | | |
| HW Access | R | | R | | | | | |
| Name | FCN | | RSRC_B | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|-----|
| SW Access:Reset | NA:0000000 | | | | | | | W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | FCN |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The TraceEnable Event Register defines the TraceEnable enabling event.

| Bits | Name | Description |
|-------|-------------|-------------|
| 16:14 | FCN[2:0] | Fcn. |
| 13:7 | RSRC_B[6:0] | Resource B. |
| 6:0 | RSRC_A[6:0] | Resource A. |

1.3.1631 ETM_TRACE_EN_CTRL1

TraceEnable Control 1 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_TRACE_EN_CTRL1: 0xE0041024

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-------------------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:0000000 | | | | | | W:0 | NA:0 |
| HW Access | NA | | | | | | R | NA |
| Name | | | | | | | TRACE_CT RL_EN | |

The TraceEnable Control 1 Register enables the start/stop logic used for trace enable

| Bits | Name | Description |
|------|---------------|--|
| 25 | TRACE_CTRL_EN | Trace start/stop enable. The possible values of this bit are: 0 Tracing is unaffected by the trace start/stop logic. 1 Tracing is controlled by the trace on and off addresses configured for the trace start/stop logic. The trace start/stop resource, resource 0x5F, is unaffected by the value of this bit. |

1.3.1632 ETM_FIFOFULL_LEVEL

FIFOFULL Level Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_FIFOFULL_LEVEL: 0xE004102C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------|---|---|-----------|---|---|---|---|
| SW Access:Reset | NA:000 | | | R/W:00000 | | | | |
| HW Access | NA | | | R | | | | |
| Name | FIFOFULL_LVL | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The FIFOFULL Level Register holds the level below which the FIFO is considered full, although its function varies for different ETM architectures. From ETMv3.0 the value in this register also controls the point at which data trace suppression occurs.

| Bits | Name | Description |
|------|-------------------|---|
| 4:0 | FIFOFULL_LVL[4:0] | The number of bytes left in the FIFO, below which the FIFOFULL or SuppressData signal is asserted. For example, setting this value to 15 causes data trace suppression or processor stalling, if enabled, when there are less than 15 free bytes in the FIFO. |

1.3.1633 ETM_SYNC_FREQ

Synchronization Frequency Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_SYNC_FREQ: 0xE00411E0

| | | | | | | | | |
|-----------------|---------------|-----------|-----------|-----------|---------------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | SyncFrequency | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:0000 | | | | R:0100 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | SyncFrequency | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Synchronization Frequency Register holds the trace synchronization frequency value.

| Bits | Name | Description |
|------|---------------------|--|
| 11:0 | SyncFrequency[11:0] | Synchronization frequency (default = 1024) |

1.3.1634 ETM_ETM_ID

ETM ID Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_ETM_ID: 0xE00411E4

| | | | | | | | | |
|-----------------|-----------------|-----------|-----------|-----------|-----------------|----------------|-----------|------------------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:0101 | | | | R:0011 | | | |
| HW Access | R | | | | R | | | |
| Name | MinorETMArchVer | | | | ImplRev | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:1111 | | | | R:0010 | | | |
| HW Access | R | | | | R | | | |
| Name | CoreFam | | | | MajorETMArchVer | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:000 | | | R:1 | R:0 | R:1 | NA:0 | R:0 |
| HW Access | NA | | | R | R | R | NA | R |
| Name | | | | BrPcktEnc | TrustZone-Supp | Thumb2Sup p | | LoadPC- First |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R:01000001 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ImplCode | | | | | | | |

The ETM ID Register holds the ETM architecture variant, and precisely defines the programmer's model for the ETM.

| Bits | Name | Description |
|-------|---------------|--|
| 31:24 | ImplCode[7:0] | Implementor code. The following code is defined, all other values are reserved by ARM Limited: 0x41 = A (ARM Limited). |
| 20 | BrPcktEnc | Branch packet encoding implemented: If this bit is not set (b0), the ETM implements the original branch packet encoding. If this bit is set (b1), the ETM implements the alternative branch packet encoding. |
| 19 | TrustZoneSupp | TrustZone support. If this bit is not set (b0), then the ETM behaves as if the processor is in secure state at all times. If this bit is set (b1), the TrustZone architectural extensions are supported by the processor. |
| 18 | Thumb2Supp | Thumb-2 support. If this bit is not set (b0), BL and BLX immediate are traced as two instructions. Exceptions might occur between these instructions. If this bit is set (b1), the Thumb-2 architectural extensions are supported by the processor. Thumb 32-bit BL/BLX instructions are traced as one instruction. |

1.3.1634 ETM_ETM_ID (continued)

| | | |
|-------|----------------------|--|
| 16 | LoadPCFirst | <p>Load pc first. If this bit is set to b1, LSMs with the pc in the list load the pc first, followed by the other registers in the normal order. This can be decompressed by using the following procedure:</p> <ol style="list-style-type: none"> 1. Calculate the number of items transferred by the LSM by looking at the code image. 2. As each item is read, assign an address equal to 4 greater than the previous one as normal. 3. When the number of items read equals the total number of items transferred, subtract (4 * number of items) from each address other than the first. |
| 15:12 | CoreFam[3:0] | <p>Core family. The meaning of this field depends on the value of the Implementor Code. The following apply if Implementor code = A (ARM Limited), and are the only values that are defined. All other values are reserved by ARM Limited:</p> <ul style="list-style-type: none"> b0000 = ARM7 core b0001 = ARM9 core b0010 = ARM10 core b0011 = ARM11 core b1111 = Defined elsewhere The value of these bits is 0b1111, indicating that the processor family is not identified in this register. |
| 11:8 | MajorETMArchVer[3:0] | <p>Major ETM architecture version number, see The ETM architecture version:</p> <ul style="list-style-type: none"> b0000 = ETMv1 b0001 = ETMv2 b0010 = ETMv3 |
| 7:4 | MinorETMArchVer[3:0] | Minor ETM architecture version number |
| 3:0 | ImplRev[3:0] | Implementation revision. |

1.3.1635 ETM_CFG_CODE_EXT

Configuration Code Extension Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CFG_CODE_EXT: 0xE00411E8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|-------------|---|---|
| SW Access:Reset | R:00000 | | | | | R:000 | | |
| HW Access | R | | | | | R | | |
| Name | SzExtInBus | | | | | NumExtInSel | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|----------|----|----|---------------|--------------|------------|---|---|
| SW Access:Reset | R:000 | | | R:1 | R:1 | R:000 | | |
| HW Access | R | | | R | R | R | | |
| Name | NumInstr | | | DataAddr-Supp | RegRead-able | SzExtInBus | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------|------------------|---------------|------------|-----------|----|----|----|
| SW Access:Reset | NA:0 | R:1 | R:0 | R:1 | R:0100 | | | |
| HW Access | NA | R | R | R | R | | | |
| Name | | TimestampingImpl | EmbICEBehCtrl | TraceSSBlk | NumEmbICE | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------|----|--------------|---------------|------------|--------|----|----|
| SW Access:Reset | NA:00 | | R:0 | R:1 | R:1 | NA:000 | | |
| HW Access | NA | | R | R | R | NA | | |
| Name | | | Times-tampSz | Times-tampEnc | RedFuncCtr | | | |

The Configuration Code Extension Register holds additional bits for ETM configuration code. This register describes the extended external inputs.

| Bits | Name | Description |
|------|------------------|---|
| 29 | TimestampSz | Timestamp size. Set to 0 to indicate a size of 48 bits. |
| 28 | TimestampEnc | Timestamp encoding. Set to 1 to indicate that the timestamp is encoded as a natural binary number. |
| 27 | RedFuncCtr | Reduced function counter. Set to 1 to indicate that Counter 1 is a reduced function counter. |
| 22 | TimestampingImpl | This bit is set to 1, indicating that timestamping is implemented. |
| 21 | EmbICEBehCtrl | EmbeddedICE Behavior Control Register implemented. This bit is b1 if the register is implemented, and b0 if it is not implemented. |
| 20 | TraceSSBlk | Trace Start/Stop block can use EmbeddedICE watchpoint inputs. This bit is b1 if the Trace Start/Stop block can use these inputs, and is b0 otherwise. |

1.3.1635 ETM_CFG_CODE_EXT (continued)

| | | |
|-------|------------------|--|
| 19:16 | NumEmbICE[3:0] | Number of EmbeddedICE watchpoint inputs implemented. This field can take any value from b0000 (0 inputs) to b1000 (8 inputs). |
| 15:13 | NumInstr[2:0] | Number of Instrumentation resources supported. The maximum value of this field is b100, for four Instrumentation resources. |
| 12 | DataAddrSupp | Set to b1 if data address comparisons are not supported. |
| 11 | RegReadable | Set to b1 if all registers are readable. |
| 10:3 | SzExtInBus[7:0] | Size of extended external input bus. This field must be 0 if bits [2:0] are 0. |
| 2:0 | NumExtInSel[2:0] | Number of extended external input selectors. |

1.3.1636 ETM_TR_SS_EMBICE_CTRL

Trace Start/Stop EmbeddedICE Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_TR_SS_EMBICE_CTRL: 0xE00411F0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|------------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | StrtResSel | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|---------|----|----|----|-----------|----|----|----|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | StpResSel | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Trace Start/Stop EmbeddedICE Control Register specifies the EmbeddedICE watchpoint comparator inputs that are used as trace start and stop resources.

| Bits | Name | Description |
|-------|-----------------|---|
| 19:16 | StpResSel[3:0] | Stop resource selection. Setting a bit in this field to b1 selects the corresponding EmbeddedICE watchpoint input as a TraceEnable stop resource. Bit [16] corresponds to input 1, bit [17] to input 2, and this pattern continues up to bit [19] corresponding to input 4. |
| 3:0 | StrtResSel[3:0] | Start resource selection. Setting a bit in this field to b1 selects the corresponding EmbeddedICE watchpoint input as a TraceEnable start resource. Bit [0] corresponds to input 1, bit [1] to input 2, and this pattern continues up to bit [3] corresponding to input 4. |

1.3.1637 ETM_CS_TRACE_ID

CoreSight Trace ID Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CS_TRACE_ID: 0xE0041200

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------|-------------|---|---|---|---|---|---|
| SW Access:Reset | NA:0 | R/W:0000000 | | | | | | |
| HW Access | NA | R | | | | | | |
| Name | | TraceID | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The CoreSight Trace ID Register defines the 7-bit Trace ID, for output to the trace bus.

| Bits | Name | Description |
|------|--------------|--|
| 6:0 | TraceID[6:0] | Trace ID to output onto the trace bus. At reset this register is 0x00. |

1.3.1638 ETM_OS_LOCK_ACCESS

OS Lock Access Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_OS_LOCK_ACCESS: 0xE0041300

| | | | | | | | | |
|-----------------|--------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | LOCK_UNLOCK_ACCESS | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | LOCK_UNLOCK_ACCESS | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | LOCK_UNLOCK_ACCESS | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | LOCK_UNLOCK_ACCESS | | | | | | | |

The OS Lock Access Register (OSLAR) is used to lock and unlock access to ETM debug registers.

| Bits | Name | Description |
|------|------------------------------|--|
| 31:0 | LOCK_UNLOCK_ACCES S[31:0] | Write 0xC5ACCE55 to this field to lock the ETM debug registers. Write any other value to this field to unlock the ETM debug registers. |

1.3.1639 ETM_OS_LOCK_STATUS

OS Lock Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_OS_LOCK_STATUS: 0xE0041304

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | NA:00000 | | | | | R:1 | R:0 | R:0 |
| HW Access | NA | | | | | W | W | W |
| Name | | | | | | Access32 | Locked | LockImpl |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The OS Lock Status Register (OSLSR) is used to find whether the ETM debug registers are locked. It can also be used to find whether ETM debug register locking is implemented on your ETM macrocell.

| Bits | Name | Description |
|------|----------|---|
| 2 | Access32 | 32-bit access bit. If ETM debug register locking is implemented then this bit is set (b1), to indicate that 32-bit access is required to write to the OS Lock Access Register to lock the ETM debug registers. |
| 1 | Locked | Locked bit: b0: ETM debug registers are not locked. b1: ETM debug registers are locked. Any access to these registers returns a slave-generated error response. The reset value of this field corresponds to the value on the DBGOSLOCKINIT pin. |
| 0 | LockImpl | ETM debug register locking implemented: b0: OS Lock and OS Save/Restore registers are not implemented. In this case, bits [31:0] of the OS Lock Status register reads as zero. b1: OS Lock and OS Save/Restore registers are implemented and it is possible to set the OS Lock for this macrocell, to lock the ETM debug registers. The reset value of this field is Implementation-defined. |

1.3.1640 ETM_PDSR

Device Power-Down Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PDSR: 0xE0041314

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | NA:0000000 | | | | | | | R:1 |
| HW Access | NA | | | | | | | W |
| Name | | | | | | | | ETMPow- ered |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Indicates the power-down status of the ETM.

| Bits | Name | Description |
|------|------------|---|
| 0 | ETMPowered | ETM powered up. The value of this bit indicates whether you can access the ETM Trace Registers. The value of this bit is always 1, indicating that the ETM Trace Registers can be accessed. |

1.3.1641 ETM_ITMISCIN

Integration Test Miscellaneous Inputs

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_ITMISCIN: 0xE0041EE0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|----------|-------|---|-------|---|
| SW Access:Reset | NA:000 | | | R:0 | NA:00 | | R:00 | |
| HW Access | NA | | | W | NA | | W | |
| Name | | | | COREHALT | | | EXTIN | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Integration test.

| Bits | Name | Description |
|------|------------|--|
| 4 | COREHALT | A read of this bit returns the value of the COREHALT input pin. |
| 1:0 | EXTIN[1:0] | A read of these bits returns the value of the EXTIN[1:0] input pins. |

1.3.1642 ETM_ITTRIGOUT

Integration Test Trigger Out

Reset: N/A

Register : Address

ETM_ITTRIGOUT: 0xE0041EE8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---------|
| SW Access:Reset | NA:0000000 | | | | | | | W:U |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | TRIGGER |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Integration test. You must set bit [0] of ETMITCTRL to use this register.

| Bits | Name | Description |
|------|---------|--|
| 0 | TRIGGER | TRIGGER output value. A write to this bit sets the TRIGGER output. |

1.3.1643 ETM_ITATBCTR2

ETM Integration Test ATB Control 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_ITATBCTR2: 0xE0041EF0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---------|
| SW Access:Reset | NA:0000000 | | | | | | | R:1 |
| HW Access | NA | | | | | | | W |
| Name | | | | | | | | ATREADY |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:0000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:0000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:0000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Integration test. You must set bit [0] of ETMITCTRL to use this register.

| Bits | Name | Description |
|------|---------|---|
| 0 | ATREADY | ATREADY input value. A read of this bit returns the value of the ETM ATREADY input. |

1.3.1644 ETM_ITATBCTR0

ETM Integration Test ATB Control 0

Reset: N/A

Register : Address

ETM_ITATBCTR0: 0xE0041EF8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---------|
| SW Access:Reset | NA:0000000 | | | | | | | W:U |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | ATVALID |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

Integration test. You must set bit [0] of ETMITCTRL to use this register.

| Bits | Name | Description |
|------|---------|---|
| 0 | ATVALID | ATVALID output value. A write to this bit sets the value of the ETM ATVALID output. |

1.3.1645 ETM_INT_MODE_CTRL

Integration Mode Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_INT_MODE_CTRL: 0xE0041F00

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|-----------|
| SW Access:Reset | NA:0000000 | | | | | | | R/W:0 |
| HW Access | NA | | | | | | | R |
| Name | | | | | | | | EnIntTest |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Integration Mode Control Register is used to enable topology detection or to check integration testing.

| Bits | Name | Description |
|------|-----------|---|
| 0 | EnIntTest | When set to b1, the device goes into an integration mode to enable Topology Detection or Integration Testing to be checked. At reset this bit is b0. |

1.3.1646 ETM_CLM_TAG_SET

Claim Tag Set Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CLM_TAG_SET: 0xE0041FA0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|-------------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:1111 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | ClaimTagSet | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Claim Tag Set Register is used to set bits in the claim tag and find the number of bits supported by the claim tag.

| Bits | Name | Description |
|------|------------------|---|
| 3:0 | ClaimTagSet[3:0] | On reads, returns 0xF. On writes, a 1 in a bit position causes the corresponding bit in the claim tag value to be set. |

1.3.1647 ETM_CLM_TAG_CLR

Claim Tag Clear Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CLM_TAG_CLR: 0xE0041FA4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|---------------|---|---|---|
| SW Access:Reset | NA:0000 | | | | R/W:0000 | | | |
| HW Access | NA | | | | R | | | |
| Name | | | | | ClaimTagClear | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Claim Tag Clear Register is used to clear bits in the claim tag to b0, and to find the current value of the claim tag.

| Bits | Name | Description |
|------|--------------------|---|
| 3:0 | ClaimTagClear[3:0] | On reads, returns the current claim tag value. On writes, a 1 in a bit position causes the corresponding bit in the claim tag value to be cleared to b0. |

1.3.1648 ETM_LOCK_ACCESS

Lock Access Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_LOCK_ACCESS: 0xE0041FB0

| | | | | | | | | |
|-----------------|--------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | LOCK_UNLOCK_ACCESS | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | LOCK_UNLOCK_ACCESS | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | LOCK_UNLOCK_ACCESS | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | W:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | LOCK_UNLOCK_ACCESS | | | | | | | |

The Lock Access Register (LAR or LOCKACCESS) is used to lock and unlock access to all other ETM registers.

| Bits | Name | Description |
|------|------------------------------|---|
| 31:0 | LOCK_UNLOCK_ACCES S[31:0] | A write of 0xC5ACCE55 unlocks the ETM. A write of any other value locks the ETM. Writes to this register from an interface that ignores the lock registers are ignored. |

1.3.1649 ETM_LOCK_STATUS

Lock Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_LOCK_STATUS: 0xE0041FB4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|---|----------|--------|----------|
| SW Access:Reset | NA:00000 | | | | | R:0 | R:0 | R:0 |
| HW Access | NA | | | | | W | W | W |
| Name | | | | | | Access32 | Locked | LockImpl |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Lock Status Register has two uses: - If you read this register from any interface, you can check bit [0] to find out whether the lock registers are implemented for the interface you are using. - If you read this register from an interface for which lock registers are implemented, you can check bit [1] to find out whether the registers are currently locked.

| Bits | Name | Description |
|------|----------|--|
| 2 | Access32 | Reads as b0. Indicates that the Lock Access Register is 32 bits. |
| 1 | Locked | Indicates if the ETM is locked: b1: Writes are ignored b0: Writes are permitted. If this register is accessed from an interface where the lock registers are ignored, this field reads as b0 regardless of whether the ETM is locked. |
| 0 | LockImpl | Indicates if the lock registers are implemented for this interface: b1: This access is from an interface that requires the ETM to be unlocked b0: This access is from an interface that ignores the lock registers. |

1.3.1650 ETM_AUTH_STATUS

Authentication Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_AUTH_STATUS: 0xE0041FB8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|----------|---|--------------|---|-----------|---|
| SW Access:Reset | R:11 | | R:00 | | R:00 | | R:00 | |
| HW Access | W | | W | | R | | W | |
| Name | NonInvSupp | | SInvSupp | | NSNonInvSupp | | NSInvSupp | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Authentication Status Register reports the level of tracing currently permitted by the authentication signals provided to the ETM.

| Bits | Name | Description |
|------|-------------------|---|
| 7:6 | NonInvSupp[1:0] | Reads as b11: Permission for secure non-invasive debug is supported by the ETM. |
| 5:4 | SInvSupp[1:0] | Reads as b00: Secure invasive debug not supported by the ETM. |
| 3:2 | NSNonInvSupp[1:0] | Permission for Non-secure non-invasive debug. This field is only implemented if the processor core implemented with the ETM supports the TrustZone security extensions. When this field is implemented the permitted values are: b10: Non-secure non-invasive debug disabled b11: Non-secure non-invasive debug enabled. This field is a logical OR of the NIDEN and DBGEN signals. It takes the value b11 when the OR is TRUE, and b10 when the OR is FALSE. If the core does not support the TrustZone extensions, bits [3:2] are reserved, read as b00. |
| 1:0 | NSInvSupp[1:0] | Reads as b00: Non-secure invasive debug not supported by the ETM. |

1.3.1651 ETM_DEV_TYPE

Device Type Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_DEV_TYPE: 0xE0041FCC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|---|---|---|----------|---|---|---|
| SW Access:Reset | R:0001 | | | | R:0011 | | | |
| HW Access | R | | | | R | | | |
| Name | SubType | | | | MainType | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

The Device Type Register returns the CoreSight device type of the component.

| Bits | Name | Description |
|------|---------------|--------------------------------|
| 7:4 | SubType[3:0] | 0x1 Sub type, processor trace. |
| 3:0 | MainType[3:0] | 0x3 Main type, trace source. |

1.3.1652 ETM_PID4

ETM Peripheral Identification Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID4: 0xE0041FD0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000100 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID4 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Peripheral Identification Register 4

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID4[7:0] | Peripheral Identification Register 4 |

1.3.1653 ETM_PID5

ETM Peripheral Identification Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID5: 0xE0041FD4

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID5 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Peripheral Identification Register 5

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID5[7:0] | Peripheral Identification Register 5 |

1.3.1654 ETM_PID6

ETM Peripheral Identification Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID6: 0xE0041FD8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID6 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Peripheral Identification Register 6

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID6[7:0] | Peripheral Identification Register 6 |

1.3.1655 ETM_PID7

ETM Peripheral Identification Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID7: 0xE0041FDC

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID7 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Peripheral Identification Register 7

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID7[7:0] | Peripheral Identification Register 7 |

1.3.1656 ETM_PID0

ETM Peripheral Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID0: 0xE0041FE0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00100100 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Peripheral Identification Register 0

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID0[7:0] | Peripheral Identification Register 0 |

1.3.1657 ETM_PID1

ETM Peripheral Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID1: 0xE0041FE4

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:10111001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID1 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Peripheral Identification Register 1

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID1[7:0] | Peripheral Identification Register 1 |

1.3.1658 ETM_PID2

ETM Peripheral Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID2: 0xE0041FE8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00111011 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID2 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Peripheral Identification Register 2

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID2[7:0] | Peripheral Identification Register 2 |

1.3.1659 ETM_PID3

ETM Peripheral Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID3: 0xE0041FEC

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID3 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Peripheral Identification Register 3

| Bits | Name | Description |
|------|-----------|--------------------------------------|
| 7:0 | PID3[7:0] | Peripheral Identification Register 3 |

1.3.1660 ETM_CID0

ETM Component Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CID0: 0xE0041FF0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00001101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Component Identification Register 0

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID0[7:0] | Component Identification Register 0 |

1.3.1661 ETM_CID1

ETM Component Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CID1: 0xE0041FF4

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:10010000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID1 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Component Identification Register 1

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID1[7:0] | Component Identification Register 1 |

1.3.1662 ETM_CID2

ETM Component Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CID2: 0xE0041FF8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID2 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|-------------|----|----|----|----|----|---|---|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|-------------|----|----|----|----|----|----|----|
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Component Identification Register 2

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID2[7:0] | Component Identification Register 2 |

1.3.1663 ETM_CID3

ETM Component Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CID3: 0xE0041FFC

| | | | | | | | | |
|-----------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:10110001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID3 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | NA:00000000 | | | | | | | |
| HW Access | NA | | | | | | | |
| Name | | | | | | | | |

ETM Component Identification Register 3

| Bits | Name | Description |
|------|-----------|-------------------------------------|
| 7:0 | CID3[7:0] | Component Identification Register 3 |

1.3.1664 ROM_TABLE_NVIC

NVIC

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_NVIC: 0xE00FF000

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000011 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | NVIC | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:11110000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | NVIC | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:11110000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | NVIC | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:11111111 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | NVIC | | | | | | | |

(no description)

| Bits | Name | Description |
|------|------------|-----------------------------------|
| 31:0 | NVIC[31:0] | Points to the NVIC at 0xE000E000. |

1.3.1665 ROM_TABLE_DWT

DWT

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_DWT: 0xE00FF004

| | | | | | | | | |
|-----------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000011 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DWT | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:00100000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DWT | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:11110000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DWT | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R:11111111 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | DWT | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|--|
| 31:0 | DWT[31:0] | DWT Points to the Data Watchpoint and Trace block at 0xE0001000. |

1.3.1666 ROM_TABLE_FPB

FPB

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_FPB: 0xE00FF008

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000011 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | FPB | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00110000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | FPB | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:11110000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | FPB | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:11111111 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | FPB | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---|
| 31:0 | FPB[31:0] | FPB Points to the Flash Patch and Breakpoint block at 0xE0002000. |

1.3.1667 ROM_TABLE_ITM

ITM

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_ITM: 0xE00FF00C

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000011 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ITM | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00010000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ITM | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:11110000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ITM | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:11111111 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ITM | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|--|
| 31:0 | ITM[31:0] | Points to the Instrumentation Trace block at 0xE0000000. |

1.3.1668 ROM_TABLE_TPIU

TPIU

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_TPIU: 0xE00FF010

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000011 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | TPIU | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00010000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | TPIU | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:11110100 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | TPIU | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:11111111 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | TPIU | | | | | | | |

(no description)

| Bits | Name | Description |
|------|------------|---|
| 31:0 | TPIU[31:0] | Points to the TPIU. Value has bit [0] set to 1 if TPIU is fitted. TPIU is at 0xE0040000 |

1.3.1669 ROM_TABLE_ETM

ETM

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_ETM: 0xE00FF014

| | | | | | | | | |
|-----------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000011 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ETM | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:00100000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ETM | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:11110100 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ETM | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R:11111111 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | ETM | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---|
| 31:0 | ETM[31:0] | Points to the ETM. Value has bit [0] set to 1 if ETM is fitted. ETM is at 0xE0041000. |

1.3.1670 ROM_TABLE_END

END

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_END: 0xE00FF018

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | END | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | END | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | END | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | END | | | | | | | |

(no description)

| Bits | Name | Description |
|------|-----------|---|
| 31:0 | END[31:0] | Marks the end of the ROM table. If CoreSight components are added, they are added starting from this location and the End marker is moved to the next location after the additional components. |

1.3.1671 ROM_TABLE_MEMTYPE

MEMTYPE

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_MEMTYPE: 0xE00FFFC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000001 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | MEMTYPE | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | MEMTYPE | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | MEMTYPE | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R | | | | | | | |
| Name | MEMTYPE | | | | | | | |

(no description)

| Bits | Name | Description |
|------|---------------|--|
| 31:0 | MEMTYPE[31:0] | Bits [31:1] RAZ. Bit [0] is set when the system memory map is accessible using the DAP. Bit [0] is clear when only debug resources are accessible using the DAP. |

1.3.1672 ROM_TABLE_PID4

ROM Table Peripheral Identification Register 4

Reset: Reset Signals Listed Below

Register : Address

ROM_TABLE_PID4: 0xE00FFD0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|---|---|---|-------------|---|---|---|
| SW Access:Reset | R:0000 | | | | W:UUUU | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | PID4 | | | | jep106_id_2 | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID4 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID4 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID4 | | | | | | | |

ROM Table Peripheral Identification Register 4

| Bits | Name | Description |
|------|------------------|---|
| 31:4 | PID4[27:0] | Peripheral Identification Register 4 |
| 3:0 | jep106_id_2[3:0] | Peripheral Identification Register 4 - JEP106 continuation code |

Reset Table

| resetsignal | field(s) |
|---|------------------|
| N/A | jep106_id_2[3:0] |
| System reset for retention flops [reset_all_retention] | PID4[27:0] |

1.3.1673 ROM_TABLE_PID5

ROM Table Peripheral Identification Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID5: 0xE00FFFD4

| | | | | | | | | |
|-----------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID5 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID5 | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID5 | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID5 | | | | | | | |

ROM Table Peripheral Identification Register 5

| Bits | Name | Description |
|------|------------|--------------------------------------|
| 31:0 | PID5[31:0] | Peripheral Identification Register 5 |

1.3.1674 ROM_TABLE_PID6

ROM Table Peripheral Identification Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID6: 0xE00FFD8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID6 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID6 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID6 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID6 | | | | | | | |

ROM Table Peripheral Identification Register 6

| Bits | Name | Description |
|------|------------|--------------------------------------|
| 31:0 | PID6[31:0] | Peripheral Identification Register 6 |

1.3.1675 ROM_TABLE_PID7

ROM Table Peripheral Identification Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID7: 0xE00FFDC

| | | | | | | | | |
|-----------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID7 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID7 | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID7 | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID7 | | | | | | | |

ROM Table Peripheral Identification Register 7

| Bits | Name | Description |
|------|------------|--------------------------------------|
| 31:0 | PID7[31:0] | Peripheral Identification Register 7 |

1.3.1676 ROM_TABLE_PID0

ROM Table Peripheral Identification Register 0

Reset: Reset Signals Listed Below

Register : Address

ROM_TABLE_PID0: 0xE00FFE0

| | | | | | | | | |
|-----------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW Access:Reset | W:UUUUUUUU | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | part_num_0 | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID0 | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID0 | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID0 | | | | | | | |

ROM Table Peripheral Identification Register 0

| Bits | Name | Description |
|------|-----------------|--|
| 31:8 | PID0[23:0] | Peripheral Identification Register 0 |
| 7:0 | part_num_0[7:0] | Peripheral Identification Register 0 - Part Number [7:0] |

Reset Table

| resetsignal | field(s) |
|--|-----------------|
| N/A | part_num_0[7:0] |
| System reset for retention flops [reset_all_retention] | PID0[23:0] |

1.3.1677 ROM_TABLE_PID1

ROM Table Peripheral Identification Register 1

Reset: Reset Signals Listed Below

Register : Address

ROM_TABLE_PID1: 0xE00FFE4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|---|---|---|------------|---|---|---|
| SW Access:Reset | W:UUUU | | | | W:UUUU | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | jep106_id_0 | | | | part_num_1 | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID1 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID1 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID1 | | | | | | | |

ROM Table Peripheral Identification Register 1

| Bits | Name | Description |
|------|------------------|---|
| 31:8 | PID1[23:0] | Peripheral Identification Register 1 |
| 7:4 | jep106_id_0[3:0] | Peripheral Identification Register 1 - JEP106 identity code [3:0] |
| 3:0 | part_num_1[3:0] | Peripheral Identification Register 1 - Part Number [11:8] |

Reset Table

| resetsignal | field(s) |
|---|--------------------------------------|
| N/A | part_num_1[3:0], jep106_id_0[3:0] |
| System reset for retention flops [reset_all_retention] | PID1[23:0] |

1.3.1678 ROM_TABLE_PID2

ROM Table Peripheral Identification Register 2

Reset: Reset Signals Listed Below

Register : Address

ROM_TABLE_PID2: 0xE00FFE8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|---|---|---|------------|-------------|---|---|
| SW Access:Reset | W:UUUU | | | | W:1 | W:UUU | | |
| HW Access | R/W | | | | R/W | R/W | | |
| Name | revision | | | | always_set | jep106_id_1 | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID2 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID2 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID2 | | | | | | | |

ROM Table Peripheral Identification Register 2

| Bits | Name | Description |
|------|------------------|--|
| 31:8 | PID2[23:0] | Peripheral Identification Register 2 |
| 7:4 | revision[3:0] | Peripheral Identification Register 2 - Revision |
| 3 | always_set | Peripheral Identification Register 2 - Always set. Indicates that a JEDEC assigned value is used |
| 2:0 | jep106_id_1[2:0] | Peripheral Identification Register 2 - JEP106 identity code [6:4] |

Reset Table

| resetsignal | field(s) |
|--|---------------------------------|
| N/A | jep106_id_1[2:0], revision[3:0] |
| System reset for retention flops [reset_all_retention] | always_set, PID2[23:0] |

1.3.1679 ROM_TABLE_PID3

ROM Table Peripheral Identification Register 3

Reset: Reset Signals Listed Below

Register : Address

ROM_TABLE_PID3: 0xE00FFEC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|----------|---|---|---|
| SW Access:Reset | W:UUUU | | | | R:0000 | | | |
| HW Access | R/W | | | | R/W | | | |
| Name | part_num_2 | | | | cust_mod | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID3 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID3 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | PID3 | | | | | | | |

ROM Table Peripheral Identification Register 3

| Bits | Name | Description |
|------|-----------------|--|
| 31:8 | PID3[23:0] | Peripheral Identification Register 3 |
| 7:4 | part_num_2[3:0] | Peripheral Identification Register 3 - RevAnd equals Part Number [15:12] |
| 3:0 | cust_mod[3:0] | Peripheral Identification Register 3 - Customer Modified |

Reset Table

| resetsignal | field(s) |
|--|------------------------------|
| N/A | part_num_2[3:0] |
| System reset for retention flops [reset_all_retention] | cust_mod[3:0], PID3[23:0] |

1.3.1680 ROM_TABLE_CID0

ROM Table Component Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_CID0: 0xE00FFFF0

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00001101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID0 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID0 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID0 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID0 | | | | | | | |

ROM Table Component Identification Register 0

| Bits | Name | Description |
|------|------------|-------------------------------------|
| 31:0 | CID0[31:0] | Component Identification Register 0 |

1.3.1681 ROM_TABLE_CID1

ROM Table Component Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_CID1: 0xE00FFFF4

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00010000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID1 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID1 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID1 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID1 | | | | | | | |

ROM Table Component Identification Register 1

| Bits | Name | Description |
|------|------------|-------------------------------------|
| 31:0 | CID1[31:0] | Component Identification Register 1 |

1.3.1682 ROM_TABLE_CID2

ROM Table Component Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_CID2: 0xE00FFFF8

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:00000101 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID2 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID2 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID2 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID2 | | | | | | | |

ROM Table Component Identification Register 2

| Bits | Name | Description |
|------|------------|-------------------------------------|
| 31:0 | CID2[31:0] | Component Identification Register 2 |

1.3.1683 ROM_TABLE_CID3

ROM Table Component Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_CID3: 0xE00FFFC

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------|---|---|---|---|---|---|---|
| SW Access:Reset | R:10110001 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID3 | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------------|------------|----|----|----|----|----|---|---|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID3 | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID3 | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------|------------|----|----|----|----|----|----|----|
| SW Access:Reset | R:00000000 | | | | | | | |
| HW Access | R/W | | | | | | | |
| Name | CID3 | | | | | | | |

ROM Table Component Identification Register 3

| Bits | Name | Description |
|------|------------|-------------------------------------|
| 31:0 | CID3[31:0] | Component Identification Register 3 |



0xe00ffc

1.3.1683 ROM_TABLE_CID3 (continued)

Revision History



Revision History

| Document Title: PSoC® 5LP REGISTERS TRM (TECHNICAL REFERENCE MANUAL) | | | | |
|---|-------------|-------------------|-------------------------|------------------------------|
| Document Number: 001-82120 | | | | |
| Revision | ECN# | Issue Date | Origin of Change | Description of Change |
| ** | 3754878 | 09/25/2012 | VVSK | Initial release |
| *A | 3818220 | 11/21/2012 | VVSK | Corrected Rev. ** ECN number |

