ECHELON®

Series 5000 Chip Data Book

005-0199-01B

Echelon Corporation
www.echelon.com

Welcome

Echelon's FT 5000 Free Topology Smart Transceiver is the successor to Echelon's FT 3120® Smart Transceiver and FT 3150® Smart Transceiver. Likewise, Echelon's Neuron® 5000 Processor is the successor to the Neuron 3120 Chip and Neuron 3150 Chip.

Combined with the Echelon high-performance FT-X3 Communications Transformer, the FT 5000 Smart Transceiver sets new benchmarks for performance, robustness, and low cost. Ideal for use in LONWORKS® devices designed for building, industrial, transportation, home, and utility automation applications, FT 5000 Smart Transceivers can be used in both new product designs and as a means of reducing costs for existing devices.

The FT 5000 Smart Transceivers includes a network transceiver that is fully compatible with the TP/FT-10 channel. The free topology transceiver supports polarity-insensitive cabling using a star, bus, daisy chain, loop, or combined topologies. This flexibility frees the installer from the need to adhere to a strict set of wiring rules. Free topology wiring reduces the time and expense of device installation by allowing the wiring to be installed in the most expeditious and cost-effective manner. It also simplifies network expansion by eliminating restrictions on wire routing, splicing, and device placement.

The Neuron 5000 Processor has similar performance, robustness, and low cost as the FT 5000 Smart Transceiver, but you can use it with a number of different types of network transceivers so that you can integrate different channel types (such as the TP/XF-1250 channel) into a LONWORKS network.

Together, the FT 5000 Smart Transceiver and the Neuron 5000 Processor are part of a family of products, collectively known as Series 5000 chips.

This document provides detailed technical specifications for the electrical interfaces, mechanical interfaces, and operating environment characteristics for the FT 5000 Smart Transceiver and Neuron 5000 Processor. In some cases, example vendor sources are included to simplify the task of integrating a Series 5000 chip with application electronics. You can find contact information for the vendor sources listed in Appendix F, *Vendor Contact Information*, on page 169.

This manual does not describe Echelon's Power Line Smart Transceivers. For more information about that technology, see the *PL 3120 / PL 3150 / PL 3170 Power Line Smart Transceiver Data Book* (005-0193-01A).

Audience

This manual provides specifications and user instructions for engineers who develop applications and devices that use FT 5000 Smart Transceivers or Neuron 5000 Processors, and for users of network interfaces based on the FT Smart Transceivers or Neuron Chips.

What's New for Echelon's Smart Transceivers and Neuron Chips

Echelon's FT 5000 Smart Transceiver and Neuron 5000 Processor include many new features and functions compared with Echelon's FT 3120 Smart Transceiver, Neuron 3120 Chip, FT 3150 Smart Transceiver, and Neuron 3150 Chip. This section describes some of the major new features and functions of the Series 5000 chips.

3.3 V Operation

Series 5000 chips operate with a 3.3 V power supply.

Series 3100 chips require a 5 V power supply.

New Memory Architecture

Series 5000 chips have a new memory architecture, for both the external memory interface and the internal on-chip memory. The external memory interface for external non-volatile memory is a serial interface using either the SPI or I²C protocol. The internal on-chip memory includes 64 KB of RAM, of which 44 KB is user-accessible. Series 5000 chips have no user-accessible on-chip ROM or flash memory. Instead, they rely on external non-volatile memory for user application code and data. The default system firmware image is contained in on-chip ROM, but newer images can be contained in the external non-volatile memory, which allows the system firmware to be upgraded as necessary.

FT 3120 Smart Transceivers and Neuron 3120 chips have no external non-volatile memory, but instead have up to 8 KB of on-chip flash memory. FT 3150 Smart Transceivers and Neuron 3150 Chips use a parallel external memory interface for external non-volatile memory. Series 3100 chips include 2 to 4 KB of RAM and 16 KB of ROM. User application code and data is loaded into the internal flash for 3120 devices and into external non-volatile memory for 3150 devices. The system firmware is contained in on-chip ROM for some Series 3100 chips.

Performance Enhancements

Series 5000 chips support an internal system clock speed of up to 80 MHz. The internal system clock speed is user-adjustable from 5 MHz to 80 MHz, based on the device's hardware template maintained by the NodeBuilder FX Development Tool or Mini FX Evaluation Kit. The external crystal frequency for all Series 5000 devices is 10 MHz.

Series 3100 chips support an internal system clock speed that is one-half of the frequency of the external crystal or oscillator. For example, an FT 3120-E4P40 Smart Transceiver has an internal system clock speed of 20 MHz based on an external input clock rate of 40 MHz. The internal system clock speed is not user-adjustable.

Interrupt Support

Series 5000 chips support hardware user interrupts in addition to the support provided through I/O models. The Neuron C language includes new keywords to manage hardware user interrupts for application programs.

Series 3100 chips do not support hardware user interrupts. However, for the Series 3100 power line chips, certain I/O models include interrupt support.

Hardware Multiply and Divide

Series 5000 chips support new Neuron assembly language instructions for multiplication and division. These instructions use hardware multiply and divide functions to provide improved performance for 8-bit multiplication and division. The older software multiplication and division system functions are still supported.

Series 3100 chips have no hardware multiply and divide functions, and rely on system software multiplication and division system functions.

Support for 254 Network Variables and 127 Aliases

Series 5000 chips use system firmware version 19, which supports up to 254 network variables and 127 aliases for Neuron hosted devices (that is, devices without a host microprocessor).

Series 3100 chips with system firmware version 15 or earlier support up to 62 network variables for Neuron hosted devices. Series 3100 chips with system firmware version 16 or later support up to 254 network variables. You must use the NodeBuilder FX Development Tool to take advantage of 254 network variables or 127 aliases.

Smaller Package

Series 5000 chips are packaged as a 7 mm by 7 mm 48-pin quad flat no leads (QFN) chip.

Series 3100 chips come in several package types, including 32-pin small-outline integrated circuit (SOIC), 44-pin thin quad flat package (TQFP), and 64-pin plastic quad flat package (PQFP).

Additional I/O Model Support

Series 5000 chips include improved hardware support for the Serial Peripheral Interface (SPI) and Serial Communication Interface (SCI) serial I/O models, which provides increased performance for devices that use these interfaces. Series 5000 chips also support all of the I/O models previously supported only by PL 3120 Smart Transceivers and PL 3150 Smart Transceivers, including the Infrared Pattern model, Magcard Bitstream model, SCI (UART) model, and SPI model. In addition, Series 5000 devices support a new I/O model, the Stretched Triac model, which improves usability and performance for triac devices.

Series 3100 free topology chips do not include hardware support for the SPI and SCI (UART) serial I/O models, although Series 3100 power line chips do provide hardware support for these I/O models.

Related Documentation

Table 1 lists related Echelon documentation that can be useful when designing or using Series 5000 chips with LONWORKS devices and LONWORKS networks. The table includes documentation for the NodeBuilder FX Development Tool and the Mini FX Evaluation Kit, the primary development tools for LONWORKS devices. It also lists related products, such as the FTXL™ transceiver and ShortStack® Micro Server, which are both host-based LONWORKS devices. All of these manuals are available from the Echelon Web site (www.echelon.com).

Table 1. Related Documentation

Title	Part Number	Description
FT 5000 EVB Hardware Guide	078-0390-01B	This manual describes the hardware for the FT 5000 EVB evaluation boards that are included with the NodeBuilder FX/FT Development Tool and the Mini FX/FT Evaluation Kit.

Title	Part Number	Description
Introduction to the LONWORKS Platform	078-0183-01B	This manual provides an introduction to the ISO/IEC 14908 (ANSI/EIA/CEA-709.1 and EN 14908) Control Networking Protocol, and provides a high-level introduction to LONWORKS® networks and the tools and components that are used for developing, installing, operating, and maintaining them.
I/O Model Reference for Smart Transceivers and Neuron Chips	078-0392-01B	This manual provides information about the I/O models used by Echelon's Neuron Chips and Smart Transceivers. It includes hardware and software considerations for each of the I/O models.
LONWORKS Host Application Programmer's Guide	078-0016-01B	This manual describes how to create LONWORKS host applications. Host applications are application programs that run on hosts other than Neuron® Chips and use the LONTALK® protocol to communicate with devices on a LONWORKS network.
Mini FX User's Guide	078-0398-01A	This manual describes how to use the Mini FX Evaluation Kit. You can use the Mini FX Evaluation Kit to develop a prototype or production control system that requires networking, or to evaluate the development of applications for control networks using the LONWORKS platform.
Neuron Assembly Language Reference	078-0399-01A	This manual describes the Neuron assembly language and how to write Neuron assembly language functions.
Neuron C Programmer's Guide	078-0002-01H	This manual describes how to write programs using the Neuron C Version 2.2 programming language.
Neuron C Reference Guide	078-0140-01F	This manual provides reference info for writing programs using the Neuron C Version 2.2 programming language.

Title	Part Number	Description
NodeBuilder FX User's Guide	078-0405-01A	This manual describes how to develop LONWORKS devices and applications using the NodeBuilder Development Tool.

For information about previous generation Smart Transceivers, see the Echelon *FT 3120 / FT 3150 Smart Transceiver Data Book*. For information about previous generation Neuron Chips, see Motorola® *LONWORKS Technology Device Data*, Toshiba *Neuron Chip TMPN3150/3120*, or Cypress™ *Neuron Chip Technical Reference Manual*.

All of the Echelon product documentation is available in Adobe® PDF format. To view the PDF files, you must have a current version of the Adobe Reader®. Most Echelon products include the English-language version of the Adobe Reader; you can download other language versions from Adobe at: www.adobe.com/products/acrobat/readstep2.html.

Standards Documents Referenced in this Manual

This manual refers to the following standards documents:

- American Society for Testing and Materials (ASTM) B258 - 02(2008) Standard Specification for Standard Nominal Diameters and Cross-Sectional Areas of AWG Sizes of Solid Round Wires Used as Electrical Conductors. www.astm.org/Standards/B258.htm
- Comité européen de normalisation electrotechnique[1] (CENELEC) EN 55022 – Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement.
- Comité international spécial des perturbations radioélectriques[2] (CISPR) 22 – Information Technology Equipment – Radio Disturbance Characteristics – Limits and Methods of Measurement.
- Electrostatic Discharge Association standard ESD STM5.1: Electrostatic Discharge Sensitivity Testing – Human Body Model. www.esda.org/freedowloads.html
- European Union Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC. europa.eu.int/eur-lex/pri/en/oj/dat/2003/l_037/l_03720030213en00190023.pdf
- Comité européen de normalisation[3] (CEN) Electromagnetic Compatibility (EMC) standards (see **Table 2** on page viii).
- International Organization for Standardization (ISO) and International Electrotechnical Commission (IEC) standard ISO/IEC 14908 Control Network Protocol
- Institute of Electrical and Electronics Engineers (IEEE) Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990). www.ieee.org/web/standards/home/index.html.

[1] European Committee for Electrotechnical Standardization

[2] International Special Committee on Radio Interference

[3] European Committee for Standardization

- Institute for Printed Circuits (IPC) / Joint Electron Device Engineering Council (JEDEC) Solid State Technology Association standard: IPC/JEDEC J-STD-020D.1 – Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. www.jedec.org/download/search/JSTD020D-01.pdf
- Title 47 of the Code of Federal Regulations (CFR) Part 15, Radio Frequency Devices. www.fcc.gov/oet/info/rules/
- US Military Standard MIL-STD-883 Test Method Standard, Microcircuits: Method 3015.7, Electrostatic Discharge Sensitivity Classification.

You can purchase copies of CENELEC documents, IEC EMC standards, ISO standards, US Military Standards, and CISPR documents from the Information Handling Services (IHS) Global page at: global.ihs.com. IEC EMC standards are also available from the IEC at: www.iec.ch.

Table 2. IEC Electromagnetic Compatibility (EMC) Standards

Standard	Title
IEC 61000-4-1	Electromagnetic compatibility (EMC) - Part 4-1: Testing and measurement techniques - Overview of IEC 61000-4 series
IEC 61000-4-2	Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test
IEC 61000-4-3	Electromagnetic compatibility (EMC) - Part 4-3 : Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test
IEC 61000-4-4	Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test
IEC 61000-4-5	Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test
IEC 61000-4-6	Electromagnetic compatibility (EMC) - Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields

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Introduction

This chapter introduces the Series 5000 of products, LONWORKS networks, and free topology networking.

Product Family Overview

Echelon designed the original Neuron Chip as a system-on-a-chip semiconductor device to provide intelligence and networking capabilities to low-cost control devices. Through a unique combination of hardware and firmware, the Neuron Chip provided all of the key functions necessary to process inputs from sensors and control devices intelligently, and to propagate control information across a variety of network media. Since then, Echelon has continued to develop and improve the families of products that are based on the Neuron Chip.

This book describes the following additions to the Neuron families of products:

- FT 5000 Free Topology Smart Transceivers
- Neuron 5000 Processors

This book describes these products generically as "Series 5000 chips".

All Series 5000 chips include multiple processors, read-write and read-only memory (RAM and ROM), communication subsystems, and I/O subsystems. Each Series 5000 chip includes a processor core for running applications and managing network communications, memory, I/O, and a 48-bit identification number (the Neuron ID) that is unique to every device. In addition, all Series 5000 chips include the Neuron system firmware, which provides an implementation of the LonTalk® protocol (see *Introduction to LonWorks Networks* on page 3 for more information about the protocol), along with I/O libraries, and a task scheduler for application-program management. The device manufacturer provides the application code and the I/O devices that complete a LONWORKS device.

The FT 5000 Free Topology Smart Transceiver provides a built-in transceiver for TP/FT-10 channels, which provides access to polarity insensitive, free-topology, twisted-pair LONWORKS networks.

The Neuron 5000 Processor provides a media-independent communications port which permits short distance Neuron Chip-to-Neuron Chip communications, and can also be used with external line drivers and transceivers of almost any type.

FT 5000 Smart Transceiver

The FT 5000 Free Topology Smart Transceiver is the next generation Echelon Free Topology Smart Transceiver. As a Smart Transceiver, it integrates a high performance Neuron core with a free topology twisted pair transceiver. Together with the FT-X3 Communications Transformer and inexpensive serial memories, the FT 5000 Smart Transceiver provides a lower-cost, higher-performance alternative to the previous generation LONWORKS TP/FT-10 solution.

The FT-X3 communications transformer is a surface mount communications transformer that is compatible both with the FT 5000 Smart Transceiver and with the FT 3120 Smart Transceiver and FT 3150 Smart Transceiver. The FT-X3 transformer provides equivalent magnetic field noise immunity to the previous generation of communications transformers, the FT-X1 and FT-X2.

Neuron 5000 Processor

The Neuron 5000 Processor is the next generation Echelon Neuron Chip. The Neuron 5000 Processor provides a media-independent communications port that supports external

transceivers for EIA-485 or TP/XF-1250 channels, using an external transceiver circuit. The Neuron 5000 Processor can also connect to a link-power TP/FT-10 channel using a LONWORKS LPT-11 Link Power Transceiver. The Neuron 5000 Processor provides a lower-cost, higher-performance alternative to the previous generation of Neuron Chips.

Development Resources for Series 5000 Chips

A wide assortment of technical documentation, diagnostic tools, support programs, and training courses are available to assist customers with their projects. Additionally, Echelon offers fee-based pre-production design reviews of customers' products, schematics, PCB layouts, and bills of material to verify that they comply with published guidelines.

Introduction to LONWORKS Networks

In almost every industry, there is a trend away from proprietary control schemes and centralized systems. The migration towards open, distributed, peer-to-peer networks is being driven by the need for interoperability, robust technology, faster development time, and scale economies.

With thousands of application developers and millions of devices installed worldwide, the LONWORKS system is the leading open solution for building and home automation, industrial, transportation, and public utility control networks. A control network is any group of devices working in a peer-to-peer fashion to monitor sensors, control actuators, communicate reliably, manage network operation, and provide complete access to network data. A LONWORKS network provides communications and complete access to control network data from any device in the network.

The communications protocol used for LONWORKS networks is the ISO/IEC 14908-1 (ANSI/CEA 709.1-B and EN14908.1) Control Network Protocol. This protocol is an international standard seven-layer protocol that has been optimized for control applications and is based on the Open Systems Interconnection (OSI) Basic Reference Model (the OSI Model, ISO standard 7498-1). The OSI Model describes computer network communications through the seven abstract layers described in **Table 3**. The implementation of these layers in a LONWORKS device provides standardized interconnectivity for devices within a LONWORKS network.

Table 3. LONWORKS Network Protocol Layers

OSI Layer		Purpose	Services Provided
7	Application	Application compatibility	Network configuration, self-installation, network diagnostics, file transfer, application configuration, application specification, alarms, data logging, scheduling
6	Presentation	Data interpretation	Network variables, application messages, foreign frame transmission
5	Session	Control	Request/response, authentication

OSI Layer		Purpose	Services Provided
4	Transport	End-to-end communication reliability	Acknowledged and unacknowledged message delivery, common ordering, duplicate detection
3	Network	Destination addressing	Unicast and multicast addressing, routers
2	Data Link	Media access and framing	Framing, data encoding, CRC error checking, predictive carrier sense multiple access (CSMA), collision avoidance, priority, collision detection
1	Physical	Electrical interconnect	Media-specific interfaces and modulation schemes

Echelon's implementation of the ISO/IEC 14908-1 Control Network Protocol is called the *LonTalk protocol*. Echelon provides implementations of the LonTalk protocol with several product offerings, including the Neuron system firmware, LNS® Server, LNS remote client, *i*.LON® servers, the FTXL™ LonTalk protocol stack, and the ShortStack® Micro Server. This document refers to the ISO/IEC 14908-1 Control Network Protocol as the "LonTalk protocol", although other interoperable implementations exist.

A LONWORKS system is based on the following concepts:

- Control systems have many common requirements regardless of application.
- A networked control system is significantly more powerful, flexible, and scalable than a non-networked control system.
- Businesses can save and make more money with control networks over the long term than they can with non-networked control systems.

LONWORKS networks provide a complete suite of messaging services, including end-to-end acknowledgement, authentication, and priority message delivery. Network management services allow network tools to interact with devices over the network, including local or remote reconfiguration of network addresses and parameters, downloading of application programs, reporting of network problems, and start/stop/reset of device application programs.

LONWORKS networks range in sophistication from small networks embedded in machines to large networks with thousands of devices controlling fusion lasers, paper manufacturing machines, or building automation systems. LONWORKS networks are used in buildings, trains, airplanes, factories, and hundreds of other processes. Manufacturers are using open, off-the-shelf chips, operating systems, and parts to build products that feature improved reliability, flexibility, system cost, and performance.

Echelon manufactures many LONWORKS products to help developers, system integrators, and end users implement LONWORKS networks. These products provide a complete LONWORKS solution including development tools, network management software, power line and twisted pair transceivers and control modules, network interfaces, technical support and training.

See *Introduction to the LonWorks Platform* (078-0183-01B) for more information about LONWORKS networks.

Overview of Free Topology Technology

A conventional control system using bus topology wiring (such as an EIA-485 network) consists of a network of sensors and actuators that are interconnected using a twisted wire pair. In accordance with EIA-485 guidelines, all of the devices must be wired in a bus topology to limit electrical reflections and to ensure reliable communications. There is a high cost associated with installing and maintaining the cable plant that links together the devices of an EIA-485-based control system. Bus topology wiring is more time consuming and expensive to install, because the installer is unable to branch or star the wiring where convenient. All devices must be connected directly to the main bus.

The best solution to reduce installation and maintenance costs and to simplify system modifications is to use a free topology communications system. Echelon's free topology transceiver technology offers such a solution, providing an elegant and inexpensive method of interconnecting the different elements of a distributed control system.

A free topology architecture allows the installer to wire the control devices with virtually no topology restrictions. Power is supplied by a local DC power supply located at each device as shown in **Figure 1**.

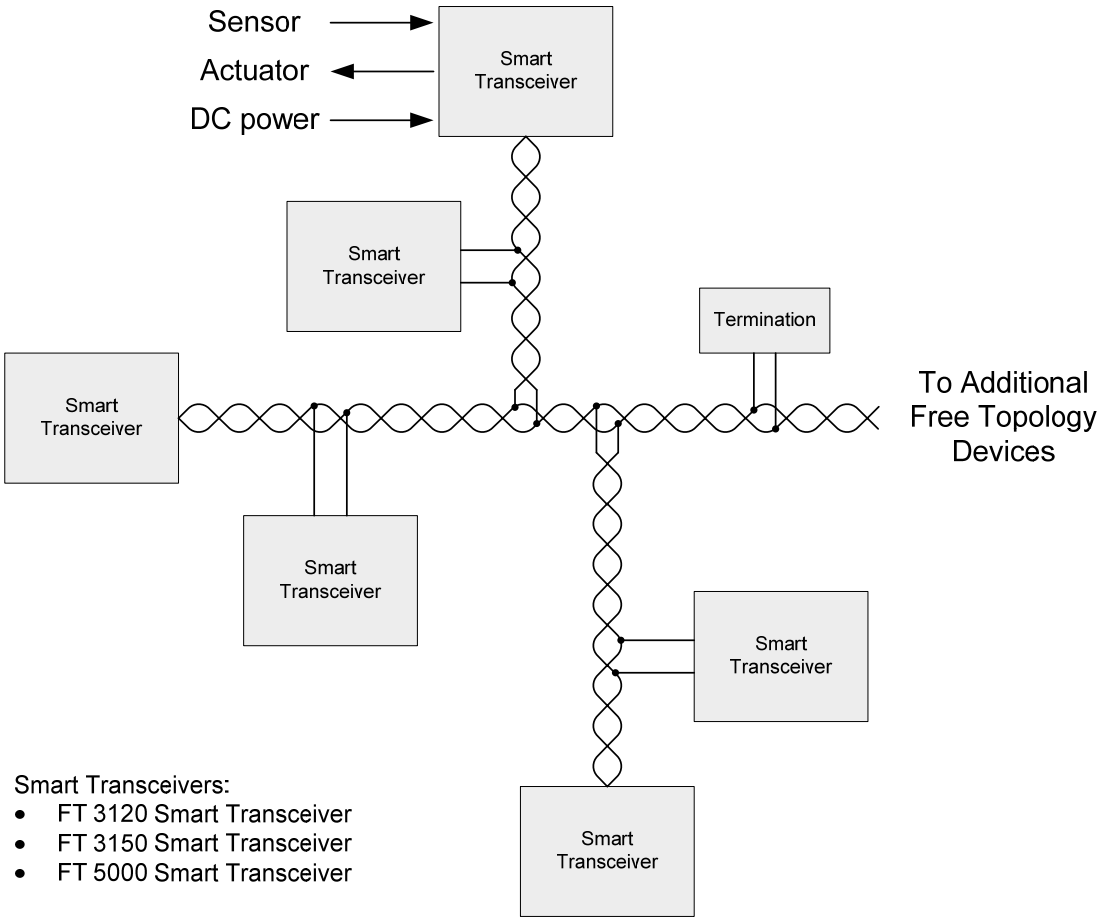


Figure 1. Free Topology Transceiver System

Unlike bus wiring designs, the free topology FT Smart Transceivers or Neuron Chips with associated transceivers use a wiring scheme that supports star, loop, or bus wiring (see **Figure 2**).

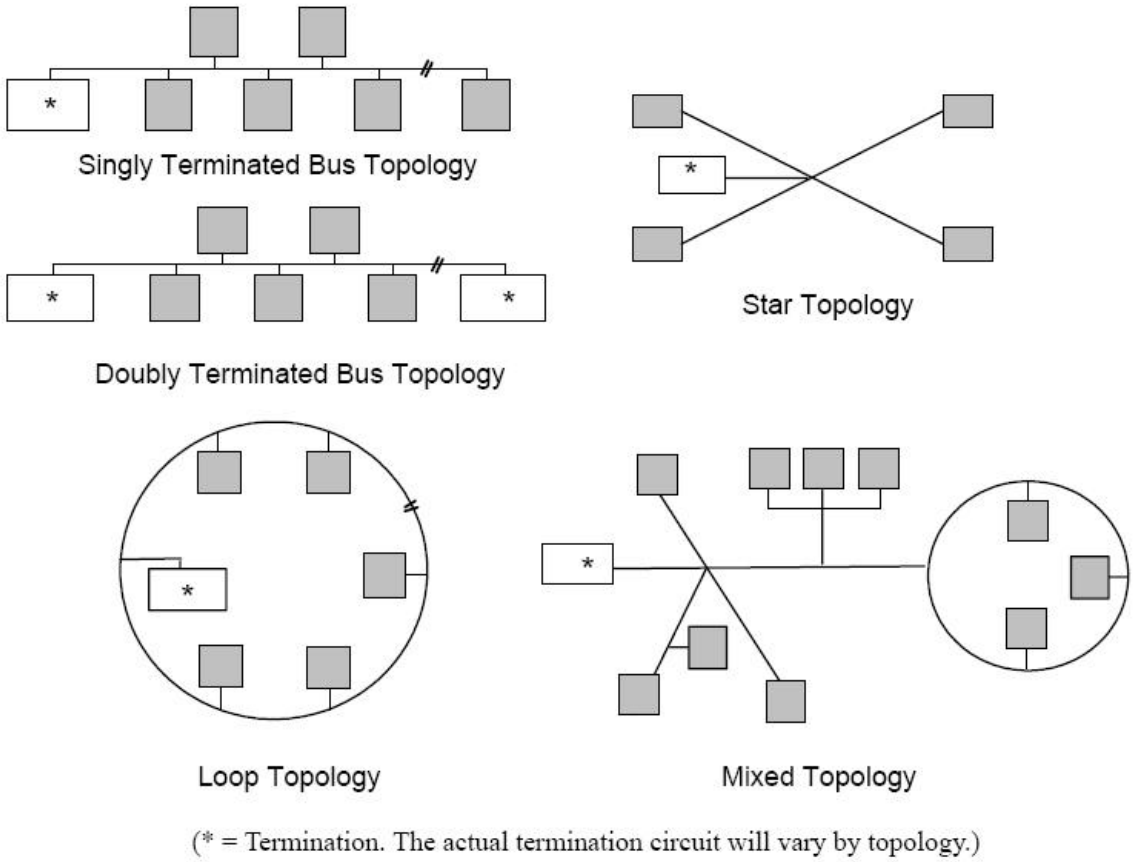


Figure 2. Typical Wiring Topologies Supported by FT Smart Transceivers

This design has many advantages:

- The installer is free to select the method of wiring that best suits the installation, reducing the need for advanced planning and allowing last minute changes at the installation site.
- If installers have been trained to use one style of wiring for all installations, free topology technology can be introduced without requiring retraining.
- Retrofit installations with existing wiring plants can be accommodated with minimal, if any, rewiring. This capability ensures that FT Smart Transceiver technology can be adapted to both old and new projects.
- Free topology permits FT Smart Transceiver or Neuron Chip systems to be expanded in the future by simply tapping into the existing wiring where it is most convenient to do so. This reduces the time and expense of system expansion, and from the customer's perspective, keeps down the life-cycle cost of the free topology network.

Key Features of Series 5000 Chips

Series 5000 chips include the following key features:

- Require only 3.3 V operation
- Provide a higher performance Neuron Core, with internal system clock rates up to 80 MHz
- Require as little as 30 mW of power for operations
- Packaged as a 7 mm by 7 mm 48-pin quad flat no leads (QFN) chip
- Allow for substantial device price reduction
- Include a serial memory interface for inexpensive external EEPROM and flash non-volatile memories
- Support up to 254 network variables (NVs) for FT 5000 Smart Transceivers and Neuron 5000 Processors, without the need for a host microprocessor
- Support user-programmable interrupts to provide faster response time to external events
- Provide an interface for the Institute of Electrical and Electronics Engineers (IEEE) Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990) of the Joint Test Action Group (JTAG) to allow a Series 5000 chip to be included in the boundary-scan chain for device production tests
- Include 12 I/O pins with 35 programmable standard I/O models that support both 5 V and 3.3 V I/O operation
- Support up to 42 KB of user application code space
- Include 64 KB RAM (of which 44 KB is user accessible) and 16 KB of ROM on-chip
- Include a unique 48-bit Neuron ID in every device for network installation and management
- Support a –40°C to +85°C operating temperature range
- Compliant with the European Union Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC.

Additional Key Features for FT 5000 Smart Transceivers

FT 5000 Smart Transceivers include the following additional key features:

- Support the low-cost surface mount FT-X3 communications transformer for FT 5000 Smart Transceivers
- Support polarity insensitive free topology star, daisy chain, bus, loop, or mixed topology wiring for TP/FT-10 channels
- Compliant with TP/FT-10 channels that currently use FT 3120 Smart Transceivers, FT 3150 Smart Transceivers, FTT-10A transceivers, or LPT-11 transceivers
- Provide very high common-mode noise immunity

Specification Summaries

The following sections summarize the specifications for FT 5000 Smart Transceivers and Neuron 5000 Processors.

Specification Summary for FT 5000 Smart Transceivers

Table 4 summarizes the specifications for the FT 5000 Smart Transceiver.

Table 4. FT 5000 Smart Transceiver Specification Summary

Description	Specification
Data communications type	Differential Manchester encoding
Transmission speed	78 kilobits per second
Network polarity	Polarity insensitive
Number of transceivers per network segment	Up to 64
Network wiring	24 to 16 AWG twisted pair; see Chapter 5, *Network Cabling and Connections for FT Devices*, on page 101 for specific wire types
Network length for free topology	Varies by wire type. See Chapter 5, *Network Cabling and Connections for FT Devices*, on page 101: • Up to 1000 m (3280 ft) maximum total wire with one repeater • Up to 500 m (1640 ft) maximum total wire with no repeaters
Network length for bus topology	Varies by wire type. See Chapter 5, *Network Cabling and Connections for FT Devices*, on page 101: • 5400 m (17 710 ft) maximum total wire with one repeater • 2700 m (8850 ft) maximum total wire with no repeaters
Maximum stub length for bus topology	3 m (9.8 ft)
Network termination	One terminator for free topology Two terminators for bus topology

Description	Specification
Voltage for FT 5000 Smart Transceiver	3.3 V ±5%
Operating temperature	–40 ºC to +85 ºC
Reflow soldering temperature profile	Refer to Joint Industry Standard document *IPC/JEDEC J-STD-020D.1* (March 2008)
Peak reflow soldering temperature	260 ºC
Package type	48-pin QFN
RoHS compliant	Yes
EMI	Designed to comply with FCC Part 15 Subpart B and EN 55022 Level B
ESD	Designed to comply with EN 61000-4-2, Level 4
Radiated Electromagnetic Susceptibility	Designed to comply with EN 61000-4-3, Level 3
Fast Transient/Burst Immunity	Designed to comply with EN 61000-4-4, Level 4
Surge Immunity	Designed to comply with EN 61000-4-5, Level 3
Conducted RF Immunity	Designed to comply with EN 61000-4-6, Level 3

Table 5 summarizes the specifications for the FT-X3 Communications Transformer.

Table 5. FT-X3 Communications Transformer Specification Summary

Description	Specification
Operating humidity	25-90% RH @50 °C, non-condensing
Non-operating humidity	95% RH @ 50 °C, non-condensing
Vibration	1.5 g peak-to-peak, 8 Hz to 2 kHz
Mechanical shock	100 g (peak)
Reflow soldering temperature profile	Refer to Joint Industry Standard document *IPC/JEDEC J-STD-020D.1* (March 2008)
Peak reflow soldering temperature	245 ºC

Specification Summary for Neuron 5000 Processors

Table 6 summarizes the specifications for the Neuron 5000 Processor.

Table 6. Neuron 5000 Processor Specification Summary

Description	Specification
Transmission speed	Depends on network transceiver: • 78 kbit/s for TP/FT-10 channel • 1250 kbit/s for TP/XF-1250 channel • See EIA-485 channel specification for transmission speed characteristics
Voltage for Neuron 5000 Processor	3.3 V ±10%
Operating temperature	–40 ºC to +85 ºC
Reflow soldering temperature profile	Refer to Joint Industry Standard document *IPC/JEDEC J-STD-020D.1* (March 2008)
Peak reflow soldering temperature	260 ºC
Package type	48-pin QFN
RoHS compliant	Yes
EMC	Depends on network transceiver

2

Hardware Resources

This chapter provides an overview of the hardware resources for an FT 5000 Smart Transceiver and a Neuron 5000 Processor, including the overall chip architecture, memory interface, operating parameters, pinouts, network connection, clock requirements, the reset function, and integrity mechanisms.

Series 5000 Architecture

The main components of the architecture for a Series 5000 chip, as shown in **Figure 3** on page 13, include:

- CPUs — a Series 5000 chip includes three processors to manage operation of the chip, the network, and the user application. At higher clock rates, there is also a separate processor to handle interrupts. See *Multiple Processors* on page 15.
- ROM — a Series 5000 chip includes 16 KB of read-only memory (ROM), which holds the default system firmware image.
- RAM — a Series 5000 chip includes 64 KB of random access memory (RAM), which stores user applications and data. The RAM is partitioned according to a logical memory map so that the amount that is available for user applications and data is less than 64 KB. See *Memory Map* on page 22 for information about how the RAM is configured.
- Serial memory interface — this interface manages the external non-volatile memory (NVM) using the serial peripheral interface (SPI) or the serial inter-integrated circuit (I^2C) interface.
- Communications port — the communications port provides network access for the chip. For an FT 5000 Smart Transceiver, this port connects to an FT-X3 Communications Transformer. For a Neuron 5000 Processor, this port connects to an external transceiver. See *Network Connection* on page 56.
- I/O — 12 dedicated I/O pins (see *Characteristics of the Digital Pins* on page 45).
- Clock, reset, and service — on-chip clock, phase-locked loop (PLL), reset, and service-pin functions.
- JTAG — a Series 5000 chip includes a JTAG (IEEE 1149.1) interface for boundary scan operations. See *JTAG Interface* on page 33.

The pinout labels shown in **Figure 3** are described in *Pin Assignments* on page 35.

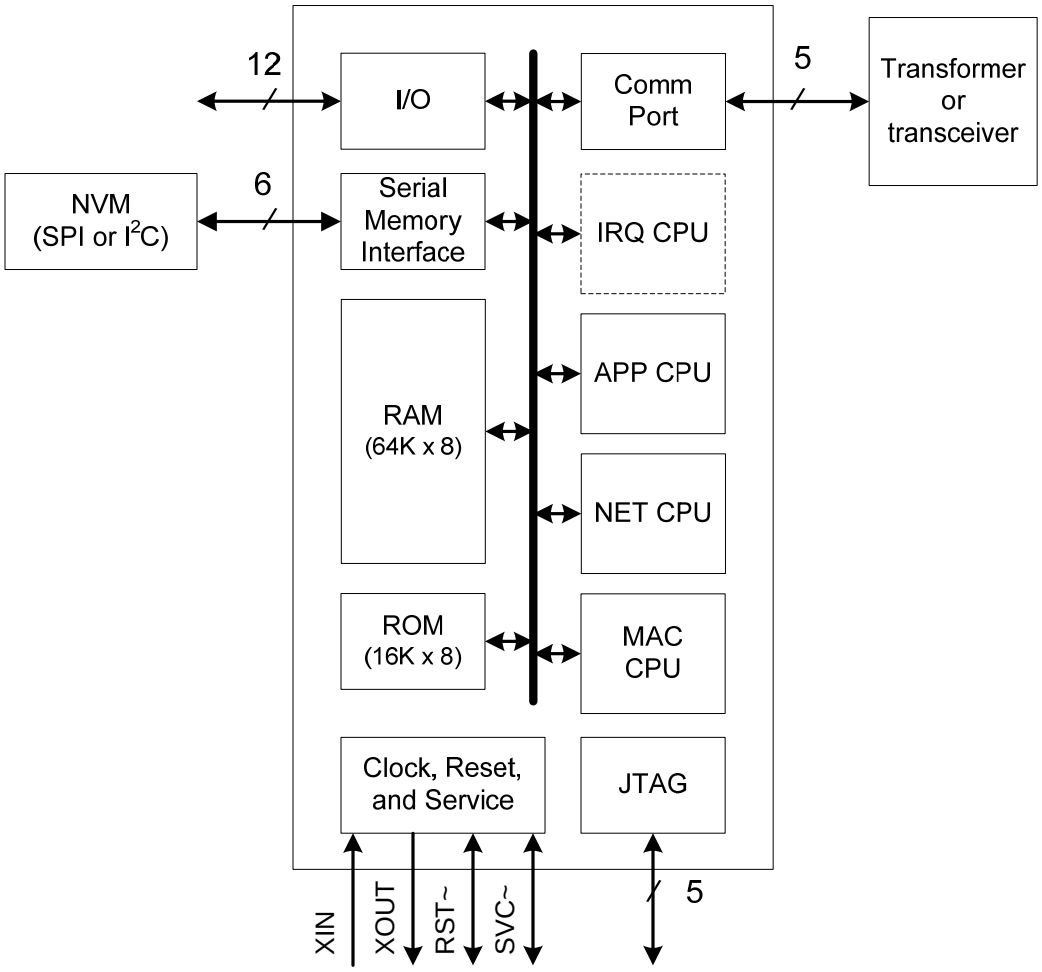


Figure 3. Series 5000 Chip Architecture

Neuron Processor Architecture

The basic Neuron processor architecture is stack-oriented:

- An 8-bit-wide stack is used for data references, and the arithmetic-logic unit (ALU) operates on the TOS (Top of Stack) register and on the next entry in the data stack (which is in RAM).
- Another stack stores the return addresses for CALL instructions, and can also be used for temporary data storage.

This stack architecture leads to very compact code. See *Assembly Instruction Set* on page 17 for a summary of the instruction set.

Figure 4 on page 14 shows the layout of a base page, which can be up to 256 bytes long. Each of the chip's processors uses a different base page, whose address is given by the contents of the BP (Base Page) register of that processor. The top of the data stack is in the 8-bit TOS register, and the next element in the data stack is at the location within the base page at the offset given by the contents of the DSP (Data Stack Pointer) register. The assembler

shorthand symbol NEXT refers to the next element in the data stack, which is determined by contents of the location (BP+DSP) in memory, and is thus not an actual processor register.

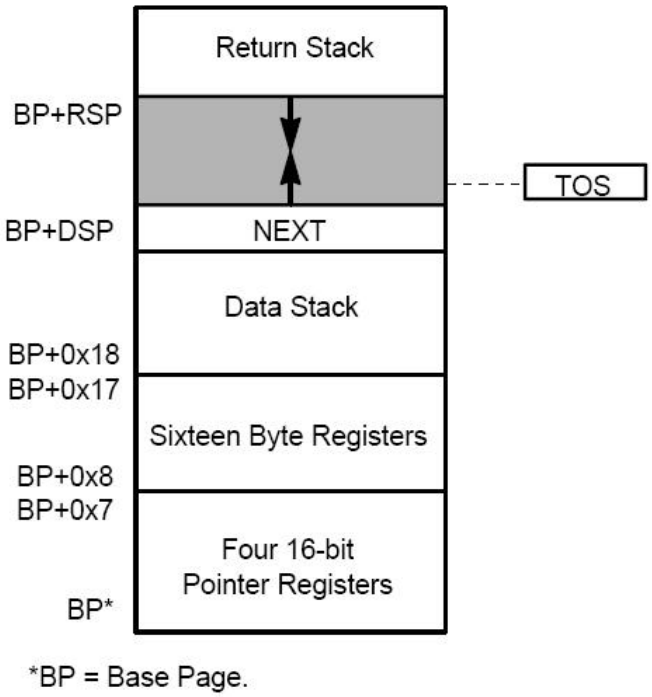


Figure 4. Base-Page Memory Layout

The data stack grows from low memory towards high memory, and is managed through the DSP (Data Stack Pointer) register. Pushing a byte of data onto the data stack involves the following steps:

1. Incrementing the DSP register
2. Storing the current contents of TOS at the address (BP+DSP) in memory
3. Moving the byte of data to TOS

Popping a byte of data from the data stack involves the following steps:

1. Moving TOS to the destination
2. Moving the contents of the address (BP+DSP) in memory to TOS
3. Decrementing the DSP register

The return stack grows from high memory towards low memory, and is managed through the RSP (Return Stack Pointer) register. Calling a subroutine involves the following steps:

1. Storing the high byte of the instruction pointer (IP) register at the address (BP+RSP) in memory
2. Decrementing RSP
3. Storing the low byte of IP at the address (BP+RSP) in memory
4. Decrementing RSP
5. Moving the destination address to the IP register

Similarly, returning from a subroutine involves the following steps:

1. Incrementing RSP
2. Moving the contents of (BP+RSP) to the low byte of the IP register
3. Incrementing RSP
4. Moving the contents of (BP+RSP) to the high byte of IP

The primary programming language used for applications is the Neuron C language, which is a derivative of the ANSI C language that has been optimized and enhanced for LONWORKS distributed control applications. The major enhancements include:

- A network communication model, based on functional blocks and network variables, that simplifies and promotes data sharing between like and disparate devices.
- A network configuration model, based on functional blocks and configuration properties, that facilitates interoperable network configuration tools.
- A type model based on standard and user resource files that expands the market for interoperable devices by simplifying the integration of devices from multiple manufacturers.
- An extensive set of I/O models that support the I/O capabilities of Neuron Chips and Smart Transceivers.
- Powerful event-driven programming extensions, based on **when** statements, that provide easy handling of network, I/O, and timer events.
- A high-level programming model that supports application-specific interrupt handlers and synchronization tools.

See the *Neuron C Programmer's Guide* for more information about the Neuron C programming language. The support for these capabilities is part of the Neuron firmware, and does not need to be written by the programmer.

Multiple Processors

The Neuron core is composed of four independent logical processors:

- Processor 1 is the Media Access Control (MAC) processor
- Processor 2 is the network (NET) processor
- Processor 3 is the application (APP) processor
- Processor 4 is the interrupt (ISR) processor

The interrupt processor is only available for system clock rates of 20 MHz and higher. At the two lower system clock rates, interrupts are handled by the application processor. See *Interrupts* on page 17 for more information about interrupts.

The processors share a common memory, arithmetic-logic unit (ALU), and control circuitry. Each processor has its own set of registers, as listed in **Table 7**.

Table 7. Register Set

Register	Size (Bits)	Contents
FLAGS	8	Carry Bit and reserved internal flags
IP	16	Next Instruction Pointer

Register	Size (Bits)	Contents
BP	16	Address of 256-Byte Base Page
DSP	8	Data Stack Pointer within Base Page
RSP	8	Return Stack Pointer within Base Page
TOS	8	Top of Data Stack, ALU Input

Processor 1 is the MAC layer processor that handles layers 1 and 2 of the seven-layer LonTalk® protocol, which includes driving the communications subsystem hardware and running the media access control algorithm. The MAC processor communicates with the NET processor using network buffers located in shared RAM memory, as shown in **Figure 5**.

Processor 2 is the network processor that implements layers 3 through 6 of the LonTalk protocol. The NET processor handles network variable processing, addressing, transaction processing, authentication, background diagnostics, software timers, network management, and routing functions. The NET processor uses network buffers in shared memory to communicate with the MAC processor, and application buffers to communicate with the APP processor. These buffers are also located in shared memory (RAM). Access to the shared memory is mediated with hardware semaphores to resolve contention when updating shared data.

Processor 3 is the application processor. The APP processor executes the user-written code, together with the system services called by user code.

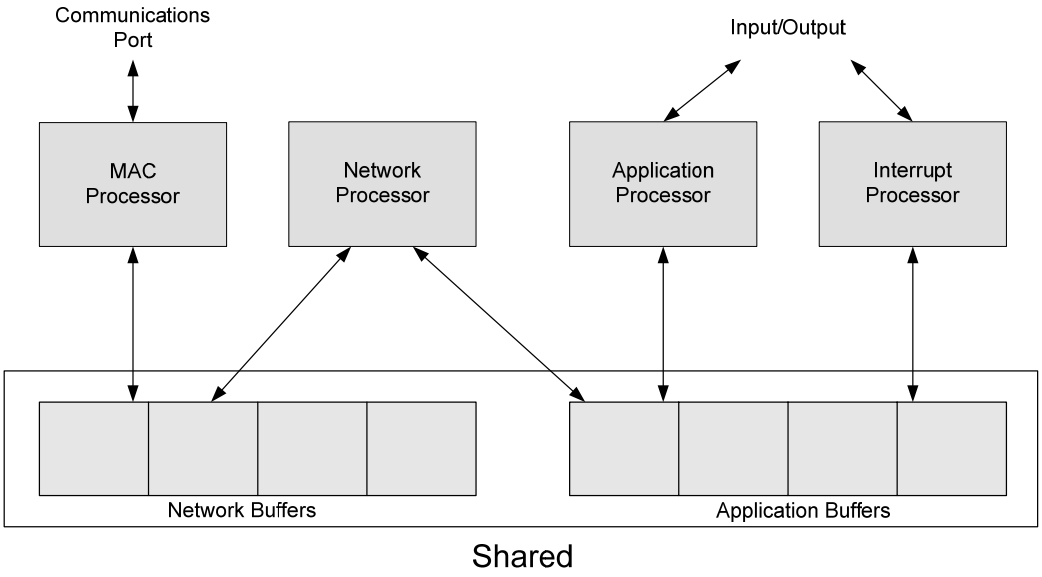


Figure 5. Processor Shared Memory Allocation

Interrupts

The Series 5000 architecture provides hardware support for handling three types of interrupts:

- Lowest priority: application interrupts
- Medium priority: system interrupts
- Highest priority: system-level traps

Application interrupts are asynchronous events related to I/O objects within an application program. An application uses the Neuron C **interrupt()** clause to define the interrupt condition and the interrupt task that handles the condition. The Neuron C program runs the interrupt task whenever the interrupt condition is met. See the *Neuron C Programmer's Guide* for more information about writing interrupt tasks and handling interrupts.

System interrupts are asynchronous system events, such as communications events or SPI UART events. These interrupts are handled by the system firmware.

System-level traps are also system events, generally error conditions. See *Processor Integrity* on page 75 for more information about these conditions.

For system clock rates of 20 MHz and higher, interrupts are handled by an independent logical processor within the Neuron Core. At the two lower system clock rates, interrupts are handled by the application processor. Thus, at the higher clock rates, an interrupt handler runs in parallel with the application processor, and so does not affect the application processor's registers and stack space. At lower clock rates, an interrupt causes a context switch within the application processor, that is, the interrupt handler saves the processor's registers before it runs and restores them after it completes. Thus, the current instruction always completes prior to servicing a new interrupt. Such context switches also occur within the ISR processor when higher priority interrupts require service.

Thus, when interrupts are processed within the ISR processor, application performance is not degraded, but when interrupts are processed within the APP processor, application performance can be affected because the one processor handles both the application and the interrupts.

Assembly Instruction Set

Table 8 on page 18, **Table 9** on page 19, and **Table 10** on page 20 list the processor instructions, their sizes (in bytes), and their timings (in processor cycles). This information is provided to help you calculate code sizes and execution times.

Most assembly instructions take between one and seven processor cycles (two instructions require 14 cycles). Execution time scales inversely with the system clock rate. The formula for instruction time is:

$$InstructionTime = \frac{(NumberOfCycles \times 3)}{SystemClock}$$

For example, at a system clock rate of 80 MHz, instruction times vary between 37.5 ns and 175 ns.

Programming for a Neuron Chip or Smart Transceiver uses the Neuron C programming language with either the NodeBuilder FX Development Tool or the Mini FX Evaluation Kit.

Additional functions can be written in the Neuron Assembly language. The Neuron C compiler can optionally produce an assembly listing, and examining this listing can help the programmer to optimize the Neuron C source code. See the *Neuron Assembly Language Reference* for more information about the processor instructions.

Table 8. Program Control Instructions

Instruction	Instruction Size (Bytes)	CPU Cycles Required	Description
NOP	1	1	No operation
SBR	1	1	Short unconditional branch Offset: 0 to 15.
BR BRC BRNC	2	2	Branch Branch on carry Branch on not carry Offset: –128 to +127.
SBRZ SBRNZ	1	3	Short branch on TOS zero Short branch on TOS not zero Offset: 0 to 15. Drops TOS.
BRF	3	4	Unconditional branch far
BRZ BRNZ	2	4	Branch on TOS zero Branch on TOS not zero Offset: –128 to +127. Drops TOS.
RET	1	5	Return from subroutine. Drops two bytes from return stack.
BRNEQ	3	4 / 6 (taken / not taken)	Branch if TOS not equal Offset: –128 to +127. Drops TOS if equal.
DBRNZ	2	5	Decrement [RSP] and branch if not zero Offset: –128 to +127. If not taken, drops one byte from return stack.
CALLR	2	5	Call subroutine relative Offset: –128 to +127. Pushes two bytes to return stack.
CALL	2	6	Call subroutine Address in low 8 KB. Pushes two bytes to return stack.

Instruction	Instruction Size (Bytes)	CPU Cycles Required	Description
CALLF	3	7	Call subroutine far Pushes two bytes to return stack.

Table 9. Memory and Stack Instructions

Instruction	Instruction Size (Bytes)	CPU Cycles Required	Description
PUSH TOS	1	3	Increment DSP, duplicate TOS into NEXT
DROP TOS	1	3	Move NEXT to TOS, decrement DSP
DROP_R TOS	1	6	Move NEXT to TOS, decrement DSP, return from call
PUSH NEXT PUSH DSP PUSH RSP PUSH FLAGS	1	4	Push processor register
POP NEXT POP DSP POP RSP POP FLAGS	1	4	Pop processor register
DROP NEXT	1	2	Decrement DSP
DROP_R NEXT	1	5	Decrement DSP and return from call
PUSH !D POP !D	1	4	Push / pop byte register [8 to 23]
PUSH !TOS	1	4	Push TOS EA = BP + TOS, push byte to NEXT.
POP !TOS	1	4	Pop TOS EA = BP + TOS, pop byte from NEXT.
PUSH [RSP]	1	4	Push from return stack to data stack, RSP unchanged
DROP [RSP]	1	2	Increment RSP
PUSHS #literal	1	4	Push short literal value [0 to 7]

Instruction	Instruction Size (Bytes)	CPU Cycles Required	Description
PUSH #literal	2	4	Push 8-bit literal value [0 to 255]
PUSHPOP	1	5	Pop from return stack, push to data stack
POPPUSH	1	5	Pop from data stack, push to return stack
PUSH [DSP][-D] POP [DSP][-D]	1	5	Push / pop DSP modified by D EA = BP + DSP – displacement [1 to 8]
PUSHD #literal	3	6	Push 16-bit literal value, high byte first
PUSHD [PTR]	1	6	Push from 16-bit pointer [0 to 3], high byte first
POPD [PTR]	1	6	Pop to 16-bit pointer [0 to 3], low byte first
PUSH [PTR][TOS] POP [PTR][TOS]	1	6	Push / pop 16-bit pointer [0 to 3], modified by TOS EA = (16-bit pointer) + TOS.
PUSH [PTR][D] POP [PTR][D]	2	7	Push / pop 16-bit pointer [0 to 3], modified by D EA = (16-bit pointer) + displacement [0 to 255]
PUSH absolute POP absolute	3	7	Push / pop absolute memory address
Note: EA = Effective Address.			

Table 10. Arithmetic and Logic Instructions

Instruction	Instruction Size (Bytes)	CPU Cycles Required	Description
INC DEC NOT	1	2	Increment TOS Decrement TOS Negate TOS
ROLC RORC	1	2	Rotate left TOS through carry Rotate right TOS through carry
SHL SHR	1	2	Unsigned left shift TOS, clear carry Unsigned right shift TOS, clear carry

Instruction	Instruction Size (Bytes)	CPU Cycles Required	Description
SHLA SHRA	1	2	Signed left shift TOS into carry Signed right shift TOS into carry
ADD AND OR XOR ADC	1	4	Operate with NEXT on TOS, drop NEXT
ADD #literal AND #literal OR #literal XOR #literal	2	3	Operate with literal on TOS
ADD_R AND_R OR_R XOR_R	1	7	Operate with NEXT on TOS, drop NEXT and return
ALLOC #literal	1	3	Add [1 to 8] to data stack pointer
DEALLOC_R #literal	1	6	Subtract [1 to 8] from data stack pointer and return
SUB NEXT,TOS	1	4	TOS = NEXT – TOS, drop NEXT
SBC NEXT, TOS	1	4	TOS = NEXT – TOS – carry, drop NEXT
SUB TOS,NEXT	1	4	TOS = TOS – NEXT, drop NEXT
XCH	1	4	Exchange TOS and NEXT
INC [PTR]	1	6	Increment 16-bit pointer [0 to 3]
DIV	1	14	Divide NEXT by TOS, quotient is in TOS, remainder is in NEXT
MUL	1	14	Multiply NEXT * TOS, result is in TOS, NEXT

Memory Architecture

The memory architecture for a Series 5000 chip includes on-chip memory and off-chip non-volatile memory. Every Series 5000 device must have at least 2 KB of off-chip memory available in an EEPROM device. A Series 5000 device can optionally include additional off-

chip EEPROM memory (as a larger EEPROM device) or off-chip flash memory in addition to an EEPROM device, for additional application data or alternate system images.

Important: The memory architecture for a Series 5000 chip uses a serial interface for off-chip memory. This architecture differs from that of Series 3100 chips:

- Neuron 3120 Chips and 3120 Smart Transceivers use on-chip EEPROM, with no external memory.
- Neuron 3150 Chips and 3150 Smart Transceivers use on-chip EEPROM, plus a parallel interface for off-chip memory.
- PL 3170 Smart Transceivers and FTXL 3190 Free Topology Transceivers use on-chip EEPROM, with no external memory.

On-Chip Memory

A Series 5000 chip has the following on-chip memory:

- 16 KB of read-only memory (ROM)

  The ROM holds the default Neuron firmware image for the chip, including the system firmware for the MAC and network processors.

- 64 KB of random access memory (RAM)

  The RAM provides memory for user applications and data, stack segments for each processor, and network and application buffers. The RAM is partitioned according to a logical memory map, as described in *Memory Map*.

A Series 5000 chip contains no internal non-volatile memory (such as EEPROM memory) for application use. However, each Series 5000 chip does contain its unique Neuron identifier (Neuron ID) in non-volatile read-only memory.

The chip's memory management block allows the RAM to emulate both ROM and non-volatile memory (NVM) by ensuring that changes to the RAM are shadowed to external NVM at appropriate intervals. All writes that are intended for NVM are written to the RAM, and then are shadowed to the NVM. Thus, the chip's internal processors access the RAM only; they do not directly access either the ROM or external NVM.

The state of the RAM is retained as long as power is applied to the device. After a device reset, the initialization sequence copies the contents of the ROM and relevant NVM data to the RAM.

Memory Map

A Neuron C application has a memory map of 64 KB. **Figure 6** on page 23 shows the memory map for a Series 5000 chip. The hardware template for a device specifies how the application uses the memory map. The memory map is a logical view of device memory, rather than a physical view, because the Series 5000 chip's processors only directly access RAM.

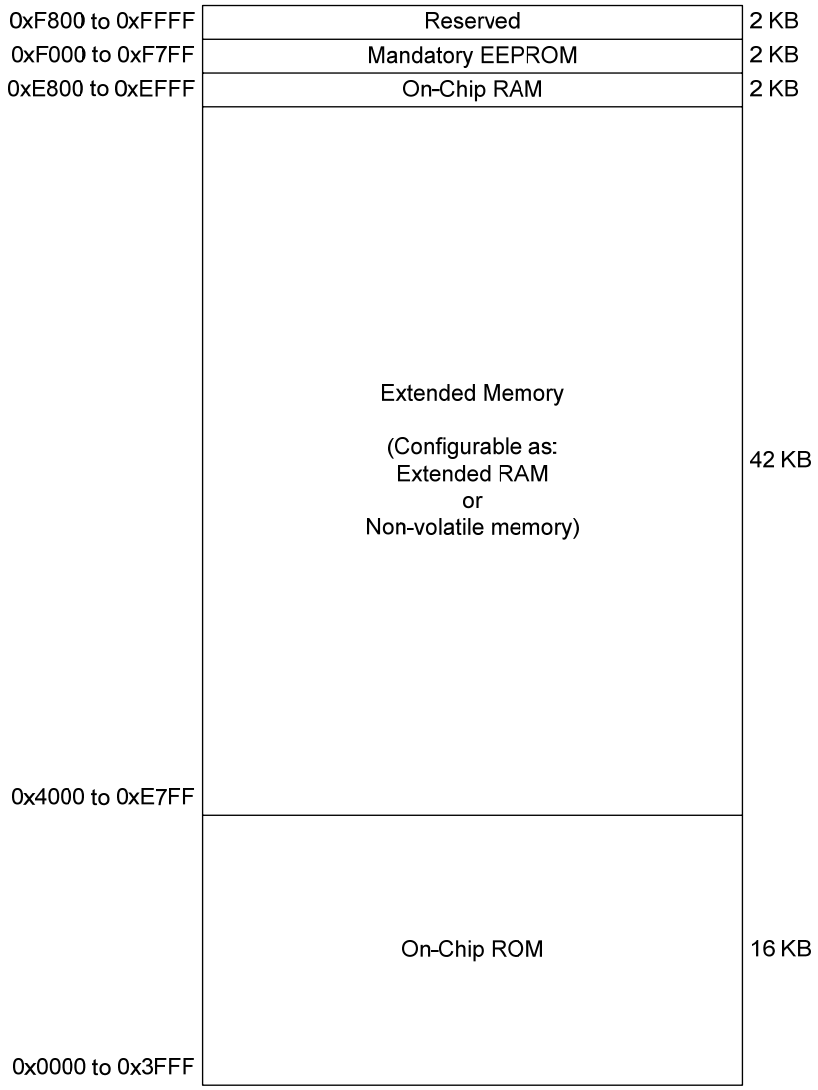


Figure 6. Series 5000 Chip Memory Map

The memory map divides the Series 5000 chip's physical RAM into the following types of logical memory:

- On-chip ROM (16 KB at addresses 0x0000 to 0x3FFF) — This area is a copy of the system firmware image and system function libraries from the physical ROM. This area is write-protected so that an application cannot alter the system firmware.
- Extended on-chip RAM or extended non-volatile memory (up to 42 KB at addresses 0x4000 to 0xE7FF) — Some of this area is shadowed into RAM from the external NVM, and some of this area is application-usable RAM. Memory ranges for each are configurable within the device hardware template.
- On-chip RAM (2 KB at addresses 0xE800 to 0xEFFF) — This area holds stack segments and RAMNEAR data.
- Mandatory EEPROM (2 KB at addresses 0xF000 to 0xF7FF) — This area is shadowed from the mandatory 2 KB of EEPROM, and holds device configuration data. For small devices, this 2 KB can also hold application code and data.

- Reserved memory (2 KB at addresses 0xF800 to 0xFFFF) — This area is reserved for system use.

Using the NodeBuilder FX Development Tool or the Mini FX Evaluation Kit, you can adjust the address values for the extended non-volatile memory and the extended on-chip RAM within a device's hardware template. These two values share the same area of physical RAM.

Important: The size of an external EEPROM part must include the 2 KB of mandatory EEPROM as well as the size required for application code and data.

Example: A 16 KB EEPROM provides 2 KB for the mandatory EEPROM (at addresses 0xF000 to 0xF7FF) and 14 KB for application code and data (at addresses 0x4000 to 0x77FF. Thus, the device memory map can include 28 KB, 0x7800 to 0xE7FF, for the extended on-chip RAM.

External Serial Memory Interface

The interface for accessing off-chip non-volatile memory (NVM) is a serial interface that follows either of the following protocols: serial Inter-Integrated Circuit (I^2C) or serial peripheral interface (SPI). At the time of publication of this manual, there are no serial flash parts that use the I^2C protocol and meet the required specifications for the Series 5000 external memory interface; thus only SPI serial flash memory parts are described. However, there are many available Electrically Erasable Programmable Read-Only Memory (EEPROM) devices that use either the I^2C protocol or the SPI protocol, and meet the required specifications for the Series 5000 external memory interface.

A Series 5000 chip requires at least 2 KB of off-chip memory available in an EEPROM device. **Table 11** summarizes the allowed device configurations for external memory.

Table 11. Allowed External Memory Device Configurations

EEPROM		Flash	
I^2C	SPI	SPI	Description
☑			→ A single I^2C EEPROM memory device, from 2 KB to 64 KB in size → No flash memory device
	☑		→ A single SPI EEPROM memory device, from 2 KB to 64 KB in size → No flash memory device
☑		☑	→ One I^2C EEPROM (at least 2 KB in size, up to 64 KB in size, but the system uses only the first 2 KB of the EEPROM memory) → One SPI flash memory device
	☑	☑	→ One SPI EEPROM (at least 2 KB in size, up to 64 KB in size, but the system uses only the first 2 KB of the EEPROM memory) → One SPI flash memory device

As **Table 11** shows, a Series 5000 device supports using a single EEPROM memory device, or a single EEPROM memory device plus a single flash memory device. Small applications could use a single EEPROM memory device for both application code and configuration data, but larger applications are more likely to use a small EEPROM memory device for configuration data and a flash memory device for application code.

If a Series 5000 device includes external flash memory, the flash memory represents the entire user non-volatile memory for the device. That is, any additional EEPROM memory beyond the mandatory 2 KB is not used.

For 32 KB EEPROM memory devices, the system firmware reserves 256 bytes of the total memory space. That is, a 32 KB EEPROM provides 32 512 bytes of memory for user application code and data, rather than 32 768 bytes. Thus, the memory map for a 32 KB EEPROM memory device includes 2048 bytes (2 KB) for the mandatory EEPROM memory plus up to 30 464 (0x7700) bytes for the extended non-volatile memory.

For 64 KB EEPROM memory devices, the maximum amount of EEPROM that can be used is equal to the amount of RAM in the Series 5000 device, 44 KB. The memory map for a 64 KB EEPROM memory device includes 2 KB for the mandatory EEPROM memory plus up to 42 KB for extended non-volatile memory. The extra 20 KB of data space in the EEPROM memory device is unused by an application, but could be used to hold an external system image to upgrade the device's system firmware.

If your device will support inclusion of a future alternate system firmware image, be sure to add an extra 16 KB to the overall external memory requirements for the device. That is, if the device uses an EEPROM device, ensure that the EEPROM device is at least 16 KB larger than what your application requires; if the device uses a flash device in addition to the required 2 KB EEPROM device, the standard 64 KB flash device is large enough for any application plus a future alternate system image.

If your device includes an alternate system firmware image, you can store the image either in EEPROM or flash memory. For 64 KB EEPROM or flash devices, the alternate system image is stored in the last 16 KB of the device, and so does not reside with the application code.

Serial Inter-Integrated Circuit (I^2C)

The serial Inter-Integrated Circuit (I^2C) protocol for the Series 5000 chip uses the pins listed in **Table 12** and shown in **Figure 7** on page 26.

Table 12. Memory Interface Pins for the I^2C Protocol

Pin Number	Pin Name	Direction	Description
Pin 43	SDA_CS1~	Bidirectional	Serial Data (SDA) signal
Pin 45	SCL	Output	Serial Clock (SCL) signal
Note: Signal direction is from the point of view of the Series 5000 chip.			

These pins are 3.3 V pins, and are 5 V tolerant.

A Series 5000 chip is always the master I^2C device; an external NVM device is always a slave device.

The I²C memory device must reside at address 0 (typically set by tying the device's A0, A1, and A2 pins to GND). Both 1-byte and 2-byte address modes are supported, but 3-byte addressing mode is not supported. The device's data type identifier code is b'1010.

A Series 5000 chip runs the I²C protocol from the serial memory interface at 400 kHz (the I²C fast mode).

Important: If the Series 5000 device does not include any SPI memory devices, you must add a 10 kΩ pull-down resistor to pin 46 (MISO).

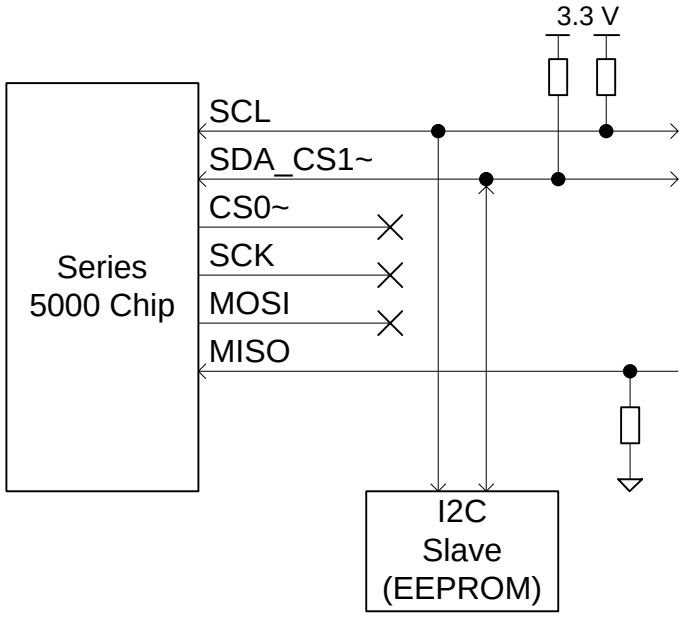


Figure 7. I²C Memory Interface

The serial clock and serial data pins (SCL and SDA_CS1~) are open drain pins, and thus require pull-up resistors. The value of the pull-up resistors depends on the total bus capacitance (number of devices connected to the bus and length of the bus); see the *I2C-bus specification and user manual* (UM10204) from NXP Semiconductor. For example, for a total bus capacitance of 30 pF, you can use a minimum resistance value of 1 kΩ, and a maximum resistance value of 10 kΩ.

Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) protocol for the Series 5000 chip uses the pins listed in **Table 13** and shown in **Figure 8** on page 27.

Table 13. Memory Interface Pins for the SPI Protocol

Pin Number	Pin Name	Direction	Description
Pin 40	CS0~	Output	First slave-select (SS) signal
Pin 43	SDA_CS1~	Bidirectional	Second slave-select (SS) signal
Pin 46	MISO	Input	Master Input, Slave Output (MISO) signal
Pin 47	SCK	Output	Serial clock (SCK) signal

Pin Number	Pin Name	Direction	Description
Pin 48	MOSI	Output	Master Output, Slave Input (MOSI) signal
Note: Signal direction is from the point of view of the Series 5000 chip.			

These pins are 3.3 V pins, and are 5 V tolerant.

A Series 5000 chip is always the master SPI device; any external NVM devices are always slave devices. Multimaster configurations are not supported.

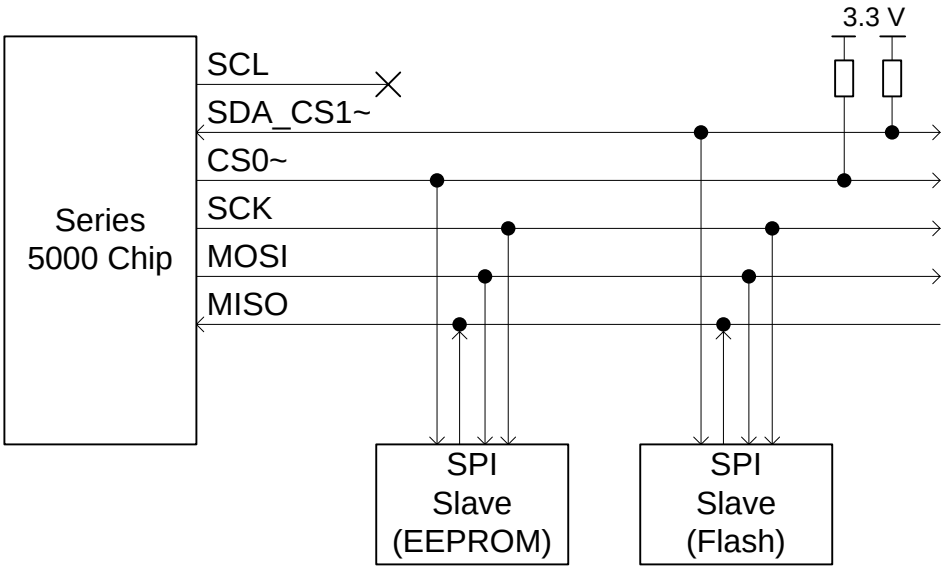


Figure 8. SPI Memory Interface

The two chip select pins (CS0~ and SDA_CS1~) require 10 kΩ pull-up resistors.

Important: If the Series 5000 device does not include any I²C memory devices, you must also add a pull-up resistor (maximum 10 kΩ) to pin 45 (SCL).

A Series 5000 chip can support up to two SPI slave devices from the serial memory interface: one EEPROM device at CS0~ and one flash device at SDA_CS1~.

Series 5000 devices support 2-byte addressing mode for SPI EEPROM devices, but do not support 3-byte addressing.

The SPI protocol defines four modes of operation; each mode specifies different behavior for flow control on the data bus with respect to the clock signal polarity (CPOL) and phase (CPHA). A Series 5000 device uses SPI Mode 0: CPOL is 0, CPHA is 0, and the SCK line is idle low. For this mode, the Series 5000 chip latches in data on the rising edge of the SCK line, and is output on the falling edge of the SCK line.

A Series 5000 chip runs the SPI protocol from the serial memory interface at 2.5 MHz.

Using both I²C and SPI Memory Devices

Figure 9 on page 28 shows a Series 5000 device that includes both an I²C memory device (a 2 KB EEPROM device) and a SPI memory device (a flash memory device). Because only one device is active at a time, there is no conflict between the two external memory devices.

The serial clock and serial data pins (SCL and SDA_CS1~) are open drain pins, and thus require pull-up resistors. The value of the pull-up resistors depends on the total bus capacitance (number of devices connected to the bus and length of the bus); see the *I2C-bus specification and user manual* (UM10204) from NXP Semiconductor. For example, for a total bus capacitance of 30 pF, you can use a minimum resistance value of 1 kΩ, and a maximum resistance value of 10 kΩ.

Important: If the Series 5000 device includes an I²C EEPROM device with a SPI flash memory device (as shown in **Figure 9**), you must add a 10 kΩ pull-down resistor to pin 46 (MISO). This pull-down resistor is not required if the Series 5000 device includes an SPI EEPROM device (see **Figure 8**).

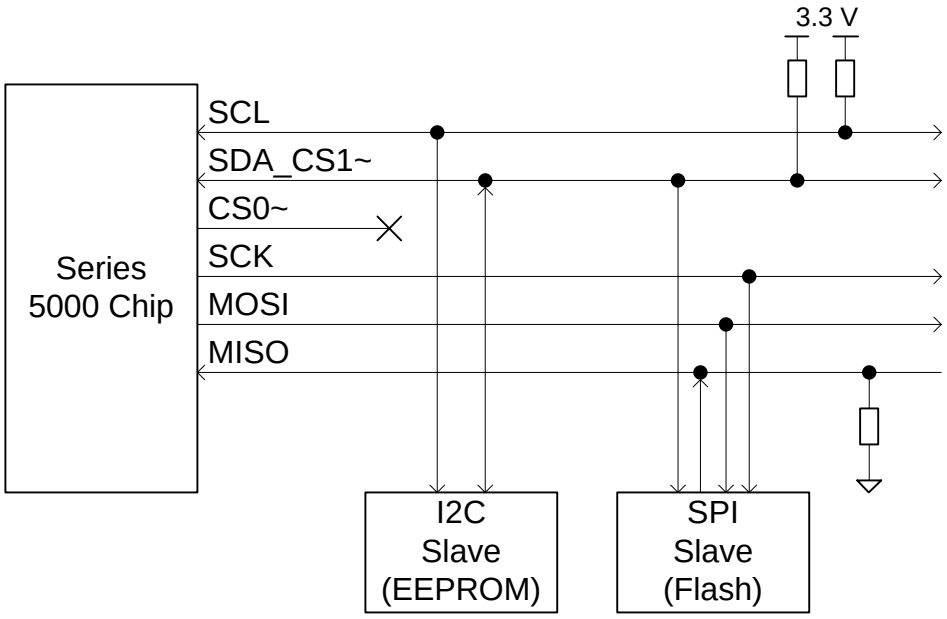


Figure 9. Including both I²C and SPI Memory Devices

Maintaining Non-Volatile Memory Integrity

For most applications, recovering from a low-power event or power outage simply requires a device reset. However, for some applications, ensuring that the non-volatile memory maintains its integrity across a low-power event or power outage is important. Thus, for some applications, it is necessary to ensure that any given NVM write operation completes, regardless of the current state of device power, to guarantee that there is no data corruption. In this case, we consider only EEPROM integrity, because write times are relatively short and cumulative write lifetimes are relatively long.

NVM data integrity depends on both when power begins to drop and on the ramp rate of V_{DD33} during power down. There are two time intervals during which a power outage can occur that have implications for NVM data integrity:

- The Series 5000 chip has sent some, but not all, of the bits of the current byte to the EEPROM device. The Series 5000 chip has not sent stop condition for the byte. The EEPROM latches each bit in internal registers, and waits for the CS or SCK transition to mark the beginning of the internal write cycle. In this case, during device restart, the Neuron firmware will resynchronize the memory interface so that the EEPROM device will discard the incomplete data. If the Neuron firmware can reconstruct the missing data, it will initiate a new NVM write for it.

- The Series 5000 chip has sent all of the bits of the current byte to the EEPROM device, but has not yet sent the stop condition. The EEPROM latches each bit in internal registers, and waits for the CS or SCK transition to mark the beginning of the internal write cycle. In this case, adding a power island to your hardware design to provide enough power to the EEPROM device so that it can complete the write will ensure data integrity.

To ensure NVM data integrity at the byte level, add a power island for the EEPROM device, as shown in **Figure 10**. The power island provides power to the EEPROM device for a short time during a power outage and allows the EEPROM device to complete any write operations that are in progress.

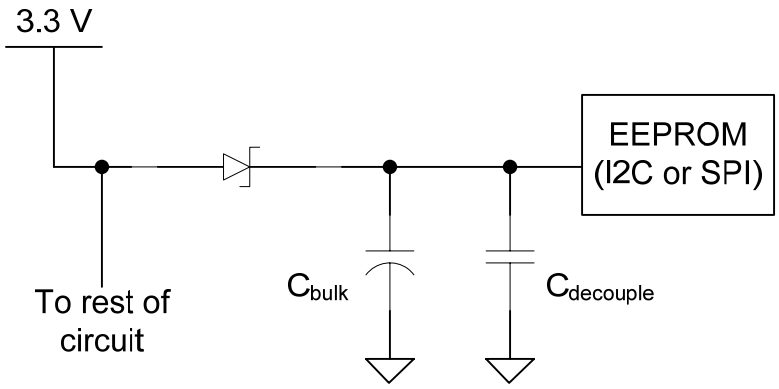


Figure 10. Power Island for EEPROM Device

The main features of the power island are:

- A Schottky diode
- An electrolytic bulk capacitor

The decoupling capacitor shown in **Figure 10** is not part of the power island, but is required for the EEPROM device. A typical decoupling capacitor for an EEPROM device is 0.1 µF, rated for 16 V.

The Schottky diode allows power to flow to the EEPROM device during normal operations, but provides voltage clamping when power is removed (during a power outage) so that the power from the bulk capacitor can flow to the EEPROM device rather than to the rest of the circuit. An example Schottky diode for this application is an On Semiconductor® NSR0230P2T5G Schottky Barrier Diode.

The value of the bulk capacitor depends on the specific EEPROM device. As power drops within the overall circuit, it reaches the low-voltage trip levels for the Series 5000 chip and for the EEPROM device, at which points the chips reset. **Figure 11** on page 30 shows a simple graph of the power drop. The figure assumes a linear power drop. In the figure, the low-voltage trip level for the Series 5000 chip is marked at 2.7 V, at which point the chip resets. The low-voltage trip point for the EEPROM device depends on the specific device; in the figure, it is marked at 1.8 V, but could be as high as 2.5 V.

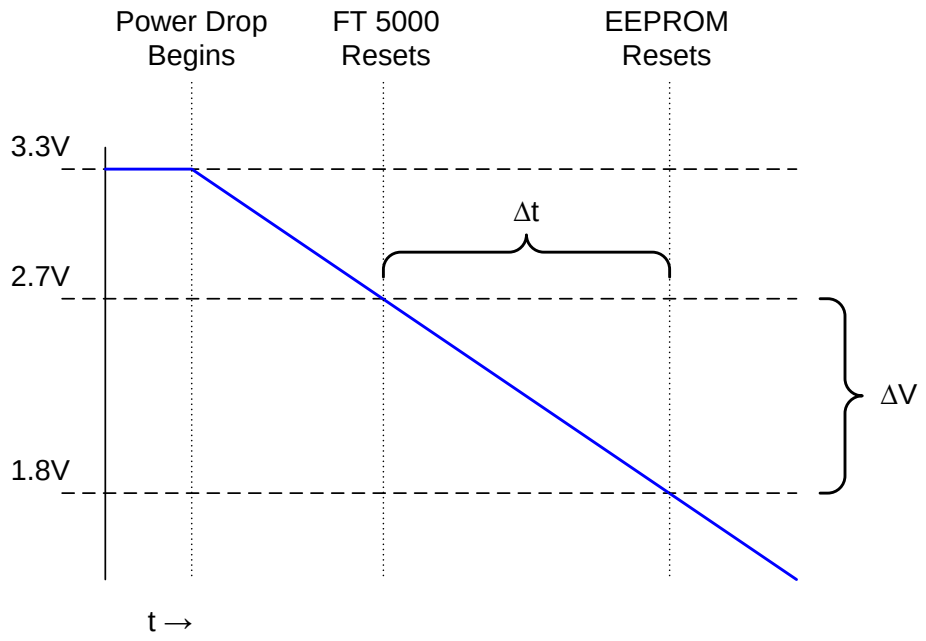


Figure 11. Linear Power Drop for Series 5000 Device

As shown in **Figure 11**, the difference in voltage levels between the Series 5000 chip's low-voltage trip point and the EEPROM device's low-voltage trip point is labeled ΔV. For the figure, ΔV = 0.9 V. The time between the Series 5000 chip's low-voltage trip point and the EEPROM device's low-voltage trip point is labeled Δt. The function of the bulk capacitor in **Figure 10** on page 29 is to ensure that Δt is at least equal to the time required for the EEPROM device to complete a write operation before the voltage level reaches the EEPROM device's low-voltage trip point.

To calculate the required value for the bulk capacitor, use the following formula:

$$C = I\left(\frac{\Delta t}{\Delta V}\right)$$

where:

- I is the operating current for the EEPROM device, typically from 3 to 8 mA. I also includes the reverse leakage current (I_R) for the Schottky diode, which is typically 10 µA.
- Δt is the EEPROM device's write time (t_w), typically 5 ms.
- ΔV is the voltage difference between the Series 5000 chip's low-voltage trip point and the EEPROM device's low-voltage trip point, typically 0.9 V.

Example: Using typical values for I, Δt, and ΔV, the value of C for the bulk capacitor ranges between 17 µF and 44 µF. Using standard electrolytic capacitors, C_{bulk} would be 22 µF or 47 µF.

Device Support

A Series 5000 device supports any EEPROM device that supports the SPI or I²C protocol, and meets the requirements described in *Serial Inter-Integrated Circuit (I2C)* on page 25 or in *Serial Peripheral Interface (SPI)* on page 26.

Echelon has qualified the following SPI flash memory devices for use with a Series 5000 device:

- Atmel® AT25F512B 512-Kilobit 2.7-volt Minimum SPI Serial Flash Memory
- Numonyx™ M25P05-A 512-Kbit, serial flash memory, 50 MHz SPI bus interface
- Silicon Storage Technology SST25VF512A 512 Kbit SPI Serial Flash

Additional devices could be qualified in the future.

The data model that the system flash driver uses assumes direct memory access to the flash device, that is, the driver does not use a flash file system.

Device Programming

You can use any of the following methods to program the external non-volatile memory for a Series 5000 device:

- Program the memory device with a universal programmer, such as one from BPM Microsystems™ or HiLo Systems, before you solder the part to the Series 5000 device PCB
- Program the memory part in-circuit using a serial SPI or I²C programming device, such as the Total Phase™ Aardvark™ I2C/SPI Host Adapter

  For the Aardvark I2C/SPI Host Adapter with the Flash Center Memory Programmer software, you must convert the .NME or .NMF application image file that is generated by the NodeBuilder tool to a .HEX file. In addition, you need to use a byte padding value of "00" (the default padding value used by the Aardvark I2C/SPI Host Adapter is "FF").
- Program the memory part over the LONWORKS network, using a network manager such as the LonMaker® Integration tool or the NodeLoad utility

Clearing the Non-Volatile Memory

In general, if you have a working device, you should not need to clear the external EEPROM non-volatile memory for a Series 5000 chip. For a working device, you can receive a service-pin message and reload the non-volatile memory from the network as needed. However, if it should become necessary to clear the EEPROM non-volatile memory (for example, during device development), perform the following tasks:

1. Press and hold the device's Reset button. If the device does not have a Reset button, connect the **RST~** pin (pin 28) of the Series 5000 chip to GND to hold the chip in the reset state.
2. For I²C EEPROM parts: Temporarily connect the EEPROM's SCL pin to GND.

   For SPI EEPROM parts: Temporarily connect the EEPROM's MISO pin to GND.
3. Release the device's Reset button (or remove the GND connection from the Series 5000 chip's **RST~** pin).
4. Wait a few seconds until the device's Service Pin LED is illuminated (on solid, not flashing). If the device does not have a Service Pin LED, connect a logic analyzer or oscilloscope to the **SVC~** pin (pin 1) of the Series 5000 chip and verify that it reads as logic low, and does not change state.

5. For I²C EEPROM parts: Disconnect the EEPROM's SCL pin from GND.

   For SPI EEPROM parts: Disconnect the EEPROM's MISO pin from GND.

6. Use NodeUtil utility to set the memory configuration and set the state for the device:

   a. Connect the PC that will run the NodeUtil utility to the same network interface that connects to the device. For example, if you connect to the device using **LON1**, connect the NodeUtil utility to **LON1**.

   b. Start the NodeUtil utility.

   c. Press the Service Pin button on the device to send a service-pin message to the NodeUtil utility. If you cannot receive a service-pin message from the device, repeat steps 1 to 5.

   d. Within the NodeUtil utility, select the **L** option to see all connected devices.

   e. Select the **G** option to manage the device that just sent a service-pin message. Typically, this is device 1.

   f. Select **W** to write to a memory location. When prompted, do not update the application checksum and do not update the configuration checksum.

   g. Enter FDE8 for the starting address. Enter one of the following values for address FDE8 to specify the memory type:

      0 for an SPI memory device
      1 for an I²C memory device with 1-byte addressing
      2 for an I²C memory device with 2-byte addressing

      Important: The memory address FDE8 applies to system firmware versions 18 and 19. For later versions of the firmware, this address might change; contact Echelon Support to verify the correct memory address.

   h. Enter a period (.) to exit the memory write session.

   i. Select **W** to write to a different memory location. When prompted, do not update the application checksum and do not update the configuration checksum.

   j. Enter F037 for the starting address. Enter a value of 0 (zero) for address 0xF037. This value triggers device re-initialization.

      Important: The memory address F037 applies to system firmware versions 18 and 19. For later versions of the firmware, this address might change; contact Echelon Support to verify the correct memory address.

   k. Enter a period (.) to exit the memory write session.

   l. Select **E** to exit device management mode.

   m. Select **E** to exit the NodeUtil utility.

Step 6 above writes values to specific bytes of the in-RAM copy of data that is in the EEPROM device. During device re-initialization and reset, the Series 5000 chip reads these bytes and copies the default chip configuration (including memory map and mode table) to the external EEPROM device. After the device completes reset, it is in the applicationless state. If you need to clear additional data within the EEPROM device, use a device programmer, such as the Aardvark I2C/SPI Host Adapter.

At this point, you can reload the device with whatever application is required (for example, a Neuron C application or a ShortStack Micro Server). Because the device has returned to its default (empty) state and default settings, if you use the NodeLoad utility, use the **-X** switch when loading an application or Micro Server image. Do not use the LonMaker Integration Tool to load an image following this procedure.

JTAG Interface

All Series 5000 chips provide an interface for the Institute of Electrical and Electronics Engineers (IEEE) Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990) of the Joint Test Action Group (JTAG) to allow a Series 5000 chip to be included in the boundary-scan chain for device production tests.

You can obtain a Boundary Scan Description Language (BSDL) file from the Echelon Web site:

- www.echelon.com/products/neuron/ for a Neuron 5000 Processor
- www.echelon.com/products/ft5000/ for an FT 5000 Smart Transceiver

The JTAG interface for Series 5000 chips can operate at up to 5 MHz. The JTAG interface includes the following pins:

- **TDI** — Test Data In (pin 21)
  Used to shift in serial test instructions and data. Connect this pin to the TDI signal of a JTAG connector or to the TDO signal of an upstream device in a JTAG chain.
- **TDO** — Test Data Out (pin 22)
  Used to shift out serial test instructions and data. When **TDO** is not being driven by the internal circuitry, the pin is in a high impedance state. Connect this pin to the TDO signal of a JTAG connector or to the TDI signal of a downstream device in a JTAG chain.
- **TCK** — Test Clock (pin 19)
  Provides the clock to run the test access port (TAP) controller state machine, which controls the JTAG data and instruction registers. You can stop the **TCK** signal in either the high or low state, and you can set the clock frequency up to 5 MHz. The **TCK** pin supports hysteresis; the typical hysteresis is approximately 300 mV.
- **TMS** — Test Mode Select (pin 20)
  Controls test operations of the TAP controller. On the falling edge of the **TCK** signal, depending on the state of the **TMS** signal, the TAP controller state machine changes state.
- **TRST~** — Test Reset (pin 17)
  Resets the TAP controller state machine.

These pins comply with the JTAG standard protocol (IEEE 1149.1) for boundary scan operations, and can be used with industry-standard JTAG tools. Each of these pins also includes an internal pull-up resistor, as recommended by the JTAG standard. These pull-ups are only strong enough to pull the input up when the pin is floating, but not strong enough for an external load.

The JTAG interface for Series 5000 chips supports the following JTAG instructions (see the device BSDL file for instruction register codes):

- BYPASS — bypasses the current device (to allow connection to another device in the chain)
  Required by the IEEE 1149.1 standard

- SAMPLE/PRELOAD — samples current values, or preloads known values into the boundary-scan cells for a follow-on operation
  Required by the IEEE 1149.1 standard
- EXTEST — tests the interconnection between two devices
  Required by the IEEE 1149.1 standard
- HIGHZ — sets all digital outputs of the Series 5000 chip to a disabled (high-impedance) state
- IDCODE — returns the Device ID for the chip

The Device ID for an FT 5000 Smart Transceiver is 0x1320062F; the Device ID for a Neuron 5000 Processor is 0x1320162F.

For more information about the JTAG standard, see *IEEE Standard Test Access Port and Boundary-Scan Architecture*, IEEE Std 1149.1-1990 (includes IEEE Std 1149.1a-1993) and *Supplement to IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture*, IEEE Std 1149.1b-1994. These documents are available from the IEEE: www.ieee.org/web/standards/home/index.html.

Operating Conditions

Table 14 describes the standard operating conditions for Series 5000 chips. In the table, all values apply to both the FT 5000 Smart Transceiver and the Neuron 5000 Processor, except the value for I_{DD3-TX}, which applies to the FT 5000 Smart Transceiver only. For a Neuron 5000 Processor, see the specifications for your specific transceiver for transmit current consumption.

Table 14. Series 5000 Chip Operating Conditions

Parameter[1]	Description	Minimum	Typical	Maximum
V_{DD3}	Supply voltage	3.0 V	3.3 V	3.6 V
T_A	Ambient temperature	–40 °C		+85 °C
f_{XIN}	XIN clock frequency[2]		10.0000 MHz	
I_{DD3-RX}	Current consumption in receive mode[3] 5 MHz 10 MHz 20 MHz 40 MHz 80 MHz		 9 mA 9 mA 15 mA 23 mA 38 mA	 15 mA 15 mA 23 mA 33 mA 52 mA
I_{DD3-TX}	Current consumption in transmit mode[3, 4]		I_{DD3-RX} + 15 mA	I_{DD3-RX} + 18 mA

Notes for Table 14:

1. All parameters assume nominal supply voltage (V_{DD3} = 3.3 V) and operating temperature (T_A between -40 °C and +85 °C), unless otherwise noted.

2. See *Clock Requirements* on page 63 for more detailed information about the XIN clock frequency.
3. Assumes no load on digital I/O pins, and that the I/O lines are not switching.

   To calculate the I_{DD3} current for each switching output, use the following formula:

   $$I_{DD3\_pin} = ((12 \times 10^{-12}) + C_{L\_pin}) \times V_S \times f_{pin}$$

   where $12x10^{-12}$ is the effective on-chip capacitance, C_{L_pin} is the load capacitance of the I/O pin, V_S is the supply voltage, and f_{pin} is the frequency at which the pin switches.

   For example, a pin with 27 pF external load switching at 1 MHz would have a total switching current of I_{DD3} = (12pF + 27pF) * 3.6V * 10^6Hz = 140 µA.

   To calculate the total I_{DD3} current, sum the I_{DD3} calculations for each pin:

   $$I_{DD3\_total} = \sum_{1}^{N} I_{DD3\_pin\_N}$$

   Any DC loads, such as LEDs or resistors, should also be added.
4. Current consumption in transmit mode represents a peak value rather than a continuous usage value because a Series 5000 device does not typically transmit data continuously.

Table 15 describes the absolute maximum conditions for Series 5000 chips. Absolute maximum ratings are limits beyond which the device might become damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Table 15. Series 5000 Chip Absolute Maximum Ratings

Parameter	Description	Minimum	Maximum
V_{DD3}	Supply voltage	–0.3 V	+3.7 V
$V_{i\text{-}digitalIn}$	Input voltage – digital I/O pins	–0.3 V	+5.5 V
$V_{i\text{-}digitalOut}$	Output voltage – digital I/O pins	–0.3 V	V_{DD3} + 0.3 V
$V_{i\text{-}other}$	Input voltage – other non-power pins	–0.3 V	V_{DD3} + 0.3 V
I_i	Input current – all non-power pins	–10 mA	+10 mA
$T_{storage}$	Storage temperature	–55 ºC	+125 ºC

All input and output pins can withstand 100 mA forced into or out of the pin without latch-up. See *Avoidance of Damaging Conditions* on page 151 for more information about latch-up.

Pin Assignments

Although the pin assignments for the Neuron 5000 Processor and the FT 5000 Smart Transceiver are very similar, there are a few differences, as described in the following sections.

All pins can withstand 2 kV Electrostatic Discharge (ESD) voltage, as tested according to MIL-STD-883 Method 3015.7.

Figure 12 shows the pinout for the FT 5000 Smart Transceiver. The central rectangle in the figure represents the bottom pad (pin 49), which must be connected to ground.

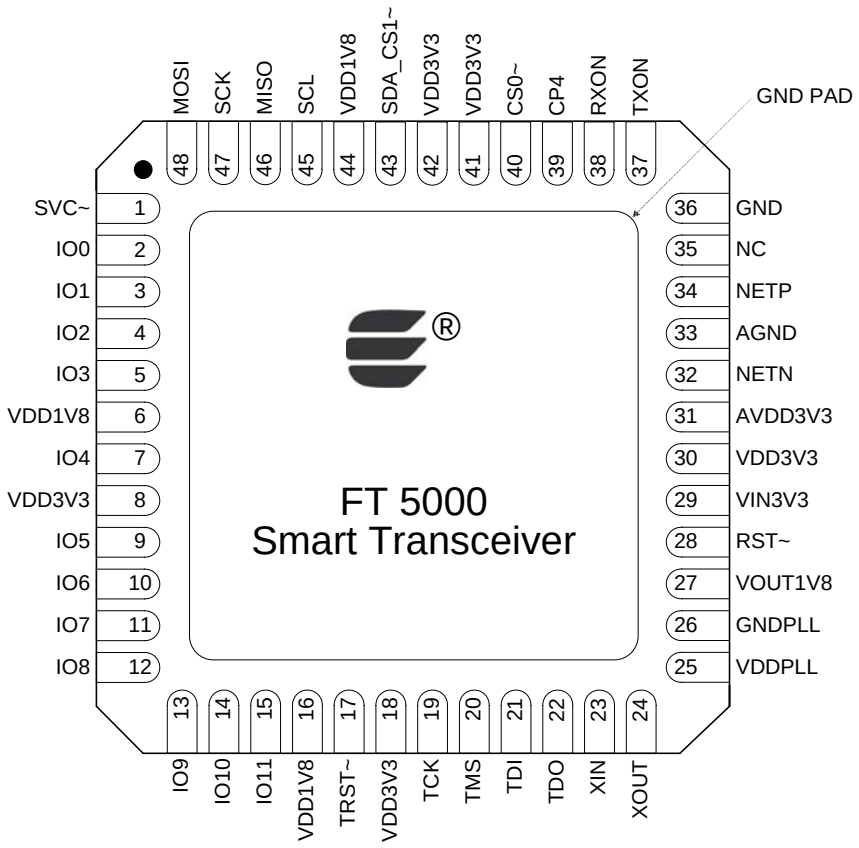


Figure 12. FT 5000 Smart Transceiver Chip Pinout Diagram

Table 16 on page 37 lists the pin assignments for the FT 5000 Smart Transceiver. All digital inputs are low-voltage transistor-transistor logic (LVTTL) compatible, 5 V tolerant, with low leakage. All digital outputs are slew-rate limited to reduce Electromagnetic Interference (EMI) concerns.

Table 16. FT 5000 Smart Transceiver Pin Assignments

Name	Pin Number	Type	Description
SVC~	1	Digital I/O	Service (active low)
IO0	2	Digital I/O	IO0 for I/O Objects
IO1	3	Digital I/O	IO1 for I/O Objects
IO2	4	Digital I/O	IO2 for I/O Objects
IO3	5	Digital I/O	IO3 for I/O Objects
VDD1V8	6	Power	1.8 V Power Input (from internal voltage regulator)
IO4	7	Digital I/O	IO4 for I/O Objects
VDD3V3	8	Power	3.3 V Power
IO5	9	Digital I/O	IO5 for I/O Objects
IO6	10	Digital I/O	IO6 for I/O Objects
IO7	11	Digital I/O	IO7 for I/O Objects
IO8	12	Digital I/O	IO8 for I/O Objects
IO9	13	Digital I/O	IO9 for I/O Objects
IO10	14	Digital I/O	IO10 for I/O Objects
IO11	15	Digital I/O	IO11 for I/O Objects
VDD1V8	16	Power	1.8 V Power Input (from internal voltage regulator)
TRST~	17	Digital Input	JTAG Test Reset (active low)
VDD3V3	18	Power	3.3 V Power
TCK	19	Digital Input	JTAG Test Clock
TMS	20	Digital Input	JTAG Test Mode Select
TDI	21	Digital Input	JTAG Test Data In
TDO	22	Digital Output	JTAG Test Data Out
XIN	23	Oscillator In	Crystal oscillator input
XOUT	24	Oscillator Out	Crystal oscillator output
VDDPLL	25	Power	1.8 V Power Input (from internal voltage regulator)
GNDPLL	26	Power	Ground
VOUT1V8	27	Power	1.8 V Power Output (of internal voltage regulator)
RST~	28	Digital I/O	Reset (active low)

Name	Pin Number	Type	Description
VIN3V3	29	Power	3.3 V input to internal voltage regulator
VDD3V3	30	Power	3.3 V Power
AVDD3V3	31	Power	3.3 V Power
NETN	32	Comm	Network Port (polarity insensitive)
AGND	33	Ground	Ground
NETP	34	Comm	Network Port (polarity insensitive)
NC	35	N/A	Do Not Connect
GND	36	Ground	Ground
TXON	37	Digital I/O	TxActive for optional network activity LED
RXON	38	Digital I/O	RxActive for optional network activity LED
CP4	39	Digital I/O	Connect to V_{DD33} through a 4.99 kΩ pullup resistor
CS0~	40	Digital I/O for Memory	SPI slave select 0 (active low)
VDD3V3	41	Power	3.3 V Power
VDD3V3	42	Power	3.3 V Power
SDA_CS1~	43	Digital I/O for Memory	I^2C: serial data SPI: slave select 1 (active low)
VDD1V8	44	Power	1.8 V Power Input (from internal voltage regulator)
SCL	45	Digital I/O for Memory	I^2C serial clock
MISO	46	Digital I/O for Memory	SPI master input, slave output (MISO)
SCK	47	Digital I/O for Memory	SPI serial clock
MOSI	48	Digital I/O for Memory	SPI master output, slave input (MOSI)
PAD	49	Ground Pad	Ground

Neuron 5000 Processor

Figure 13 on page 39 shows the pinout for the Neuron 5000 Processor. The central rectangle in the figure represents the bottom pad (pin 49), which must be connected to ground.

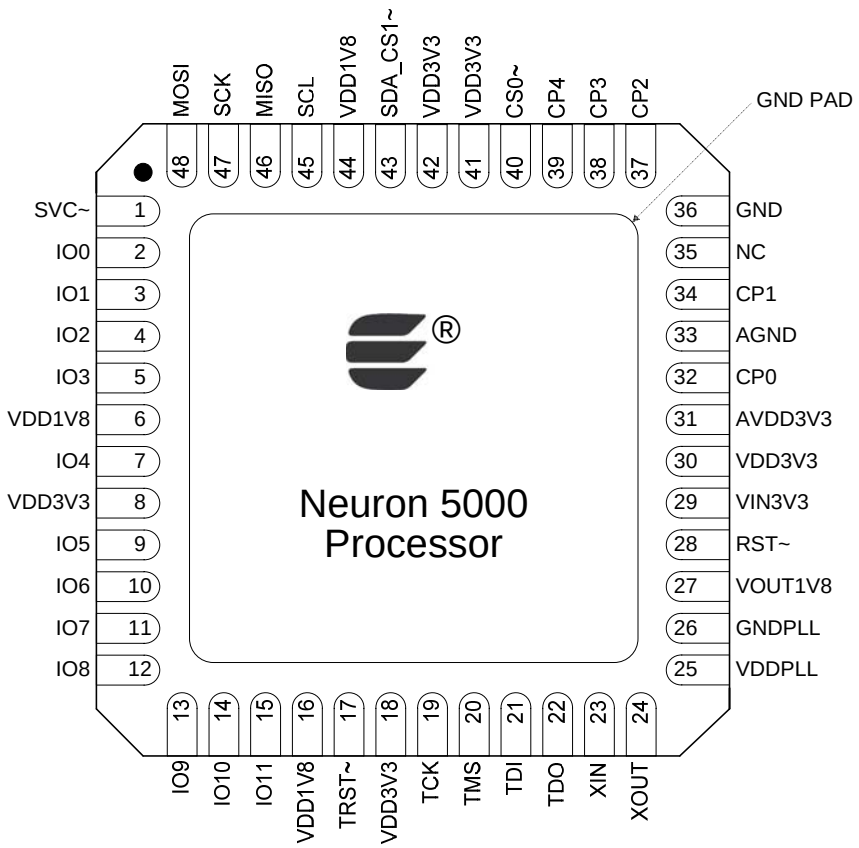


Figure 13. Neuron 5000 Processor Pinout Diagram

Table 17 lists the pin assignments for the Neuron 5000 Processor. All digital inputs are low-voltage transistor-transistor logic (LVTTL) compatible, 5 V tolerant, with low leakage. All digital outputs are slew-rate limited to reduce Electromagnetic Interference (EMI) concerns.

Table 17. Neuron 5000 Processor Pin Assignments

Name	Pin Number	Type	Description
SVC~	1	Digital I/O	Service (active low)
IO0	2	Digital I/O	IO0 for I/O Objects
IO1	3	Digital I/O	IO1 for I/O Objects
IO2	4	Digital I/O	IO2 for I/O Objects
IO3	5	Digital I/O	IO3 for I/O Objects
VDD1V8	6	Power	1.8 V Power Input (from internal voltage regulator)
IO4	7	Digital I/O	IO4 for I/O Objects
VDD3V3	8	Power	3.3 V Power
IO5	9	Digital I/O	IO5 for I/O Objects

Name	Pin Number	Type	Description
IO6	10	Digital I/O	IO6 for I/O Objects
IO7	11	Digital I/O	IO7 for I/O Objects
IO8	12	Digital I/O	IO8 for I/O Objects
IO9	13	Digital I/O	IO9 for I/O Objects
IO10	14	Digital I/O	IO10 for I/O Objects
IO11	15	Digital I/O	IO11 for I/O Objects
VDD1V8	16	Power	1.8 V Power Input (from internal voltage regulator)
TRST~	17	Digital Input	JTAG Test Reset (active low)
VDD3V3	18	Power	3.3 V Power
TCK	19	Digital Input	JTAG Test Clock
TMS	20	Digital Input	JTAG Test Mode Select
TDI	21	Digital Input	JTAG Test Data In
TDO	22	Digital Output	JTAG Test Data Out
XIN	23	Oscillator In	Crystal oscillator input
XOUT	24	Oscillator Out	Crystal oscillator output
VDDPLL	25	Power	1.8 V Power Input (from internal voltage regulator)
GNDPLL	26	Power	Ground
VOUT1V8	27	Power	1.8 V Power Output (of internal voltage regulator)
RST~	28	Digital I/O	Reset (active low)
VIN3V3	29	Power	3.3 V Power Input
VDD3V3	30	Power	3.3 V Power
AVDD3V3	31	Power	3.3 V Power
CP0	32	Comm	Single-Ended Mode: Receive serial data Special-Purpose Mode: Receive serial data
AGND	33	Ground	Ground
CP1	34	Comm	Single-Ended Mode: Transmit serial data Special-Purpose Mode: Transmit serial data
NC	35	N/A	Do Not Connect
GND	36	Ground	Ground
CP2	37	Comm	Single-Ended Mode: External transceiver enable Special-Purpose Mode: Bit clock

Name	Pin Number	Type	Description
CP3	38	Comm	Do Not Connect
CP4	39	Comm	Single-Ended Mode: Collision detect Special-Purpose Mode: Frame clock
CS0~	40	Digital I/O for Memory	SPI slave select 0 (active low)
VDD3V3	41	Power	3.3 V Power
VDD3V3	42	Power	3.3 V Power
SDA_CS1~	43	Digital I/O for Memory	I^2C: serial data SPI: slave select 1 (active low)
VDD1V8	44	Power	1.8 V Power Input (from internal voltage regulator)
SCL	45	Digital I/O for Memory	I^2C serial clock
MISO	46	Digital I/O for Memory	SPI master input, slave output (MISO)
SCK	47	Digital I/O for Memory	SPI serial clock
MOSI	48	Digital I/O for Memory	SPI master output, slave input (MOSI)
PAD	49	Ground Pad	Ground

Pin Connections

This section describes the electrical connections for the various pins on a Series 5000 chip. Unless specified otherwise, the connections apply to both the FT 5000 Smart Transceiver and the Neuron 5000 Processor.

See Appendix E, *Example Schematic*, on page 163, for a more complete example schematic for an FT 5000 Smart Transceiver.

Connect the **VDD3V3** pins (8, 18, 29, 30, 41, and 42) to V_{DD33}. Also connect the **AVDD3V3** pin (31) to an analog V_{DD33} source, if different from the digital V_{DD33} source. In general, the **VDD3V3** pins and the **AVDD3V3** pin connect to the same V_{DD33} source. In addition, connect decoupling capacitors to the **VDD3V3** pins, as shown in **Figure 14** on page 42.

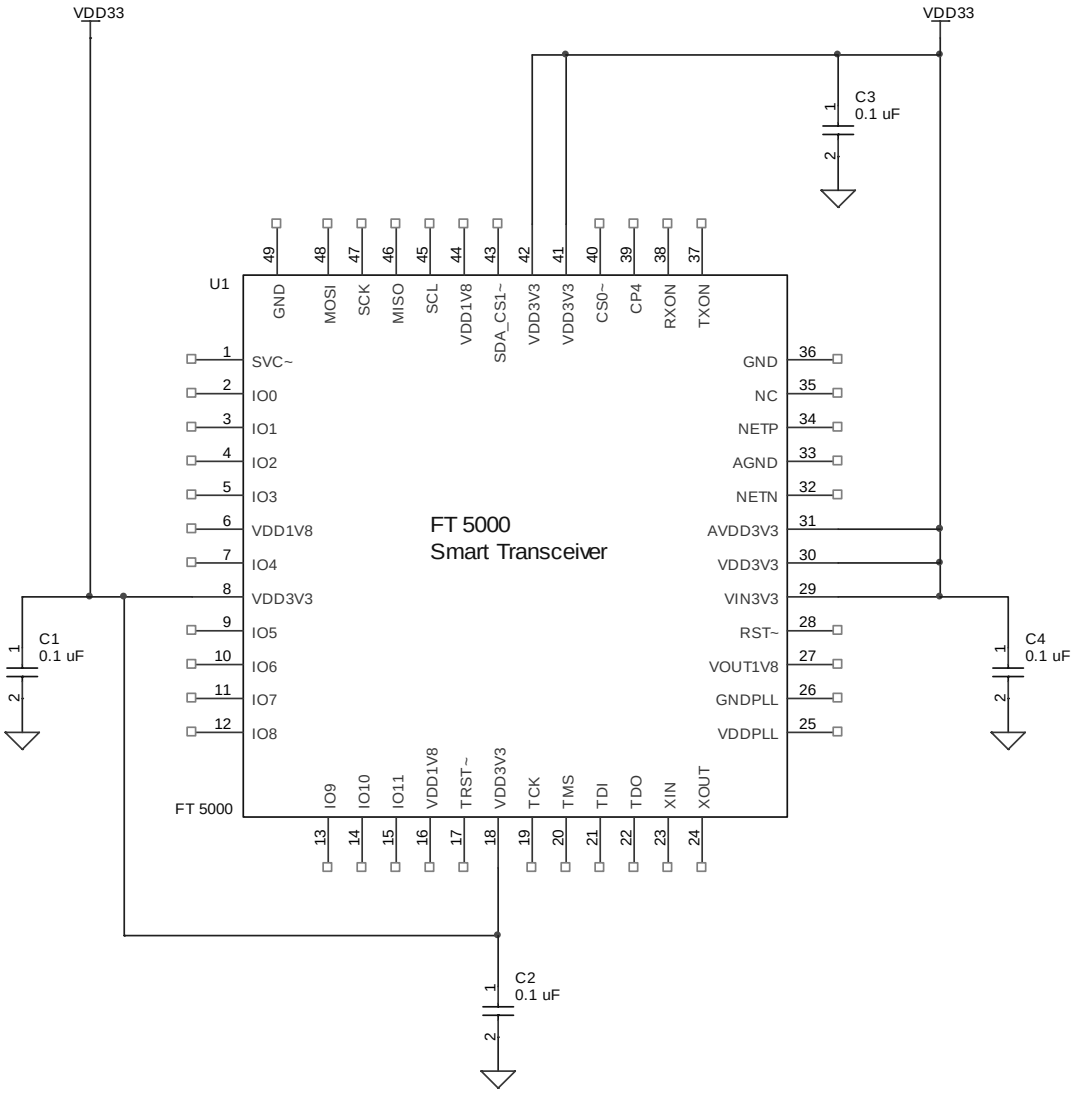


Figure 14. Connections for the VDD33 Pins

In the figure, the capacitors are:

- **C1-C4**: 0.1 µF Ceramic

The **VOUT1V8** pin (27) is the output of the on-chip voltage regulator. Connect the **VDD1V8** pins (6, 16, and 44) to the **VOUT1V8** pin (27) to connect the 1.8 V input pins to the output of the internal voltage regulator, as shown in **Figure 15** on page 43. Connect a bulk decoupling capacitor (**C5** in **Figure 15**) near the **VOUT1V8** pin (27), in addition to the other decoupling capacitor.

Important: Do not connect an external 1.8 V source to any of the **VDD1V8** pins (6, 16, and 44). Connect these pins to the **VOUT1V8** pin (27) only. **Using an external 1.8 V source voids the warranty for the chip, and can cause unpredictable and possibly irreparable results.**

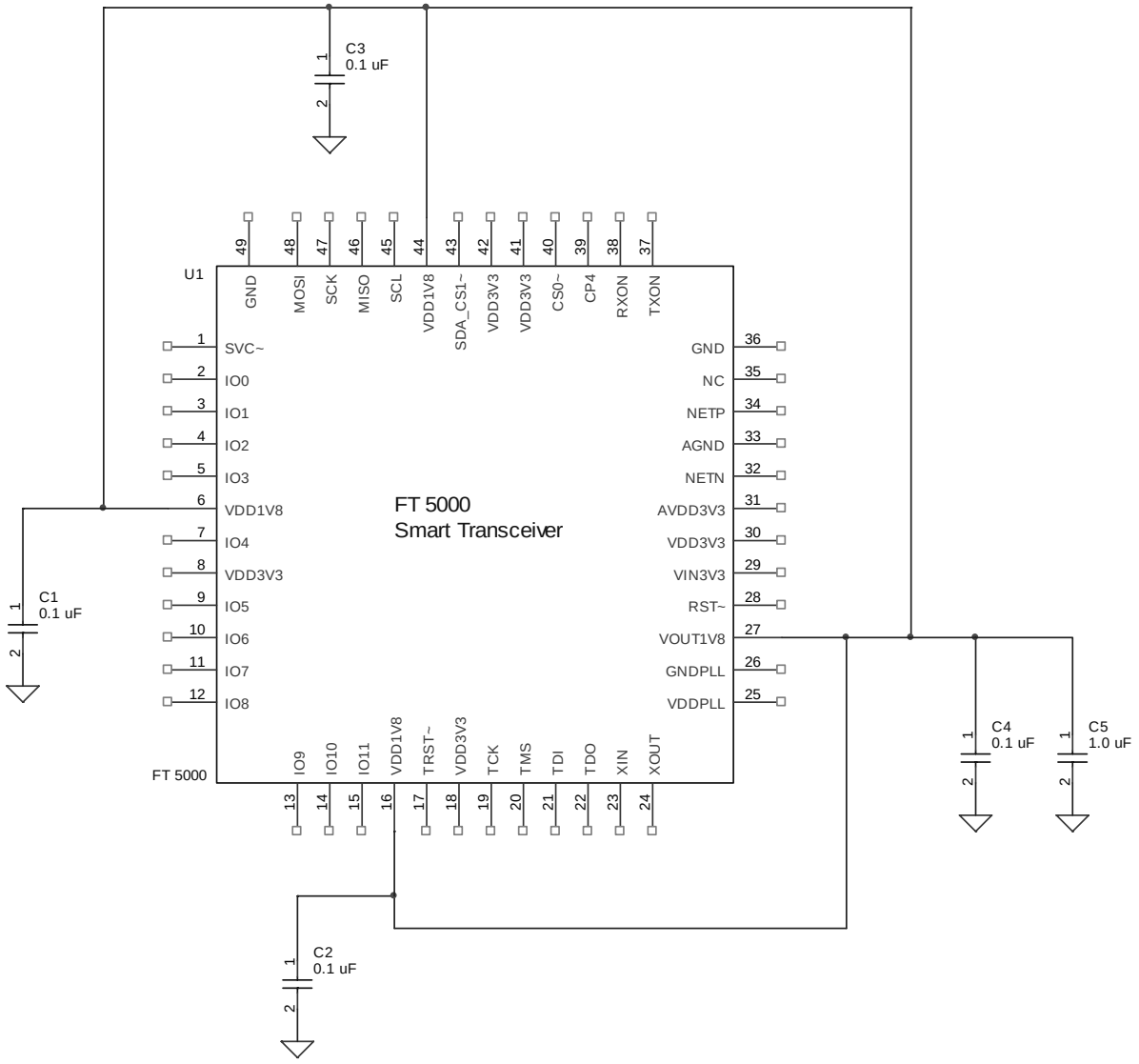


Figure 15. Connections for the VDD18 Pins

In the figure, the capacitors are:

- **C1-C4**: 0.1 µF Ceramic
- **C5**: 1.0 µF Ceramic

Connect the chip's pad (pin 49) to logic ground. Also connect the **AGND** pin (33) to logic ground. **Figure 16** on page 44 shows the connections for the ground pins.

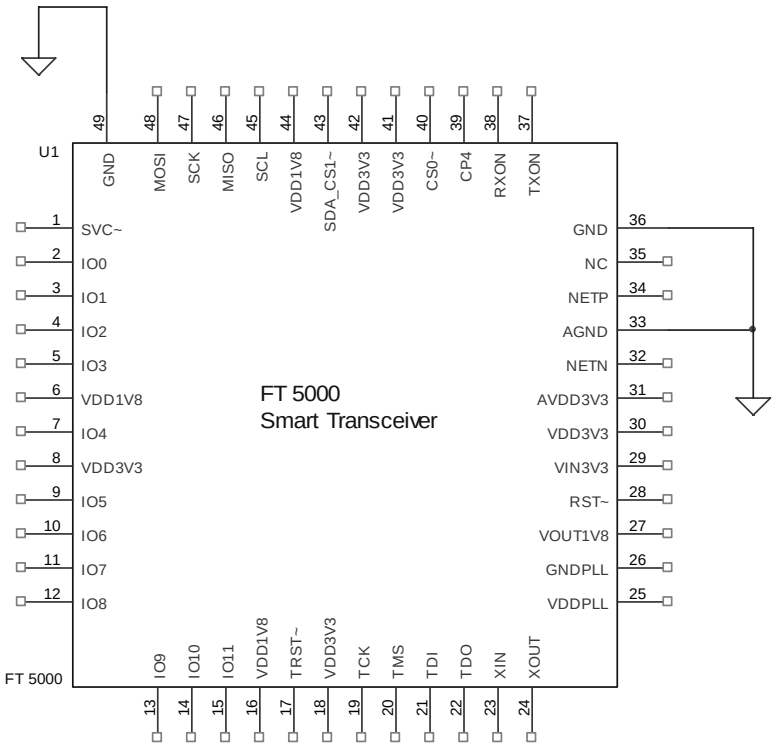


Figure 16. Connections for the Ground Pins

Connect the **VDDPLL** pin (25) to the **VOUT1V8** pin (27), with an associated chip ferrite bead, as shown in **Figure 17**. Connect the **GNDPLL** pin (26) to GND, with an associated chip ferrite bead. In addition, add stabilizing capacitors across the VDDPLL and GNDPLL pins. Place each capacitor directly adjacent to the PLL pins, on the top layer of the PCB.

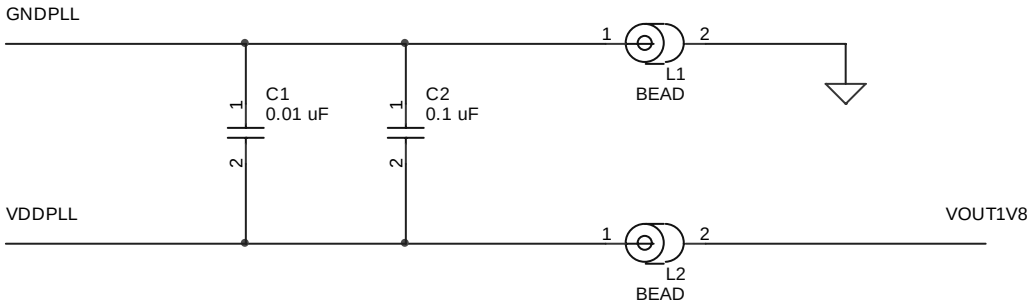


Figure 17. Connections for the PLL Pins

In the figure, the capacitors are:

- **C1**: 0.01 µF Ceramic
- **C2**: 0.1 µF Ceramic

The chip ferrite beads should be rated for ≥50 mA saturation current, provide ≥120 Ω impedance at 100 MHz per 20 ºC, and have a DC resistance ≤1 Ω. An example part is the Laird Technologies® LI0603E151R-10 part (formerly a Steward part).

Connect a 1 to 10 kΩ pull-up resistor to the JTAG **TCK** pin (19), as shown in **Figure 18** on page 45.

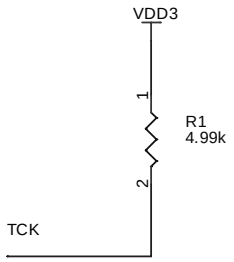


Figure 18. Connection for the JTAG TCK Pin

Characteristics of the Digital Pins

Series 5000 chips provide 12 bidirectional I/O pins that are usable in several different configurations. These pins provide flexible interfacing to external hardware and access to the internal timer/counters. In addition to reading the input pins, the application processor can read the current logic level of the output pins.

The digital I/O pins (**IO0** – **IO11**) have LVTTL-level inputs. Pins **IO0** – **IO7** also have low-level-detect latches. The **RST~** and **SVC~** pins have internal pull-ups, and the **RST~** pin has hysteresis.

See the *I/O Model Reference for Smart Transceivers and Neuron Chips* for more information about how to use the digital I/O pins.

Table 18 lists the characteristics of the digital I/O pins, which include the IO0 – IO11 pins, the memory I/O pins, the Neuron 5000 CP0 – CP4 pins, and the other digital pins listed in **Table 16** and **Table 17**.

Table 18. Series 5000 Chip Digital Pin Characteristics

Parameter[1]	Description	Minimum	Typical	Maximum
V_{OH}	Output drive high at I_{OH} = 8 mA	2.4 V	—	V_{DD3}
V_{OL}	Output drive low at I_{OL} = 8 mA	GND	—	0.4 V
V_{IH}	Input high level	2.0 V	—	5.5 V
V_{IL}	Input low level	GND	—	0.8 V
V_{HYS}	Input hysteresis for **RST~** pin and **TCK** pin	—	300 mV	—
I_{IN}	Input leakage current	—	—	10 µA
R_{PU}	Pullup resistance[2]	13 kΩ	—	23 kΩ
I_{PU}	Pullup current when pin at 0 V[2]	130 µA	—	275 µA

Notes:

1. All parameters assume nominal supply voltage (V_{DD3} = 3.3 V) and operating temperature (T_A between –40 ºC and +85 ºC), unless otherwise noted.
2. Applies to **RST~** and **SVC~** pins only.

Communications Port (CP) Pins for the Neuron 5000 Processor

The Neuron 5000 Processor has a very versatile communications port. It consists of five pins (named CP0 through CP4) that can be configured to interface to a wide variety of media interfaces (network transceivers) and operates over a wide range of data rates.

The communications port can be configured to operate in one of two modes: single-ended mode or special-purpose mode. **Table 19** lists the pin assignments for the communications port pins for each of the modes, and **Figure 19** on page 47 shows a block diagram of the communications port.

Table 19. Communications Port Pin Assignments

Pin	Drive Current	Single-Ended Mode (3.3 V)	Special-Purpose Mode (3.3 V)	Connect To
CP0	N/A	Data input	Rx input	Transceiver RXD
CP1	8 mA	Data output	Tx output	Transceiver TXD
CP2	8 mA	Transmit Enable output	Bit Clock output	Transmit Enable (single ended mode) Bit Clock (special-purpose mode)
CP3	N/A	Do Not Connect		
CP4	8 mA	Collision Detect input	Frame Clock output	Collision Detect (single ended mode) Frame Clock (special-purpose mode)

Before programming, a Neuron 5000 Processor uses its default communications parameters, which define a simplified single-ended mode 78 kbps channel. The default communications parameters allow you to load an application image over a 78 kbps network, for example during device manufacturing. Devices that use a 78 kbps transceiver (such as a 78 kbps EIA-485 transceiver or an LPT-11 Link Power Transceiver) can use the default communications parameters within development or manufacturing test networks. For production networks (networks with many devices), you should ensure that each device has communications parameters defined for the channel; use the NodeBuilder FX Development Tool or the Mini FX Evaluation Kit to develop applications with the correct communications parameters. Note that devices defined for a TP/XF-1250 channel cannot use the default communications parameters; each device's external serial non-volatile memory must be loaded with the correct communications parameters before connecting to the network.

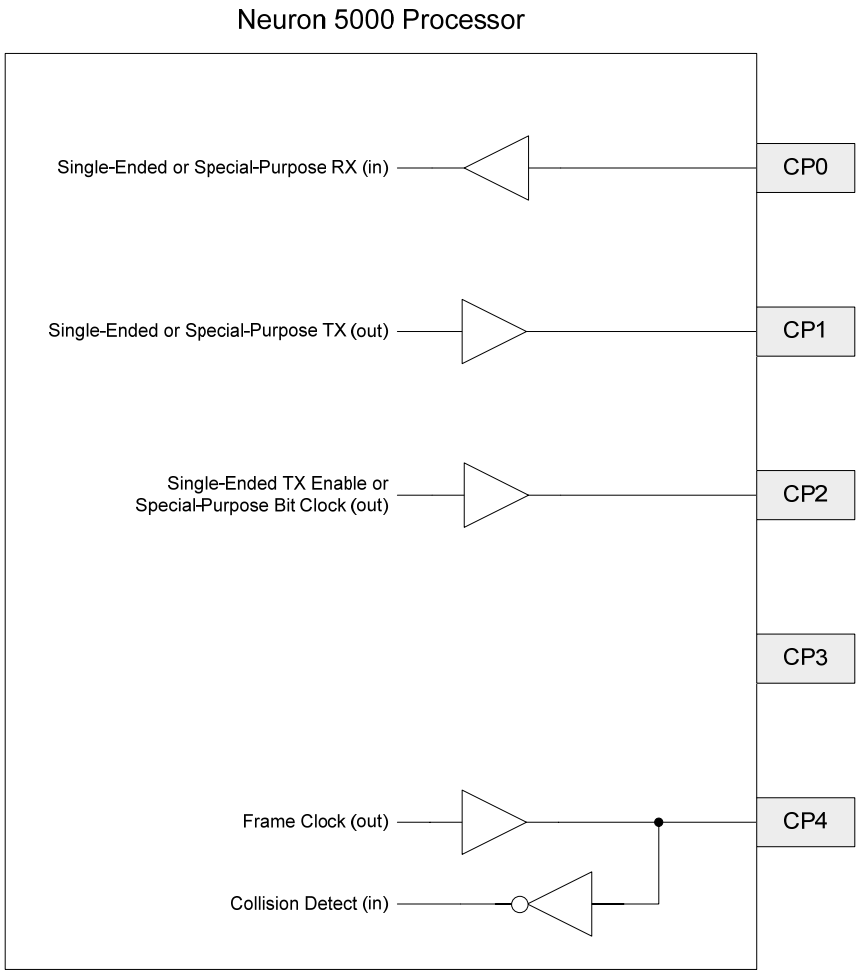


Figure 19. Internal Transceiver Block Diagram

Single-ended mode uses Differential Manchester encoding (also known as bi-phase space encoding), which is a widely used and reliable format for transmitting data over various media. This encoding scheme provides a transition at the beginning of every bit period to synchronize the receiver clock (referred to as the *clock transition*). The data is indicated by the presence or absence of a second transition (the *data transition*) halfway between clock transitions. A mid-cell transition indicates a zero. Lack of a mid-cell transition indicates a one.

The transmitter transmits a *preamble* at the beginning of a packet to allow the other devices to synchronize their receiver clocks. The preamble consists of a bit-sync field and a byte-sync field. The bit-sync field is a series of Differential Manchester ones; its duration is user selectable, and is at least four bits long. The byte-sync field is a single bit Differential Manchester zero that marks the end of the preamble, and the beginning of the first data byte of the packet.

The Neuron Chip terminates the packet by forcing a Differential Manchester code violation, that is, the Neuron Chip holds the data output transitionless long enough for the receiver to recognize an invalid code that signals the end of transmission. The data output can be either high or low for the duration of the line-code violation, depending on the state of the data output after transmitting the last bit. The line-code violation begins after the end of the last CRC bit, and lasts for at least 2.5 bit times. The last bit does not have a trailing clock edge.

The Transmit Enable pin is held active until the end of the line-code violation, and is then released.

Differential Manchester coding is polarity-insensitive. Thus, reversal of polarity in the communication link does not affect data reception.

A Neuron Chip in single-ended mode supports any of the following network bit rates:

- 2.5 Mbps
- 1.25 Mbps
- 625 kbps
- 312.5 kbps
- 156 kbps
- 78 kbps
- 39 kbps
- 19.5 kbps
- 9.6 kbps
- 4.8 kbps

The 1.25 Mbps and lower bit rates are available for any of the system-clock rates of the Neuron 5000 Processor. The 2.5 Mbps bit rate requires the Neuron 5000 Processor's system clock to be set at 20 MHz or higher.

Single-Ended Mode

Single-ended mode (3.3 V) is most commonly used with external active transceivers that interface to media such as RF, IR, fiber optics, twisted-pair cable, and coaxial cable. **Figure 20** on page 49 shows the communications port configuration for single-ended mode operation. Data communication occurs through the single-ended (with respect to GND) input and output buffers on pins CP0 and CP1.

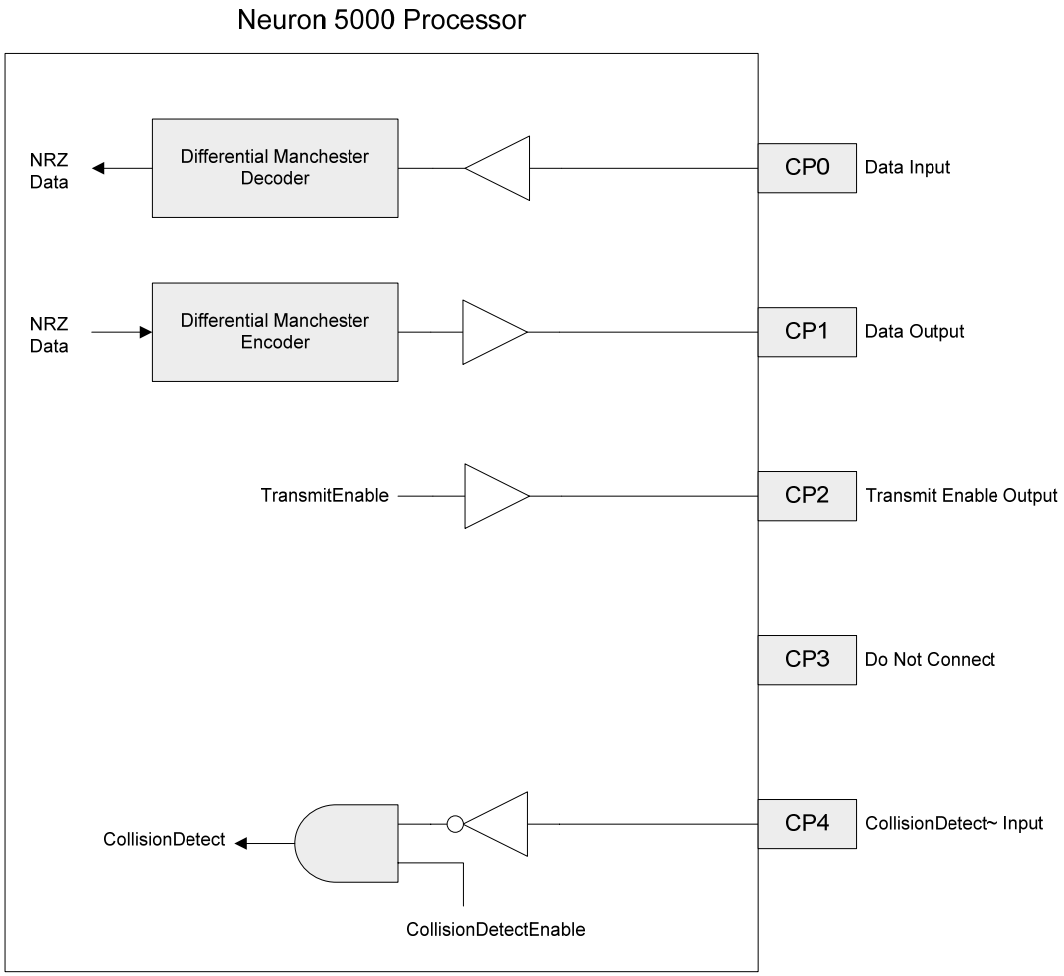


Figure 20. Single-Ended Mode Configuration

Figure 21 shows a typical packet, where T is the bit period, equal to 1/(bit rate). Clock transitions occur at the beginning of a bit period, and therefore, the last valid bit in the packet does not have a trailing clock edge.

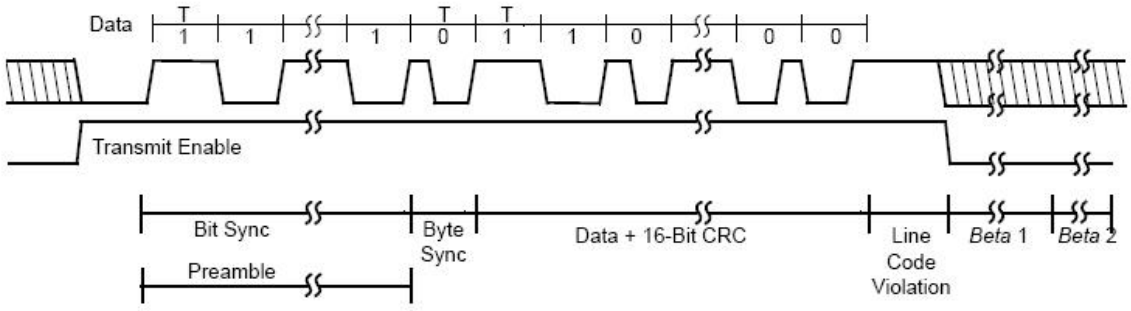


Figure 21. Single-Ended Mode Data Format

Before beginning to transmit the packet, the Neuron Chip initializes the output data pin to start low. It then asserts the Transmit Enable pin (CP2) to ensure that the first transition in the packet is from low to high. This first transition occurs within 1 bit time of asserting Transmit Enable, and marks the beginning of the packet.

Important: Transmit Enable is actively driven at all times in single-ended mode. In single-ended mode, the 8 mA driver is connected to CP1 and it is not high impedance when receiving packets.

At the end of the packet after the Differential Manchester code violation, the Transmit Enable pin on CP2 is driven low to indicate the end of transmission.

Collision Detection for Single-Ended Mode

As an option, the Neuron Chip accepts an active-low Collision Detect input from the transceiver. If collision detection is enabled, and CP4 goes low for at least one system clock period (12.5 ns with an 80 MHz system clock) during transmission, the Neuron Chip is signaled that a collision has occurred (or is occurring) and that the message must be sent again. The device then attempts to reaccess the channel.

The collision detect flag is checked by firmware at the end of the preamble and end of packet. If the node does not use collision detection, the only way that it can determine that a message has not been received is to request an acknowledgment. When acknowledged service is used, the retry timer is set to allow sufficient time for a message to be sent and acknowledged (typically 48 ms to 96 ms at 1.25 Mbps when there are no routers in the transmission path). If the retry timer times out, the device attempts to reaccess the channel. The benefit of using collision detection is that the device does not have to wait for the retry timer to time-out before attempting to resend the message, because the device detects the collision when it sends the packet.

Beta 1 and Beta 2 Timeslots in Single-Ended Mode

Important: The information in this section applies only to development of new network types. If you use a standard LONMARK channel in a LONWORKS network, you do not need to work with the Beta 1 and Beta 2 timeslots.

The idle period between packets comprises the *Beta 1* and *Beta 2* timeslots. The *Beta 1* time is the fixed component in the idle period after a packet has been sent. This component is a function of the following:

- Oscillator frequencies and accuracies on the various network devices.
- Media indeterminate time — that time following packet transmission when the network can appear to be busy due to ringing on the line.
- Minimum interpacket gap — transceiver-dependent timing requirements.
- Receive-end delay — skew between the transmitter Neuron Chip's and the receiver Neuron Chip's view of the end of the packet. This skew can occur because of buffering in the transceivers, and is typically found in special-purpose mode transceivers.

The Media Access Control (MAC) Layer timings are a function of five parameters stored in the configuration data. These parameters determine the Preamble Length, the Packet Cycle, the Beta 2 Slot Width, the Transmit Interpacket Padding, and the Receive Interpacket Padding.

All timings are given in terms of the Neuron Chip processor cycles. One cycle is 37.5 ns at 80 MHz, 75 ns at 40 MHz, 150 ns at 20 MHz, 0.3 μs at 10 MHz, and 0.6 μs at 5 MHz:

- Beta 1 Time after Transmission = 583 cycles + Transmit Interpacket Padding + Beta 2 Slot Width
- Beta 1 Time after Reception = 565 cycles + Receive Interpacket Padding + Beta 2 Slot Width

An indeterminate time is defined during the Beta 1 period in which all transitions on the channel are ignored. This period starts following the end of any packet (transmitted or received). Its duration is defined as follows:

- Indeterminate Time after transmission = 313 cycles + Transmit Interpacket Padding
- Indeterminate Time after reception = 295 cycles + Receive Interpacket Padding

Both priority (P) and non-priority slots are defined by the *Beta 2* time. Devices listen to the network prior to transmitting a packet. This prevents devices from transmitting packets on top of each other except when the packets are initiated at nearly the same time. In addition, devices randomize the time before they start transmitting on the network. When the network is idle, all nodes randomize over 16 slots. As the estimated network load increases, devices start randomizing over more slots to lower the probability of a collision. The number of randomizing slots (R) varies from 16 up to 1008, based on "n," the estimated channel backlog (the number of slots is n • 16 where "n" has a range of 1 to 63), as shown in **Figure 22**.

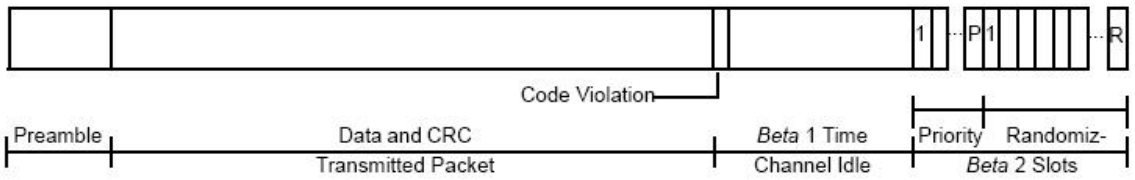


Figure 22. Packet Timing

Following a packet, and prior to randomizing, devices wait for a configurable number of priority slots to pass. Devices with priority packets and a configured priority slot transmit in a priority slot. Use of priority substantially reduces the probability of collision. The number of priority slots (P) is fixed for a given channel and can range from 0 to 127.

The Beta 2 time is defined by the following:

- Oscillator frequencies and accuracies on the various network devices.
- Number of priority slots on the channel.
- Receive start delay — the time from when a device starts transmitting to when the receiving device detect the start of transmission. This delay is a function of the receive-to-transmit turnaround time of the transceiver, the bit rate and length of the media, delay through the receiver, and initial preamble bits lost.
- For special-purpose mode transceivers, framing delays between the Neuron Chip and the transceiver.

For the receiver to detect the edge transitions, two windows are set up for each bit period, T. The first window is set at T/2 and determines if a zero is being received. The second window is at T and defines a one. This transition then sets up the next two windows (T/2 and T). If no transition occurs, a Differential Manchester code violation is detected and the packet is assumed to have ended.

Table 20 on page 52 shows the width of this window. If a transition falls outside of either window, it is not detected. Timing instability of the transitions, known as jitter, can be caused by changes in the communications medium, or instability in the transmitting or

receiving device's input clocks. The jitter tolerance windows are expressed as fractions of the bit period, T.

Table 20. Receiver Jitter Tolerance Windows

Next Data Edge (Nominal)	Next Clock Edge (Nominal)	Line Code Violation to Receive (Minimum)
0.500T	1.000T	1.46T

For the receiver to reliably terminate reception of a packet, the received line-code violation period must have no transitions until the Neuron Chip detects the end of the packet. The receiving Neuron Chip terminates a packet if no clock transitions are detected after the last bit. **Table 20** shows the minimum duration from the last clock edge to where the Neuron Chip is guaranteed to recognize the line-code violation. Data transitions are allowed in this period (and must fall within the data window).

For a Neuron Chip, the time from when an application software call is issued to send a 12-byte message to when the packet is sent is approximately 175 µs for an 80 MHz system clock (the time varies inversely with the system clock rate).

Special-Purpose Mode

In special situations, it is desirable for the Neuron Chip to provide the packet data in an unencoded format and without a preamble. In this case, an intelligent transmitter accepts the unencoded data and does its own formatting and preamble insertion. The intelligent receiver then detects and strips off the preamble and formatting, and returns the decoded data to the Neuron Chip.

PATENT NOTICE

The Special-Purpose Mode is protected by U.S. Patent No. 5,182,746 and foreign patents based on this patent. No express or implied license is granted herein with respect to such patents. If you are interested in obtaining a non-exclusive, royalty free license to these patents, please call Echelon at +1 (408) 938 5200 and ask for Contracts Management.

Such an intelligent transceiver contains its own input and output data buffers and intelligent control functions, and provides handshaking signals to properly pass the data back and forth between the Neuron Chip and the transceiver. In addition, there are many features that can be defined by and incorporated into a special-purpose transceiver:

- Ability to configure various parameters of the transceiver from the Neuron Chip
- Ability to report on various parameters of the transceiver to the Neuron Chip
- Multiple channel operation
- Multiple bit rate operation
- Use of forward error correction
- Media-specific modulation techniques requiring special message headers and framing
- Collision detection

While the special-purpose mode offers custom features, it is expected that most transceivers will use the single-ended mode for most types of media. This is because single-ended mode offers Differential Manchester encoding, which takes care of clock recovery, whereas special-purpose mode does not have this feature. In addition, the special-purpose mode is a

restricted protocol that Echelon licenses for use only when the Neuron Chip and transceiver are sold as one unit. For more details, contact Echelon Support.

When the special-purpose mode (3.3 V) is used, the Neuron 5000 Processor and the transceiver use a protocol that consists of the Neuron 5000 Processor and the transceiver each exchanging 16 bits (8 bits of status and 8 bits of data; see **Figure 23**) simultaneously and continuously at rates up to 20.0 Mbps (when the Neuron Chip's system clock is 80 MHz). The 20.0-Mbps bit rate allows time-critical flags, such as a Carrier Detect, to be exchanged across the interface with network bit rates up to 625 kbps. The maximum bit rate is 625 kbps because of the overhead associated with the handshaking.

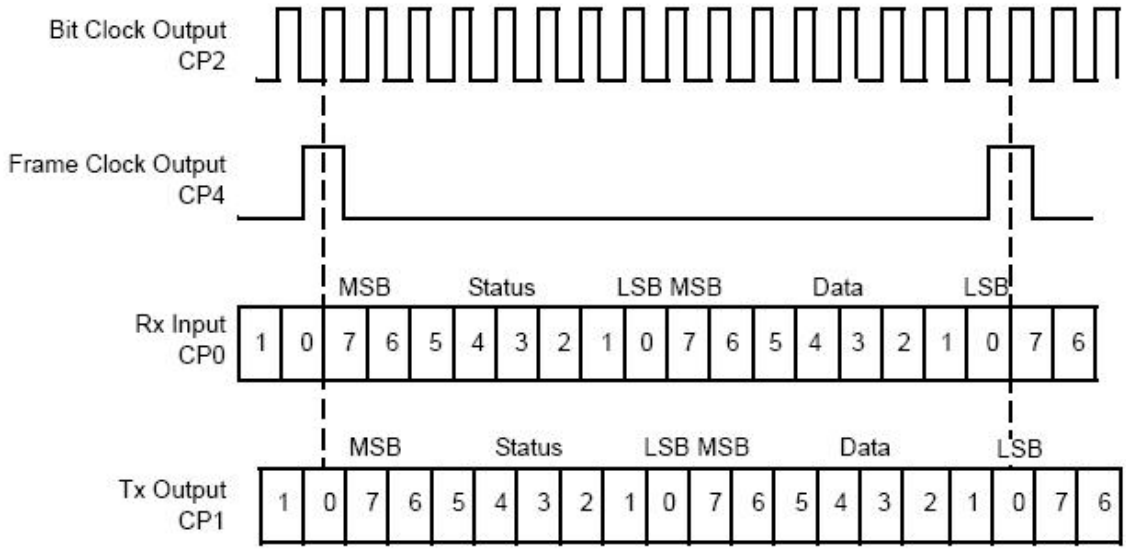


Figure 23. Special-Purpose Mode Data Format

The Neuron Chip communicates with the transceiver through its CP[4:0] pins. CP4 and CP2 are synchronizing clocks generated by the Neuron Chip: CP4 is a frame clock, and CP2 is a bit clock. CP0 and CP1 contain the exchanged data: CP0 transfers data from the transceiver to the Neuron Chip, and CP1 transfers data from the Neuron Chip to the transceiver.

The Neuron Chip and transceiver continuously exchange data through its CP0 and CP1 pins. The bit clock defines transitions between bits in the data stream. The Neuron Chip uses the falling edge of the bit clock to both sample CP0 and change CP1 to the next bit. The transceiver should use the rising edge of bit clock to sample CP1 and update CP0.

The serial data streams on CP0 and CP1 are divided into 16-bit frames. The frame clock (CP4) is used to define the boundaries of the frames. The frame clock is active (high) while the Neuron Chip is outputting the least-significant bit (LSB) of the frame on CP1. On the falling edge of the frame clock, the Neuron Chip is sampling the most-significant bit (MSB) of the next frame on CP0.

The first eight bits of each frame are interpreted as the status field and the last eight bits as the data field. The status field controls transceiver operation and controls passing data between the Neuron Chip and the transceiver. The interpretation of each status bit is shown in **Table 21** on page 54 and **Table 22** on page 54.

Table 21. Special-Purpose Mode Transmit Status Bits

Bit	Flag	Description
7	TX_FLAG	Neuron Chip in the process of transmitting packet
6	TX_REQ_FLAG	Neuron Chip requests to transmit on the network
5	TX_DATA_VALID	Neuron Chip is passing network data to the transceiver in this frame
4	Don't Care	Unused
3	TX_ADDR_R/W	If negated, Neuron Chip is writing internal transceiver register
2	TX_ADDR_2	Address bit 2 of internal transceiver register [1..7]
1	TX_ADDR_1	Address bit 1 of internal transceiver register [1..7]
0	TX_ADDR_0	Address bit 0 of internal transceiver register [1..7]
Note: For bits [2..0] the internal transceiver register 0 is not valid. Registers [1..7] are defined by the transceiver implementation.		

Table 22. Special-Purpose Mode Receive Status Bits

Bit	Flag	Description
7	SET_TX_FLAG	Transceiver accepts request to transmit packet
6	CLR_TX_REQ_FLAG	Transceiver acknowledges request to transmit packet
5	RX_DATA_VALID	Transceiver is passing network data to the Neuron Chip in this frame
4	TX_DATA_CTS	Transceiver indicates that Neuron Chip is clear to send byte of network data
3	SET_COLL_DET	Transceiver has detected a collision while transmitting the preamble
2	RX_FLAG	Transceiver has detected a packet on the network
1	RD/WR_ACK	Transceiver acknowledges read/write to internal register
0	TX_ON	Transceiver is transmitting on the network

There are three types of data that can be sent and received during each frame:

1. Network packet data — Actual data (8 bits at a time) that is to be transmitted or has been received.

2. Configuration data — Information from the Neuron Chip that tells the transceiver how it is to be set up or configured.
3. Status data — Informational parameters reported from the transceiver to the Neuron Chip (when requested by the Neuron Chip).

The contents of the configuration data and status data are defined by the transceiver.

The Neuron Chip controls the communication with the transceiver by asserting and examining status bits. There are four basic operations that the Neuron Chip performs with the transceiver: transmit packet, receive packet, write configuration, and read status.

When the Neuron Chip wants to transmit a packet, it sets the TX REQ FLAG bit of its output status field. The transceiver can then accept or reject the request. To reject the request, the transceiver sets the CLR TX REQ FLAG bit and clears the SET TX FLAG bit. The transceiver indicates that it is ready to transmit by setting the CLR TX REQ FLAG and SET TX FLAG bits for one frame. In that same frame, the transceiver must also set the TX DATA CTS bit to indicate that the Neuron Chip can send the first byte of data.

The Neuron Chip sends a packet of data only if the transceiver accepts the transmit request. The Neuron Chip then sets the TX FLAG bit for the entire duration of the packet. The transceiver must set the TX ON bit while it is transmitting a packet.

Each byte is transferred from the Neuron Chip to the transceiver with a handshake protocol. The transceiver indicates that it is ready to accept a byte by setting the TX DATA CTS bit for a single frame. The Neuron Chip uses this flag to cause it to send out another byte in a subsequent frame; the Neuron Chip also sets the TX DATA VALID bit during the frame that contains the data byte.

After the Neuron Chip sends the last byte in the packet, it clears the TX FLAG bit to indicate the end of transmission. When the transceiver finishes transmitting the packet, including any error codes, it must clear the TX ON bit to indicate that it has released the network.

The transceiver can abort transmission if it detects a collision by setting the SET COLL DET bit for one frame. The Neuron Chip then clears the TX FLAG bit and prepares to resend the packet.

The transceiver initiates packet reception by setting the RX FLAG bit. The transceiver can begin sending data to the Neuron Chip in the frame after setting the RX FLAG bit. Each frame that contains valid data must be marked with the RX DATA VALID bit set. When the transceiver finishes receiving a packet, it clears the RX FLAG bit and the Neuron Chip terminates reception of the packet.

The Neuron Chip performs a configuration write or status read by using the TX ADDR R/W and TX ADDR [2:0] bits. The TX ADDR [2:0] bits indicate which of seven transceiver registers is being accessed, and the TX ADDR R/W bit indicates whether the operation is a configuration register write (0) or status register read (1). Register 0 (TX ADDR [2:0] = 000) is unused, so that TX ADDR R/W = 0 and TX ADDR [2:0] = 000 indicates no read or write operation is to be performed.

To write to a configuration register, the Neuron Chip clears the TX ADDR R/W bit and indicates the selected register with the TX ADDR [2:0] bits. The transceiver must acknowledge that the operation is complete by setting the RD/WR ACK bit. The Neuron Chip continues to send the configuration write command until it receives a frame with the RD/WR ACK bit set.

To read a status register, the Neuron Chip sets the TX ADDR R/W bit and indicates the selected register with the TX ADDR [2:0] bits. The transceiver must acknowledge that the operation is complete by setting the RD/WR ACK bit and by placing the requested

information in the data field. The Neuron Chip continues to send the status request command until it receives a frame with the RD/WR ACK bit set.

Network Connection

How you connect a Series 5000 device to a network depends primarily on whether the Series 5000 device contains an FT 5000 Smart Transceiver or a Neuron 5000 Processor. For FT 5000 Smart Transceivers, you use the FT-X3 transformer; for Neuron 5000 Processors, you use an external transceiver and associated interconnect circuitry.

Connection for an FT 5000 Smart Transceiver

Figure 24 shows the preferred interconnection between the FT 5000 Smart Transceiver and the FT-X3 Communications Transformer; the figure also shows the associated transient protection circuitry. Connect pins 1 and 6 of the FT-X3 transformer to the FT 5000 Smart Transceiver, as shown in the figure. The figure is not a complete schematic, because it does not include the clock, reset, and power supply bypass circuits for the FT 5000 Smart Transceiver. See Appendix C, *FT-X3 Communications Transformer*, on page 143, for a schematic view of the FT-X3 Communications Transformer.

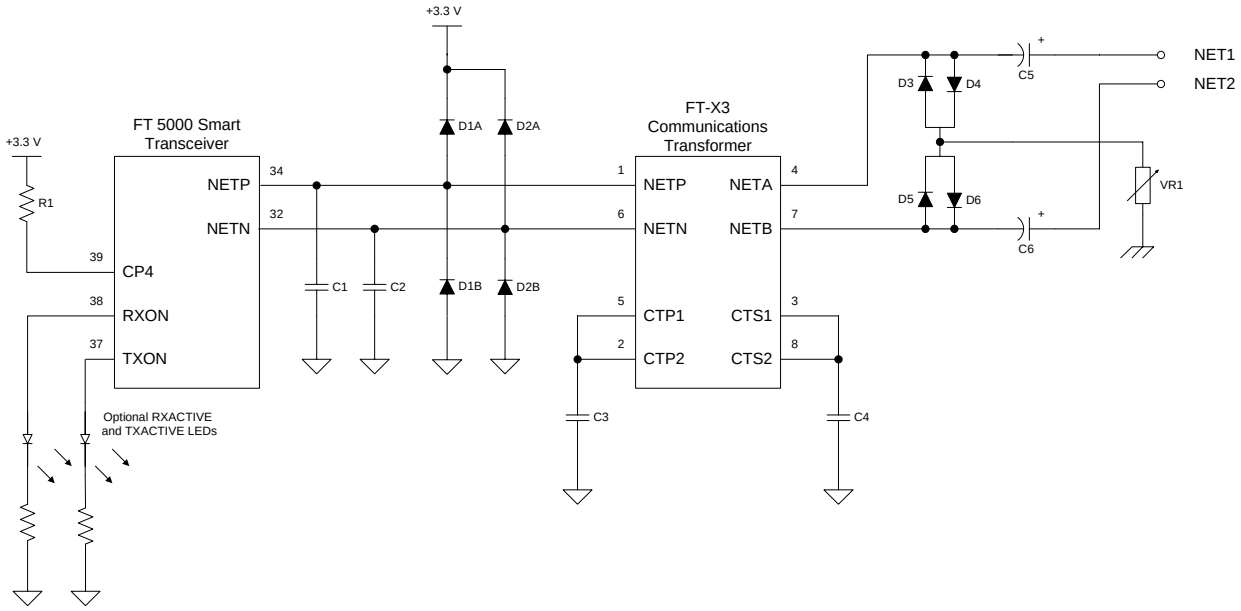


Figure 24. FT 5000 Smart Transceiver and FT-X3 Interconnections

Table 23. External Components for FT 5000 Smart Transceiver

Name	Value	Description
R1	4.99 kΩ	Pullup resistor
VR1	470 V MOV, 5 mm, 40 pF (typical)	Panasonic ERZV05D471, Digi-Key P7186-ND or equivalent

Name	Value	Description
C1, C2	56 pF, 50 V	Common-mode noise immunity capacitors (for EN61000-4-6 Level 3)
C3, C4	100 pF, 5%	Optional center-tap capacitors
C5, C6	22 µF, ≥50 V, polar	DC blocking capacitors
D1, D2	BAV99	ESD transient clamping diodes
D3, D4, D5, D6	 BAV99, 1N4148-equivalent 1N4934, 1N4935, FR1D, RS1D, RS1DB	Differential network clamping diodes: For up to 2 kV Surge Protection For up to 6 kV Surge Protection

In **Figure 24**, diodes D1 and D2 are ESD transient clamping diodes. Capacitors C1 and C2 provide common-mode noise immunity for compliance with EN61000-4-6 Level 3. Capacitors C5 and C6 are used to provide DC voltage isolation for the FT 5000 Smart Transceiver when it is used on a link power network and to protect it in the event of a DC power fault on the network wires. The capacitors are required to meet LONMARK interoperability guidelines for the TP/FT-10 channel. These capacitors are not needed for devices that will be connected exclusively to non-link power networks and do not require protection against DC faults. Two polar capacitors are used to protect against the application of a DC voltage of either polarity, while providing a total capacitance of 11 µF. Alternatively, a single non-polar capacitor of 10 µF can be used in either of the two legs that connect to the network. The initial tolerance of the capacitor should be ±20% or less, and degradation due to aging and temperature effects should not exceed 20% of the initial minimum value.

In some cases, adding capacitors (C3 and C4) between the center tap pins and earth ground can reduce EMI emissions.

Note that Series 3100 FT Smart Transceivers had a single **COMM_ACTIVE** pin (equivalent to the CP2 pin for a Series 3100 Neuron Chip) that you could connect to a special COMM_ACTIVE LED circuit to drive a pair of LEDs to display network activity. FT 5000 Smart Transceivers have two communications pins, **TXON** and **RXON**, that you can connect to network activity LEDs (RXACTIVE and TXACTIVE) without any special circuitry requirements. However, you might want to add pulse-stretching circuitry for these packet-activity signals for increased visibility. If your device does not require network activity LEDs, pins 37 and 38 should be treated as No Connect.

Comparison with FT 3120 or FT 3150 Devices

The interconnection with the network transformer for an FT 3120 Smart Transceiver or an FT 3150 Smart Transceiver is similar to the interconnection for an FT 5000 Smart Transceiver (as described in *Connection for an FT 5000 Smart Transceiver* on page 56). However, FT 3120 and FT 3150 Smart Transceivers can use one of three transformers: the FT-X1 (a through-hole part), the FT-X2 (a surface-mount part), or the FT-X3 (a surface-mount part).

Although you can use an FT-X1 or FT-X2 transformer with an FT 5000 Smart Transceiver, you cannot simply replace an existing FT 3120 or FT 3150 Smart Transceiver with an FT 5000 Smart Transceiver. The voltage requirement is different (the FT 5000 Smart Transceiver is a 3.3 V part and the FT 3120 or FT 3150 Smart Transceiver is a 5 V part); the packages are different; and the pinouts are different. In addition, if your Series 3100 device uses a COMM_ACTIVE circuit to drive network-activity LEDs, the requirements for that circuit are very specific for FT 3120 or FT 3150 Smart Transceivers, whereas for FT 5000 Smart Transceivers, you can use a simple LED driver circuit for the two network activity LEDs.

See the *FT 3120 / FT 3150 Smart Transceiver Data Book* for more information about the interface for FT 3120 or FT 3150 Smart Transceivers.

Comparison with the FTT-10A Transceiver

The FTT-10A transceiver is designed to be used with Neuron Chips (both Series 3100 and Series 5000). The migration path from a Series 3100 Neuron Chip to a Series 3100 Smart Transceiver is fairly straightforward:

- The Series 3100 Smart Transceiver has the same footprint as the corresponding Series 3100 Neuron Chip
- The FT-X1 transformer has the same footprint as the FTT-10A transceiver
- The pinout of the FT-X1 transformer is compatible with the connections between the Series 3100 Neuron Chip and the FTT-10A transformer

See the *FT 3120 and FT 3150 Smart Transceiver* datasheet for more detailed information on these pinouts and footprints.

A device based on a Series 3100 Smart Transceiver with the FT-X1 or FT-X2 transformer can run the same applications with the same functionality as a 3100 Neuron Chip with an FTT-10A transceiver. In addition, Series 3100 Smart Transceiver with the FT-X1, FT-X2, or FT-X3 transformer has the same levels of transient immunity, but has improved magnetic field noise immunity, and improved common-mode network noise immunity (as tested per EN 61000-4-6). See the *FT 3120 / FT 3150 Smart Transceiver Data Book* for more information migrating from a 3100 Neuron Chip with an FTT-10A transceiver to a Series 3100 Smart Transceiver with the FT-X1 or FT-X2 transformer.

The migration path from a Series 3100 Neuron Chip to a Series 5000 Smart Transceiver requires additional design work:

- The Series 5000 Smart Transceiver is a 3.3 V part and the Series 3100 Neuron Chip is a 5 V part
- The Series 5000 Smart Transceiver has a different footprint compared to the corresponding Series 3100 Neuron Chip
- The FT-X3 transformer has a different footprint compared to the FTT-10A transceiver
- The pinout of the FT-X3 transformer is not entirely compatible with the connections between the Series 3100 Neuron Chip and the FTT-10A transformer

A device based on a Series 5000 Smart Transceiver with the FT-X3 transformer can run the same applications (after they are recompiled for the FT 5000 Smart Transceiver) with the same functionality as a 3100 Neuron Chip with an FTT-10A transceiver or a Series 3100 Smart Transceiver with a FT-X1 or FT-X2 transformer. In addition, a Series 5000 Smart Transceiver with the FT-X3 transformer has the same levels of transient immunity,

magnetic field noise immunity, and common-mode network noise immunity (as tested per EN 61000-4-6) as a Series 3100 device.

Connection for a Neuron 5000 Processor

You can connect a Neuron 5000 Processor to an external transceiver to communicate with a TP/XF-1250 channel, an EIA-485 network, a link-power TP/FT-10 channel, or other transceivers. Use an FT 5000 Smart Transceiver for a standard (non-link-powered) TP/FT-10 channel or for a locally powered device on a link-power TP/FT-10 channel.

TPT/XF-1250 Transceivers

You can use the Neuron 5000 Processor with an Echelon TPT Twisted Pair Transceiver Module for a TP/XF-1250 channel type. However, because the Neuron 5000 Processor does not include an on-chip differential transceiver (that is, the Neuron 5000 Processor does not support the differential mode of operation that Neuron 3120 Chips and Neuron 3150 Chips supported), you must:

- Select "TP/XF-1250" as the transceiver type within the Hardware Template Editor of the NodeBuilder FX Development Tool or the Mini FX Evaluation Kit. This selection causes the Neuron firmware to configure the Neuron 5000 Processor's communications port to operate in 3.3 V single-ended mode.
- Add a single-ended mode to differential mode converter circuit, as described in the *Connecting a Neuron 5000 Processor to an External Transceiver* Engineering Bulletin (005-0202-01B). This circuit converts the Neuron 5000 Processor's 3.3 V single-ended mode signals to the 5 V differential mode signals required for the TPT/XF-1250 transceiver.

Figure 25 on page 60 shows the basic configuration for connecting a Neuron 5000 Processor to a TPT/XF-1250 transceiver.

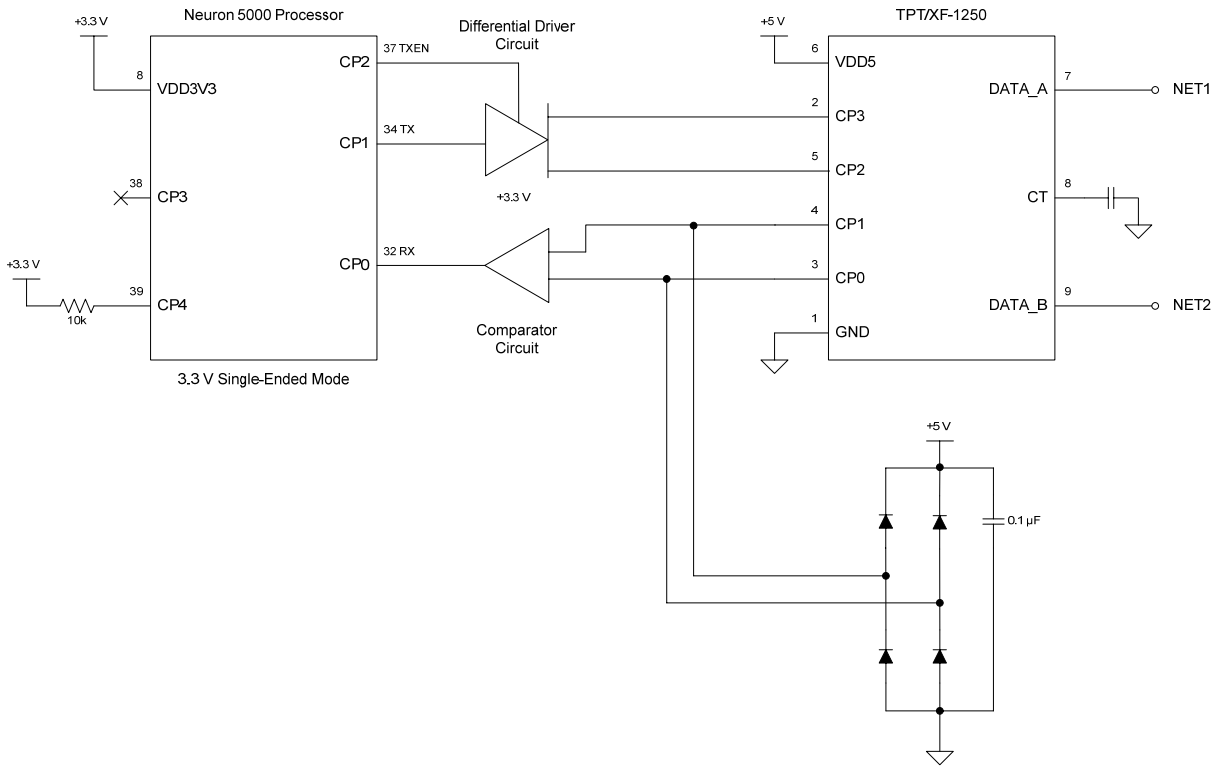


Figure 25. Connecting a Neuron 5000 Processor to a TP/XF-1250 Transceiver

In the figure, the pullup resistor for the Neuron Chip's CP4 pin is optional, but helps prevent contention on the CP4 pin if the Neuron Processor is incorrectly configured to operate in special-purpose mode (for which the CP4 pin is an output). The diode clamps for the TPT/XF-1250 transceiver's CP0 and CP1 signals are high-speed switching diodes, such as Fairchild Semiconductor® 1N4148 small-signal diodes. The value of the capacitor on the TPT/XF-1250 transceiver's transformer center tap (CT) pin depends on the device's PCB layout and EMI characteristics. A typical value is 100 pF rated for 1000 V. For more information about the TPT/XF-1250 transceiver, see the *LONWORKS TPT Twisted Pair Transceiver Module User's Guide* (078-0025-01C).

The details of the required differential driver circuit and the comparator circuit are described in the *Connecting a Neuron 5000 Processor to an External Transceiver* Engineering Bulletin (005-0202-01B).

EIA-485 Transceivers

You can use the Neuron 5000 Processor with commercially available EIA-485 transceivers. Multiple data rates (up to 1.25 Mbps), and a number of wire types can be supported. With an EIA-485 transceiver, common-mode voltage ranges between –7 V to +12 V. To implement an EIA-485 device, the Neuron 5000 Processor's communications port runs in single-ended mode.

Available industry standards that describe EIA-485 specifications provide details on unit loads, data rate, wire size, and wire distances. To ensure interoperability between devices, the LONMARK interoperability guidelines require a data rate of 39 kbps for devices that use EIA-485 transceivers. In addition, the EIA-485 transceiver must have TTL-compatible

inputs for the connection to the Neuron 5000 Processor. A typical circuit configuration, shown in **Figure 26**, can support up to 32 loads.

Individual device power sources can create problems when the common voltage exceeds –7 V, + 12 V, or with ground faults.

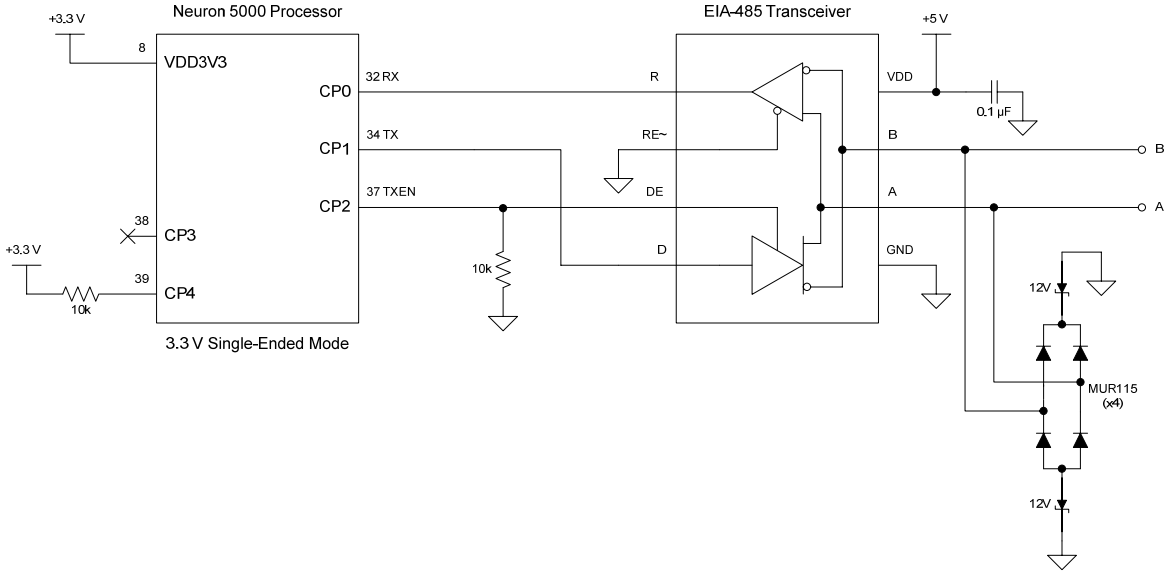


Figure 26. EIA-485 Twisted-Pair Interface (Uses Single-Ended Mode)

The EIA-485 specification requires a common ground reference for all transceivers. This common ground reference can be provided by adding a third conductor in the network cable or a separate connection to common ground at each device.

LPT-11 Link Power Transceivers

The Echelon LONWORKS LPT-11 Link Power Twisted Pair Transceiver provides a simple, cost effective method for adding a network-powered LONWORKS transceiver to any Neuron Chip-based sensor, activator, display, lighting device, or general purpose I/O controller. The LPT-11 transceiver eliminates the need to use a local power supply for each device, because device power is supplied by a central power supply over the same twisted wire pair that handles network communications.

Figure 27 on page 62 shows the basic configuration for connecting a Neuron 5000 Processor to an LPT-11 Twisted-Pair Link Power Transceiver.

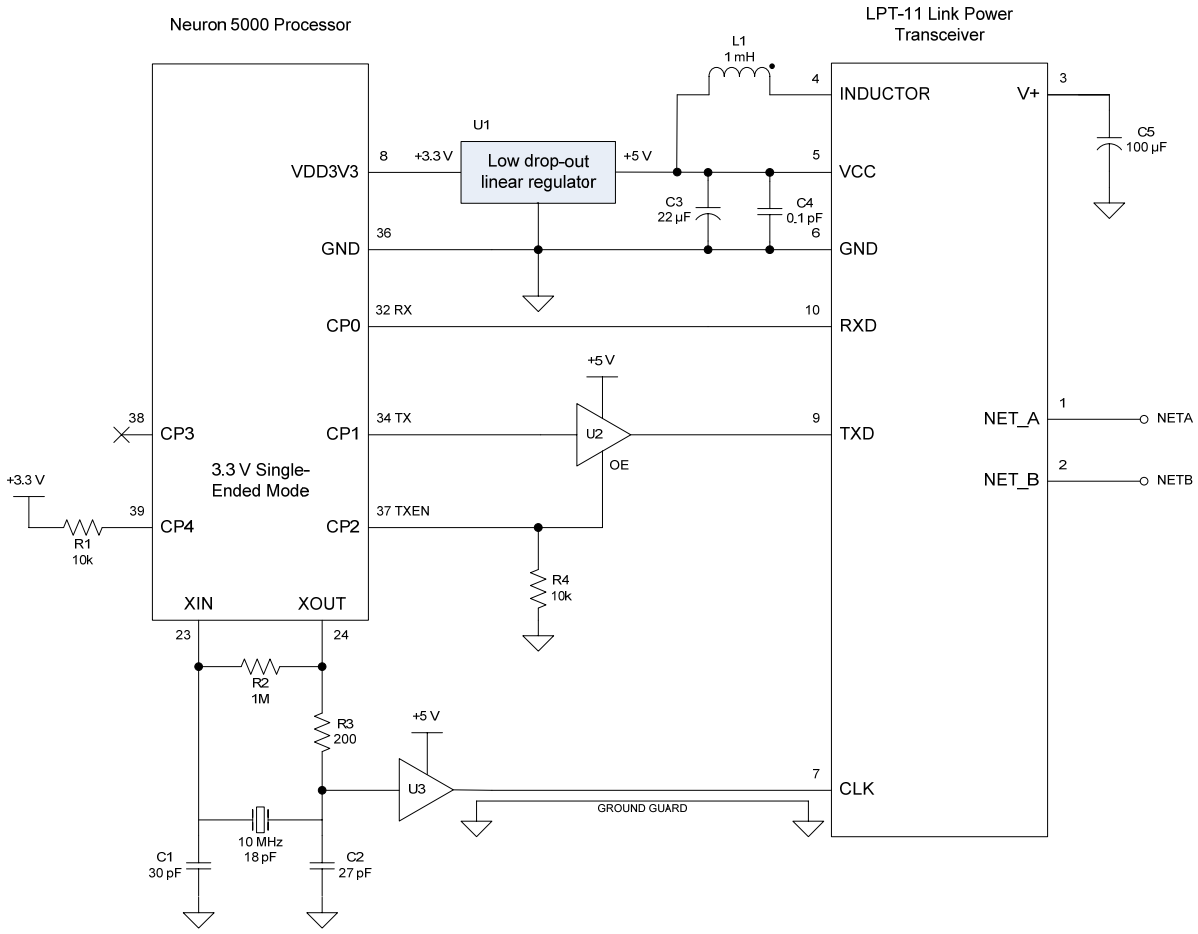


Figure 27. Connecting a Neuron 5000 Processor to an LPT-11 Link Power Transceiver

The major differences between connecting a Series 3100 Neuron Chip to an LPT-11 transceiver (see the *LonWorks LPT-11 Link Power Transceiver User's Guide*, 078-0198-01A) and connecting a Neuron 5000 Processor to an LPT-11 transceiver are:

- The connection between the LPT-11 VCC pin and the Neuron 5000 VDD3V3 pin requires the addition of a low drop-out linear regulator to convert the +5 V output from the LPT-11 transceiver to the +3.3 V input for the Neuron 5000 Processor.
- The connection between the LPT-11 TXD pin and the Neuron 5000 CP1 pin requires the addition of a non-inverting bus buffer/line driver that supports TTL-compatible input and 5V CMOS output. The output of the Neuron CP2 pin is also connected to the buffer/line driver to allow the Neuron 5000 Processor to propagate a device reset to the LPT-11 transceiver by setting the buffer/line driver to a tri-state impedance state. An example part for the buffer/line driver is an NXP® 74AHCT1G126 bus buffer/line driver.
- The connection between the LPT-11 CLK pin and the Neuron 5000 XOUT pin requires the addition of a standard (inverting or non-inverting) bus buffer/line driver that supports TTL-compatible input and 5V CMOS output.

See the *Connecting a Neuron 5000 Processor to an External Transceiver* Engineering Bulletin (005-0202-01B) for additional information.

Clock Requirements

A Series 5000 chip requires a 10 MHz external crystal or oscillator to provide its input clock signal. The chip then multiplies the input frequency by an amount specified in the device's hardware template (specified during device development using the NodeBuilder FX Development Tool or Mini FX Evaluation Kit) to derive its internal system clock frequency. For multipliers greater than one, the chip uses a phase-locked loop (PLL) to drive and manage the internal on-chip system clock frequency.

This section describes the requirements for the external crystal and compares terminology for Series 5000 chip clock frequencies with Series 3100 chip clock frequencies.

External Crystal

A Series 5000 chip requires a 10.0 MHz external clock signal for operation. An example part that meets the requirements for a Series 5000 chip is the Abracon Corporation ABMM2100000MHzD1 Ceramic Surface Mount Low Profile Quartz Crystal.

The crystal must have a load capacitance rating of 18 pF. Because a Series 5000 chip does not have internal load capacitance on-chip, you must add 30 pF combined external series capacitance, as shown in **Figure 28**.

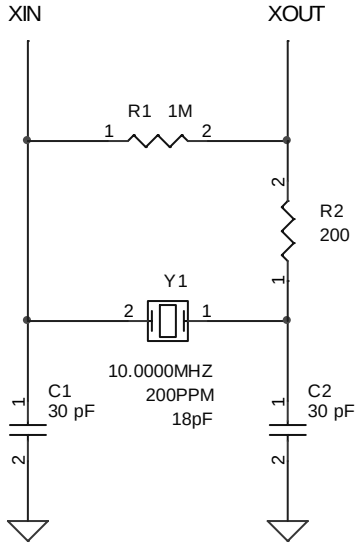


Figure 28. Series 5000 Chip Clock Generator Circuit

Unlike for a Series 3100 chip, the Series 5000 chip's **XOUT** pin cannot be used to drive an external CMOS load. However, if you maintain the required capacitance for the **XOUT** pin, you can drive an external clock, for example, as shown for the LPT-11 Link-Power Transceiver in **Figure 27** on page 62.

If your device requires a common clock signal, you can use an external 3.3 V oscillator module (such as a Vishay® Intertechnology XOSM-533 Surface Mount Oscillator), and leave **XOUT** unconnected. You could also define an output frequency I/O model for one of the Series 5000 chip's I/O pins (IO0..IO11) and connect the load's clock signal to the Series 5000 chip's I/O pin.

A 60/40 duty cycle or better is required for the external oscillator, as shown in **Figure 29** on page 64. An external oscillator must provide low-voltage transistor-transistor logic (LVTTL) voltage levels (0 to 3.3 V) to the **XIN** pin.

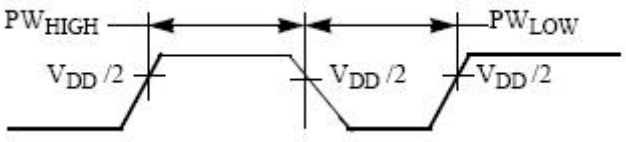


Figure 29. Test Point Levels for XIN Duty-Cycle Measurements

To ensure proper oscillator startup, the equivalent series resistance specification for the crystal should be ≤50 Ω, and the crystal shunt capacitance should be no greater than 7 pF.

A Series 5000 chip requires a clock frequency with a total accuracy of ±200 ppm over the full range of component tolerances and operating conditions, including oscillator tolerance, crystal tolerance, PCB and capacitor variation, and aging. Variation within the Series 5000 chip uses a portion of the overall ±200 ppm budget. Its duty cycle symmetry must be no worse than 60/40%. In addition, the voltage swing of the clock signal must be within the GND and V_{DD33} supply rails of the Series 5000 chip. This clock can be provided by connecting an appropriate parallel resonant crystal to the **XIN** and **XOUT** pins of the Series 5000 chip, as shown in **Figure 28**.

The remaining portion of the error budget allocated for *total crystal uncertainty* is ±85 ppm (assuming that the selected crystal has a load capacitance specification that matches the circuit loading). *Total crystal uncertainty* is the combination of the crystal's initial frequency tolerance plus its temperature and aging tolerances. Note that a typical crystal aging specification is 5 ppm/yr but, because the aging effect tends to follow a logarithmic curve, aging over a 10 year span is commonly in the range of 10 to 15 ppm (contact individual crystal vendors for detailed specifications).

Comparison with Series 3100 Clocks

For Series 3100 chips, you specified the value of the system clock through the use of a specific external crystal or oscillator (for example, a 10 MHz crystal). For Series 5000 devices, you specify the system clock rate through software tools (the NodeBuilder FX Development Tool or Mini FX Evaluation Kit). For a Series 5000 device, the external clock is always a 10 MHz crystal, but the internal system clock rate can vary from 5 MHz to 80 MHz.

Internally, a Series 3100 chip divided the external crystal's frequency by 2 to obtain an internal system clock rate; thus, a 10 MHz external crystal provided a 5 MHz internal system clock rate. However, a Series 5000 chip multiplies the external crystal's 10 MHz frequency by a value specified in the device's hardware template to specify the internal system clock rate; thus, a multiplier value of 1 yields a 10 MHz internal system clock rate, and a multiplier value of 8 yields an 80 MHz internal system clock rate. Valid multiplier values are ½, 1, 2, 4, and 8. Note that a for a multiplier value of ½, the Series 5000 chip actually runs at 10 MHz (as if a multiplier of 1 were specified), but the Neuron system firmware schedules the application such that the application runs at 5 MHz.

Because the internal system clock rate is multiplied, rather than divided, a Series 5000 chip of a specific system clock rate can be considered to be approximately twice as fast as an equivalent Series 3100 chip (for example, an FT 5000 Smart Transceiver with a system clock of 20 MHz is approximately twice as fast as FT 3150 Smart Transceiver with an input clock of 20 MHz). The difference is approximate because a specific application on a Series 5000 device might run more than twice (or less than twice) as fast it would on a Series 3100 device due to variations in the hardware and software that are required by the Neuron architecture for Series 5000 devices.

Whenever the documentation for Series 5000 devices describes the system clock rate, it refers to the 10 MHz to 80 MHz internal system clock rate that is specified in the device's hardware template, not the 10 MHz frequency value of the external crystal.

Reset Function

The reset function is a critical operation in any embedded microprocessor or microcontroller. For Series 5000 chips, the following mechanisms initiate a reset:

- The **RST~** pin is pulled low and then released by an external switch or circuit.
- Device power up.
- Watchdog timeout occurs during application execution. The watchdog period is fixed at 840 ms (1.19 Hz) for all system clock rates. The actual timeout range is between 0.8 s and 1.7 s.
- Software command either from the application program or from the network.
- An exception trap (interrupt).
- The internal Low-Voltage Indicator (LVI) circuit detects a drop in the power supply below a set level. See the FT 5000 Free Topology Smart Transceiver data sheet or the Neuron 5000 Processor data sheet for internal LVI trip points.

During a reset, when the **RST~** pin is in the low state, the Series 5000 chip pins go to the following states:

- Oscillator continues to run
- All processor functions stop
- The **SVC~** pin goes to high impedance, with pullup
- I/O pins go to high impedance
- All memory interface pins go to high impedance

Figure 32 on page 70 illustrates the condition of the pins during reset and the Series 5000 chip initialization sequence after the **RST~** pin is released.

When the **RST~** pin is released back to a high state, the Series 5000 chip begins its initialization procedure starting at address 0x0001. The time it takes the Series 5000 chip to complete its initialization differs between the type of external serial memory used (SPI or I^2C), different firmware versions that are being run, and the memory space used by the application (code and data); see *Reset Processes and Timing* on page 68 for more information.

RST~ Pin

The **RST~** pin is both an input and an output. As an input, the **RST~** pin is internally pulled high by a resistor. The **RST~** pin becomes an output when any of the following events occur:

- Internal LVI detects a low voltage condition
- Software reset initialization
- Watchdog Timer event (times out)
- Traps

In some cases it is desirable to use the input capability of the **RST~** pin to allow other devices to reset the Series 5000 device. Examples of external devices that can be used for this purpose include push button switches, microcontrollers, and external low-voltage detectors.

Important: If the proper external reset circuitry is not used, the Series 5000 device can become applicationless or unconfigured. The applicationless or unconfigured state occurs when the checksum error verification routine detects corruption in memory which could have been falsely detected because of an improper reset sequence.

The following guidelines must be followed in order for the Series 5000 device's reset functions to operate reliably:

- Any device connected to the **RST~** pin must have an open-drain (or equivalent) output. If an external device were to actively drive the **RST~** pin high, contention between that device and the Series 5000 chip's internal circuitry could result in anomalous behavior ranging from applicationless errors to device failure.
- If any external devices are connected to the **RST~** pin of the Series 5000 chip, a capacitor should be connected between **RST~** and ground to provide noise immunity. The value of this capacitor should be at least 100 pF, and must not exceed 1000 pF. For even greater noise immunity, two capacitors (totaling ≤1000 pF) can be used, with one connected from the **RST~** pin to ground and the other from **RST~** to V_{DD33}. These capacitors should be located within 5 mm of the Series 5000 chip's **RST~** pin.
- During board level in-circuit testing (ICT), the **RST~** pin should be hard wired to ground through a "pogo pin".

Figure 30 shows an example reset circuit.

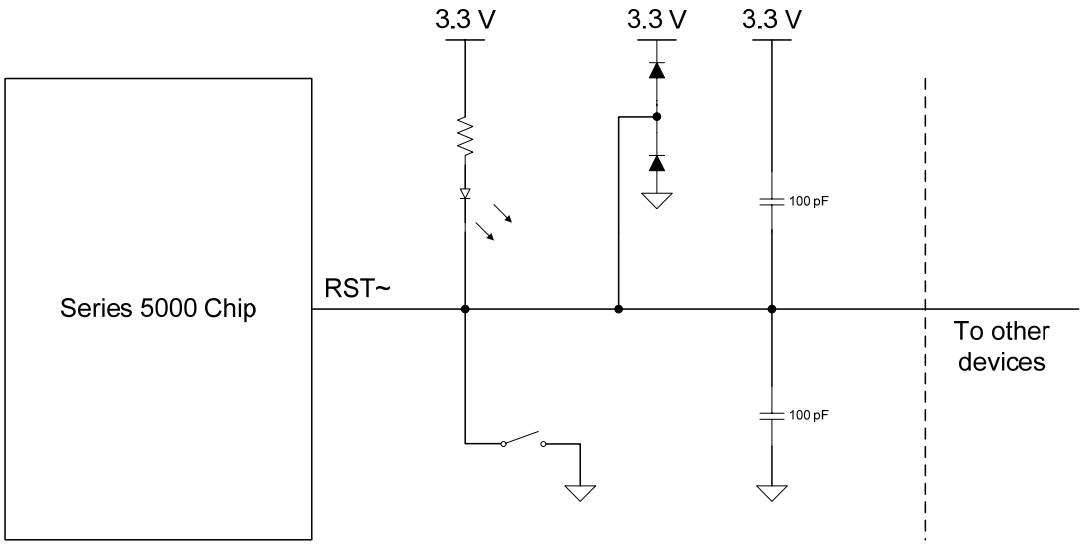


Figure 30. Reset Circuit

Reset Sources

Any of the following sources can cause a Series 5000 chip to reset:

- Device reset button press (or other hardware-driven assertion of the RST~ pin)
- Power-on reset
- LVI circuit trip

- Watchdog timer expiration
- System-level traps
- Software-driven reset

The source of the last reset is saved in the Reset Cause register for diagnostic purposes.

Power-Up and LVI

Both the power-on reset and low-voltage indications act as a single reset source. During power up sequences, the **RST~** pin is held low by the internal LVI until the power supply is stable. Likewise, when powering down, the **RST~** pin is driven low when the power supply goes below the Series 5000 chip's minimum operating voltage.

See the FT 5000 Free Topology Smart Transceiver data sheet or the Neuron 5000 Processor data sheet for internal LVI trip points.

During reset or power down, external EEPROM device can experience data corruptions. To mitigate such corruptions, the reset condition is delayed for a short time while the serial memory interface aborts current transactions and stops the SPI or I^2C interface without initiating a write sequence, if possible. If a write has already been initiated, it is possible that it could successfully complete before V_{DD33} drops below the absolute minimum for the device. See *Maintaining Non-Volatile Memory Integrity* on page 28 for additional considerations to maintain memory robustness.

Watchdog Timer

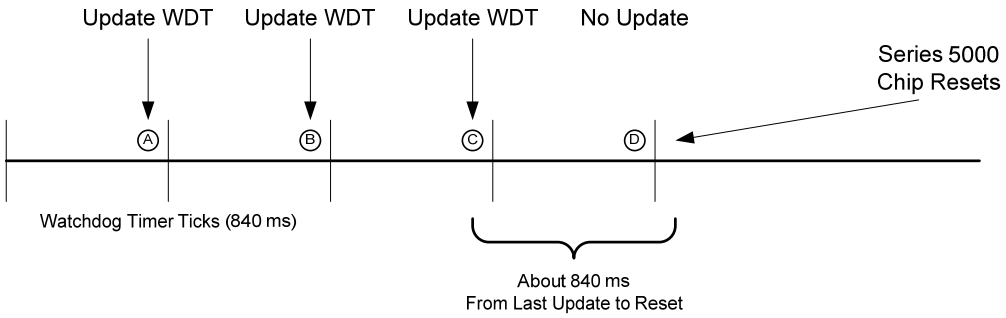
A Series 5000 chip is protected against malfunctioning software or memory faults by three watchdog timers, one for each processor that makes up the Neuron Core. If the application or the system software fails to update these timers periodically, the entire Series 5000 chip automatically resets. The Watchdog Timer circuit is always active and cannot be disabled.

The watchdog timer period is fixed at 840 ms (1.19 Hz) for all system clock rates. However, the actual timeout range is between 0.8 s and 1.7 s (see **Figure 31** on page 68). Each watchdog timer is a free-running timer, rather than a one-shot timer; that is, the timeout value is not set or reset each time the watchdog timer is updated. Updating the watchdog timer ensures that the expiration of the next timer tick does not cause a processor reset.

Example 1: The top example in **Figure 31** shows periodic WDT updates that occur just before the current WDT tick expires. The update at C ensures that the processor does not reset at the next WDT tick (which occurs immediately after the update at C). However, the missed update at D causes the processor to reset. The time between the last WDT update and the processor reset is about 840 ms.

Example 2: The bottom example in **Figure 31** shows periodic WDT updates that occur just after the current WDT tick has expired. The update at C ensures that the processor does not reset at the next WDT tick (which occurs almost a full WDT period after C). However, the missed update at D does not cause the processor to reset because the update at C ensured no reset. Instead, another WDT period elapses before the processor resets. The time between the last WDT update and the processor reset is about 1.7 s.

EXAMPLE 1



EXAMPLE 2

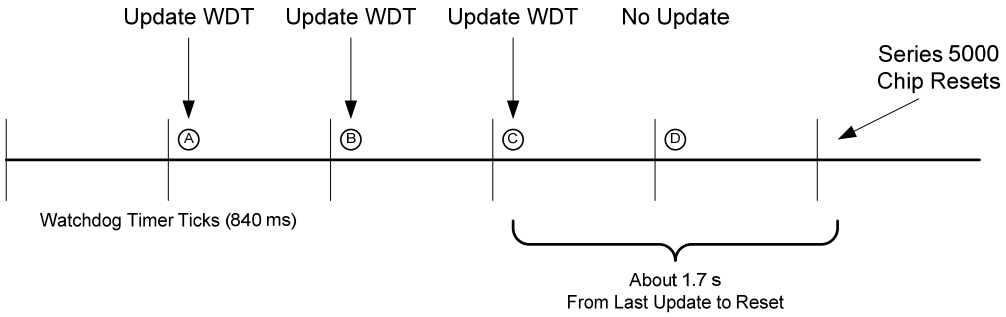


Figure 31. Series 5000 Watchdog Timer Period

Because your application typically has no knowledge of the current WDT tick, the application should update the WDT at regular intervals at least every 500 ms.

Traps

The Neuron architecture provides a set of interrupts for various error conditions that allow the application or firmware to continue to run. A system-level trap is highest level of interrupt and is non-maskable, that is, it cannot be disabled. For each of these traps, the system firmware handles the interrupt, initiates a reset if necessary, and updates the error log for the chip. See *Processor Integrity* on page 75 for additional information about these traps.

Software-Controlled Reset

When the CPU watchdog timer expires, or a software command to reset occurs, the **RST~** pin is pulled low for 256 XIN clock cycles (25.6 µs).

Reset Processes and Timing

During the reset period, the I/O pins are in a high-impedance state. The **SVC~** pin is high impedance during reset with an internal pull-up resistor.

Figure 32 on page 70 summarizes the steps that a Series 5000 chip follows in preparing to execute application code. After the **RST~** pin is released, the Series 5000 chip performs hardware and firmware initialization before executing application programs, including the following tasks:

- The system image is copied from ROM to RAM (approximately 43 ms)
- The three base processors (NET, MAC, and APP) start running and the system image starts running
- The stack initialization and built-in self-test (BIST) begins
- If an alternate system image exists, it is copied from external non-volatile memory (NVM) to RAM (a variable amount of time, based on the NVM device type), and the chip resets
- The application data in NVM is shadowed to RAM (a variable amount of time, based on the amount of data to copy and the NVM device type)
- The **SVC~** pin is initialized based on the state of the device
- The system state is initialized (external EEPROM initialized, if necessary)
- The system clock is set to the rate specified in the configuration data (prior to this point, the chip runs at 10 MHz)
- The extended RAM is initialized based on the information contained in the configuration data
- The random number seed is calculated
- The system RAM is set up
- The communication port is initialized
- Checksum is performed for the application
- The one-second timer is initialized
- The scheduler is initialized

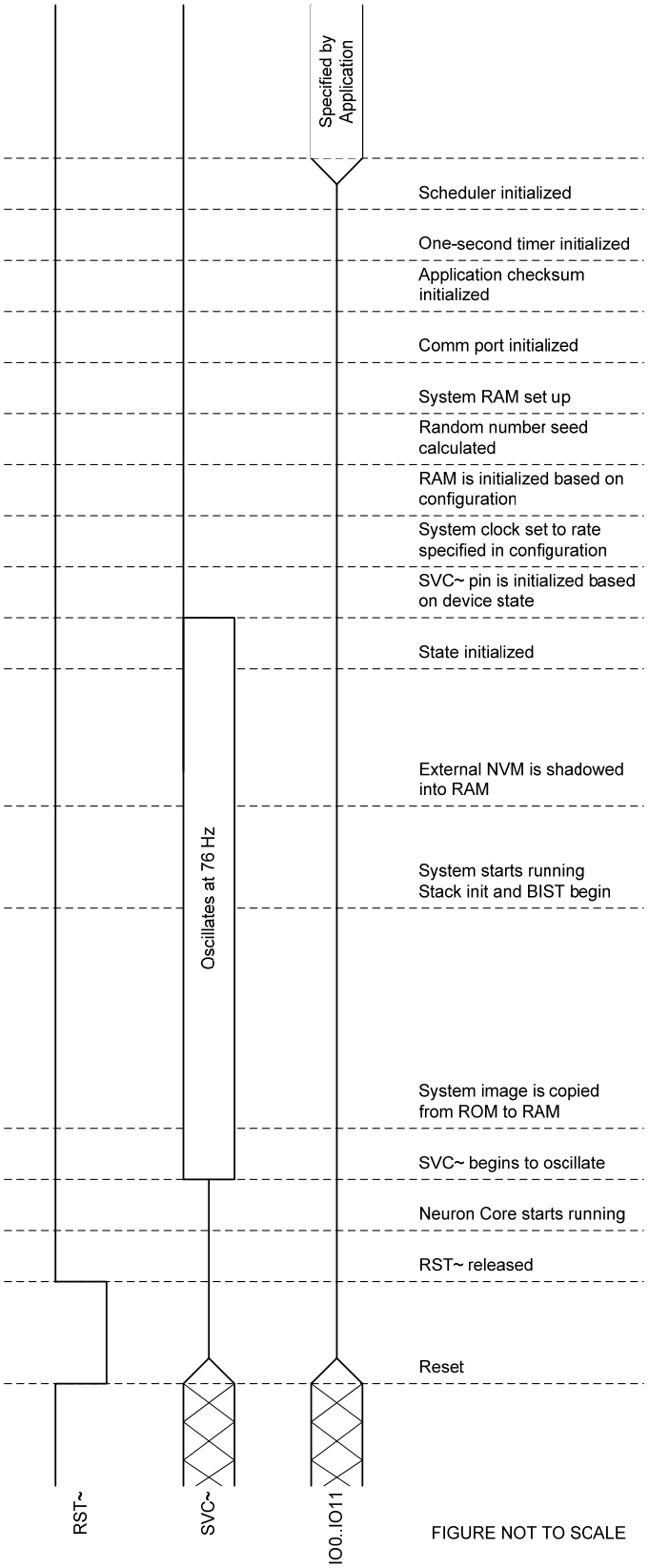


Figure 32. Reset Timeline for Series 5000 Chips

Approximately 10 µs after the **RST~** pin is released, the Neuron Core starts running. The **SVC~** pin oscillates between a solid low and a weak pullup.

The default firmware system image is copied from ROM into RAM. This process takes approximately 43 ms. This process occurs regardless of whether an alternate system image exists; the alternate system image is loaded after the system begins running and BIST complete. After an alternate system image is loaded, the chip resets, but during this reset it does not copy the system image from ROM.

The three main processors (NET, MAC, and APP) start, and the system begins running. The stack initialization and BIST task tests the on-chip RAM, the timer/counter logic, and the counter logic. The stack initialization and BIST task takes approximately 16 ms. For the test to pass, all three processors and the ROM must be functioning. A flag is set to indicate whether the Series 5000 chip passed or failed the BIST. The RAM is set to all 0s by the end of this step.

If the RAM self-test fails, the device goes offline, the service LED comes on solid, and an error is logged in the device's status structure.

Self-test results are available in the first byte of RAM (0xE800), as listed in **Table 24**.

Table 24. Self-Test Results

Value	Description
0	No Failure
1	RAM failure
2	Timer/counter failure
3	Counter failure

The external non-volatile memory (NVM) is shadowed into RAM from the EEPROM or flash memory device. The amount of time required for this process depends on the amount of NVM to be copied and the type of device:

- I²C EEPROMs: For the minimal 2 KB EEPROM configuration, this process takes 52 ms. For larger EEPROM devices, this process takes 25 ms for each 1 KB of configured EEPROM (so that the maximum EEPROM configuration of 44 KB takes 1102 ms to complete).
- SPI EEPROMs: For the minimal 2 KB EEPROM configuration, this process takes 35 ms. For larger EEPROM devices, this process takes 17.2 ms for each 1 KB of configured EEPROM.
- SPI FLASH devices: This process takes 17.7 ms for each 1 KB of configured flash memory.

The state initialization task determines if the external EEPROM needs to be initialized; if it does need to be initialized, the state initialization task configures the Series 5000 chip with the default communication parameters and copies them to the external EEPROM. This chip also enters the applicationless state.

The **SVC~** pin initialization task turns off the **SVC~** pin (high state).

The extended RAM initialization task checks the memory map to determine if any extended RAM is included in the configuration, and then clears all of the extended RAM. This task

requires approximately 7.81 ms per 1 KB of extended RAM at 80 MHz (or 8.88 ms per 1 KB of extended RAM at 10 MHz).

The random number seed calculation task creates a seed for the random number generator.

The system RAM setup task sets up internal system pointers as well as the linked lists of system buffers.

The checksum initialization task generates or checks the checksums for the application. The checksum is a negated two's complement sum of the values in the image.

The one-second timer initialization task initializes the one-second timer. At this point, the network processor is available to accept incoming packets.

The scheduler initialization task allows the application processor to perform application-related initialization:

- **State wait** — Wait for the device to leave the applicationless state.
- **Pointer initialization** — Perform a global pointer initialization.
- **Initialization step** — Execute initialization task, which is created by the compiler/linker to handle initialization of static variables and the timer/counters.
- **I/O pin initialization step** — Initialize I/O pins based on application definition. Prior to this point, I/O pins are high impedance.
- **State wait II** — Wait for the device to leave the unconfigured or hard-offline state. If waiting was required, a flag is set to indicate that the device should come up offline.
- **Parallel I/O synchronization** — Devices using parallel I/O attempt to execute the master/slave synchronization protocol.
- **Reset task** — Execute the application reset task (**when (reset){ }**).
- **Flag check** — If the offline flag was set, the chip goes offline and executes the offline task (**when(offline){ }**). If the BIST flag indicated a failure, the SERVICE LED is turned on and the offline task is executed. Otherwise, the scheduler starts its normal task scheduling loop.

The amount of time required to perform these steps depends on many factors, including: Series 5000 chip model; system clock rate; whether or not the device performs a boot of an alternate system image; whether the device is applicationless, configured, or unconfigured; amount of extended RAM; the number of buffers allocated; and application initialization. **Table 25** summarizes the time required for each of these steps for a Series 5000 chip. The times are approximate and are given as functions of the most significant application variables. Prior to the extended RAM initialization step, the chip's system clock runs at 10 MHz; all subsequent steps use the system clock at its configured rate (5 to 80 MHz), and so the time required is listed in clock cycles.

Table 25. Series 5000 Chip Reset Sequence Time

Step	Time Required	Notes
System image copied from ROM to RAM	Approximately 43 ms	
Stack Initialization and BIST	16 ms	

Step	Time Required	Notes
Alternate system image copied from NVM to RAM	400 ms for I²C EEPROM 275.2 ms for SPI EEPROM 283.2 ms for flash	After the alternate system image is copied to RAM, the chip resets. The reset does not copy the ROM to RAM.
SVC~ Pin Initialization	100 µs	
State Initialization	No initialization required: 25 µs Initialization required: 50.8 µs + (52 ms for I²C EEPROM or 35 ms for SPI EEPROM)	If the EEPROM is uninitialized, the chip uses the default communication parameters, copies them to the external EEPROM, and enters the applicationless state.
Extended RAM Initialization	7.81 ms per 1 KB of extended RAM at 80 MHz	
Random Number Seed Calculation	0	This task runs in parallel with other tasks.
System RAM Set-up	21 000 clock cycles + (600*B clock cycles)	B is the number of application or network buffers allocated.
Communication Port Initialization	0	This task runs in parallel with other tasks.
Checksum Initialization	3400 clock cycles + (175*M clock cycles)	M is the number of bytes to be checksummed.
One-Second Timer Initialization	6100 clock cycles	
Scheduler Initialization	≥ 7400 clock cycles	Assumes a trivial initialization task, no reset task and the configured state.

Example: For an FT 5000 Smart Transceiver configured to run at 80 MHz, with no EEPROM initialization required, at least 10 application or network buffers, 6 KB of SPI EEPROM non-volatile memory, and 26 KB of extended RAM, with a 5 KB application, the total time required for reset is approximately 377.05 ms:

- 203 ms is required to initialize the RAM variable space.
- 103.2 ms is required to shadow the EEPROM NVM to RAM.
- 43 ms is required to copy the system firmware image from ROM to RAM.
- 16 ms is required for stack initialization and BIST.
- 11.2 ms is required to checksum the 5 KB application.

- The remaining time (0.65 ms) encompasses all of the other reset steps.

SVC~ Pin

The **SVC~** pin alternates between input and open-drain output at a 76 Hz rate with a 50% duty cycle. When it is an output, it can sink up to 8 mA for use in driving an LED. When it is used exclusively as an input, it uses an optional external pull-up to bring the input to an inactive-high state.

Under control of the Neuron firmware, this pin is used during configuration, installation, and maintenance of the device containing the Series 5000 chip. The firmware flashes the LED at a 1/2 Hz rate when the Series 5000 chip has not been configured with network address information. Grounding the **SVC~** pin causes the Series 5000 chip to transmit a network management message containing its unique 48-bit Neuron ID and the application's program ID. This information can then be used by a network management tool to install and configure the device. **Table 26** lists the state of the Service LED for various device states. The Neuron firmware samples the **SVC~** pin whenever it is not actively driving the pin low.

A typical circuit for the **SVC~** pin LED and push-button is shown in **Figure 33**. During reset, the **SVC~** pin is pulled high by its internal pull-up resistor.

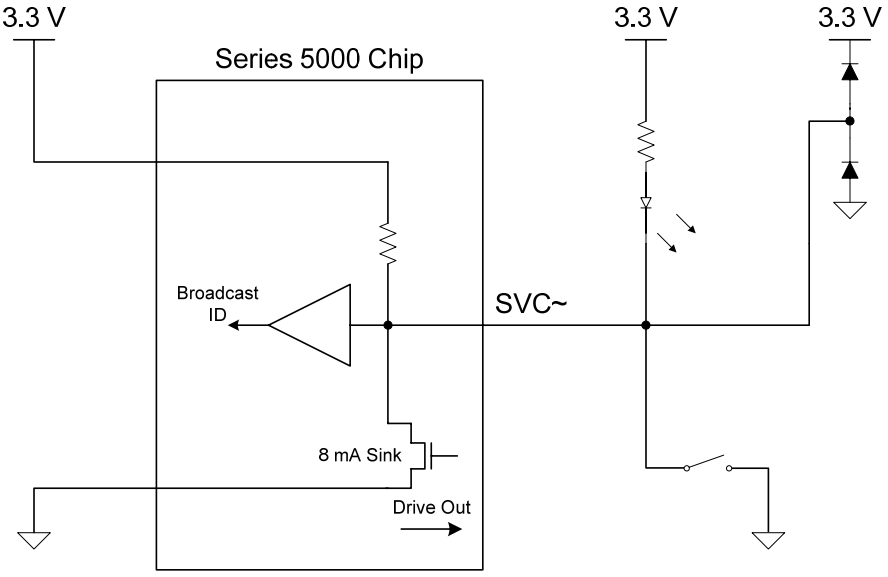


Figure 33. SVC~ Pin Circuit

Table 26. Service LED Behavior during Different States

Device State	State Code	Service LED
Applicationless and Unconfigured	3	On
Unconfigured (but with an Application)	2	Flashing
Configured, Hard Offline	6	Off

Device State	State Code	Service LED
Configured	4	Off
Defective External Memory	—	On

The **SVC~** pin is active low, and the service pin message is sent once per **SVC~** pin transition. The service pin message goes into the next available non-priority output network buffer.

Integrity Mechanisms

The Neuron architecture for a Series 5000 chip includes mechanisms for maintaining system integrity by ensuring processor integrity and application integrity.

Processor Integrity

To maintain processor integrity while an application is running, the Neuron architecture provides a set of interrupts for various error conditions that allow the application or firmware to continue to run. There are certain error conditions that, without interrupt support, would cause the processor to stop execution and possibly cause a reset of the device. A Series 5000 chip handles the following error conditions with system-level traps:

- Watchdog timer timeout
- Memory-protection violations for writing to system image
- Stack exceptions, including underflow, overflow, and collision conditions for the data stack, return stack, and ISR stack
- Execution of an illegal Neuron assembly language opcode
- Execution of the Neuron assembly language **HALT** instruction

A system-level trap is highest level of interrupt and is non-maskable, that is, it cannot be disabled. For each of these traps, the system firmware handles the interrupt, initiates a reset if necessary, and updates the error log for the chip.

System Firmware Image

The 16 KB of RAM from memory address 0x0000 to address 0x3FFF holds the executing copy of the Neuron firmware that is copied from on-chip ROM (or from an external non-volatile memory device for an updated system image). This memory area is write protected so that an application program cannot alter the system firmware. Attempted writes to this memory area trigger a memory-protection violation trap, which causes the chip to reset.

Application Integrity Using Checksums

To ensure application integrity, the Neuron firmware maintains a checksum of the application image. The checksum is a single byte, and is the two's complement of the sum of all bytes that it covers. The checksums is verified during reset processing, and also on a continual basis through a background diagnostic process.

The application image checksum covers the application code in both on-chip EEPROM and any application code in extended EEPROM or flash memory. The default behavior is that an

application checksum error causes the device to go to the applicationless state. Application read/write data residing in EEPROM or flash is not checksummed.

No checksum is computed if the device is in the applicationless state.

Upon detecting a checksum error, the reset process forces the appropriate state and logs an error in the error log. A checksum must fail twice during reset processing for it to be considered in error. If the application checksum is bad, and no application recovery options are set, an application checksum error is logged, and the device state is changed to applicationless.

If the application checksum is bad, and an application recovery option is set, and the boot application does not contain references to any flash, EEPROM, or RAM code, or there are no checksum errors in any of these regions, then the application is recovered. Otherwise, an application checksum error is logged and the device state is changed to applicationless.

3

Hardware Design Considerations

This chapter describes PCB layout guidelines for Series 5000 chips, and describes how to use an FT 5000 Smart Transceiver with a host microprocessor.

PC Board Layout Guidelines

Electrostatic discharge (ESD) and electromagnetic interference (EMI) are two of the most important design considerations when laying out the PCB for a device. See Chapter 4, *Design and Test for Electromagnetic Compatibility*, on page 87, for more information about ESD and EMI design considerations.

Tolerance of ESD and other types of network transients requires careful layout for power, ground, and other device circuitry. In general, ESD currents return to Earth ground or to other nearby metal structures. The device's ground scheme must be able to pass this ESD current between the network connection and the device's external ground connection without generating significant voltage gradients across the device's PCB. The low-inductance star-ground configuration accomplishes this task. The star-ground configuration conducts transients out of the device with minimal disruption to other function blocks.

The following list describes the general features of a careful PCB design layout for FT 5000 Smart Transceivers and Neuron 5000 Processors:

Star-Ground Configuration: The various blocks of the device that directly interface with off-board connections (the network, any external I/O, and the power supply cable) should be arranged so that the connections are together along one edge of the PCB. This arrangement allows any transient current that comes in by one connection to flow back out of the device by one of the other connections.

If connection is made between the PCB ground and a metal enclosure, that connection should be made using a low-inductance connection (like a short standoff) in the center of the star ground. The center of the star ground is anywhere within the common ground area around the off-board connections.

For a 4-layer PCB, the ground plane serves to distribute ground from the center of the star ground out to the various function blocks in the floorplan. For a 2-layer PCB, ground pours should be placed on the bottom layer (and also on the top layer where possible) in order to connect the grounds of the various function blocks to the center of the star ground.

EMC Keepout Area: The area around the FT 5000 Smart Transceiver network connection traces and components should be considered "ESD Hot", and other traces and components (and inner planes) should be kept at least 3.5 mm (0.14 inch) away from the network connection traces and components to prevent ESD arc-overs. In addition, digital signal traces (and other high-speed switching signal traces) should be routed around this keep out area. If you route signals under this area, be sure to add a return plane (ground or power) between the network connection trace layer and the other signal layers.

The PCB layout should be designed so that substantial ESD hits from the network discharge directly to the star-ground center point. Placing a 470 V MOV near the network connector and near the center of the star ground shunts the majority of the network ESD hit energy directly to the star center, which helps to limit the transient current that passes through the FT-X3 transformer.

The PCB layer ground at the center of the star-ground should have a low-inductance return to an external metal package if there is one. If there is no metal package, then this ground area should connect to the ground areas near the power supply connector and the external I/O connectors, as applicable. The transient current that is clamped by the MOV should be routed off of the PCB as directly as possible, without any

opportunity to run through the Series 5000 chip itself, and any other circuitry, such as a host microprocessor.

Transceiver-Side Clamp Diodes: Two diodes clamp the FT 5000 Smart Transceiver side of the FT-X3 transformer between V_{DD33} and ground. The V_{DD33} and ground connections between the diodes and the transformer must be made with short, wide traces using a low inductance technique, which ensures that the secondary transient energy (remaining after the primary discharge through the MOV) does not disrupt the FT Smart Transceiver. The V_{DD33} and ground connections of the diodes are designed to return transient currents to the star-ground center point.

Network-Side Clamp Diodes: Four diodes clamp the network side of the FT-X3 transformer to ground through the MOV during ESD and surge transients. The connections between the diodes and the MOV must be made using low inductance traces, which ensures that secondary transient energy remaining after the primary discharge through the MOV does not disrupt the FT Smart Transceiver. The connection of the MOV is designed to return transient currents to the star-ground center point.

Ground Return for a Series 5000 Chip: A FT 5000 Smart Transceiver has internal protection circuitry built into its NETP and NETN pins (the CP0 and CP1 pins for a Neuron 5000 Processor). When an ESD or surge transient comes in from the network, the portion of the transient that makes it to the Series 5000 chip is clamped to the chip's V_{DD33} power pins and ground pins. V_{DD33} is bypassed to ground at the Series 5000 chip, so the transient current returns to the center of the star ground through the ground layer for a 4-layer PCB, or the ground pours for a 2-layer PCB. Be sure to provide a short and wide ground path from the Series 5000 chip back to the center of the star ground.

Ground Planes: As ground is routed from the center of the star out to the function blocks on the board, planes or very wide traces should be used to lower the inductance (and therefore the impedance) of the ground distribution system.

V_{DD33} Decoupling Capacitors: A good rule of thumb is to provide at least one V_{DD3} decoupling capacitor to ground for each V_{DD33} power pin on an IC in the design. For SMT devices like a Series 5000 chip, each decoupling capacitor should be placed on the top layer with the chip, and placed as close as possible to the chip to minimize the length of V_{DD33} trace between the capacitor and the chip's V_{DD33} pad. The ground end of the capacitor should have a wide, short connection to ground. Keeping these connections short and wide reduces their inductance, which improves the effectiveness of the decoupling. SMT capacitors with a value of 0.1 μF work well for decoupling, as long as the connections are kept very short. If you use ESD clamp diodes between V_{DD33} and ground on I/Os, there should generally be at least one decoupling capacitor for every two diode clamps, placed very close to those diode clamps.

Host Microprocessor Kept Away From Network Connection: The (optional) host microprocessor (for a ShortStack device or an FTXL device) is a potential source of digital noise that could cause radiated EMI problems if that noise is allowed to couple onto the external network, power, or I/O wiring. To help prevent this coupling, the host microprocessor and any other noisy digital circuitry should be kept away from the network side of the Series 5000 chip. For example, place the host microprocessor on the opposite side of the Series 5000 chip from the network, power, and I/O connectors.

Figure 34 on page 80 shows a portion of the top layer of a 4-layer printed circuit board (PCB) layout for the FT 5000 Smart Transceiver, along with the other building blocks of a PCB design. A PCB layout for a Neuron 5000 Processor would be similar to that shown in **Figure 34**.

Variations on this suggested PCB layout are possible as long as the general principles discussed in this chapter are followed. Through-hole capacitors and diodes can be used, but SMT components are generally superior because of their lower series inductance.

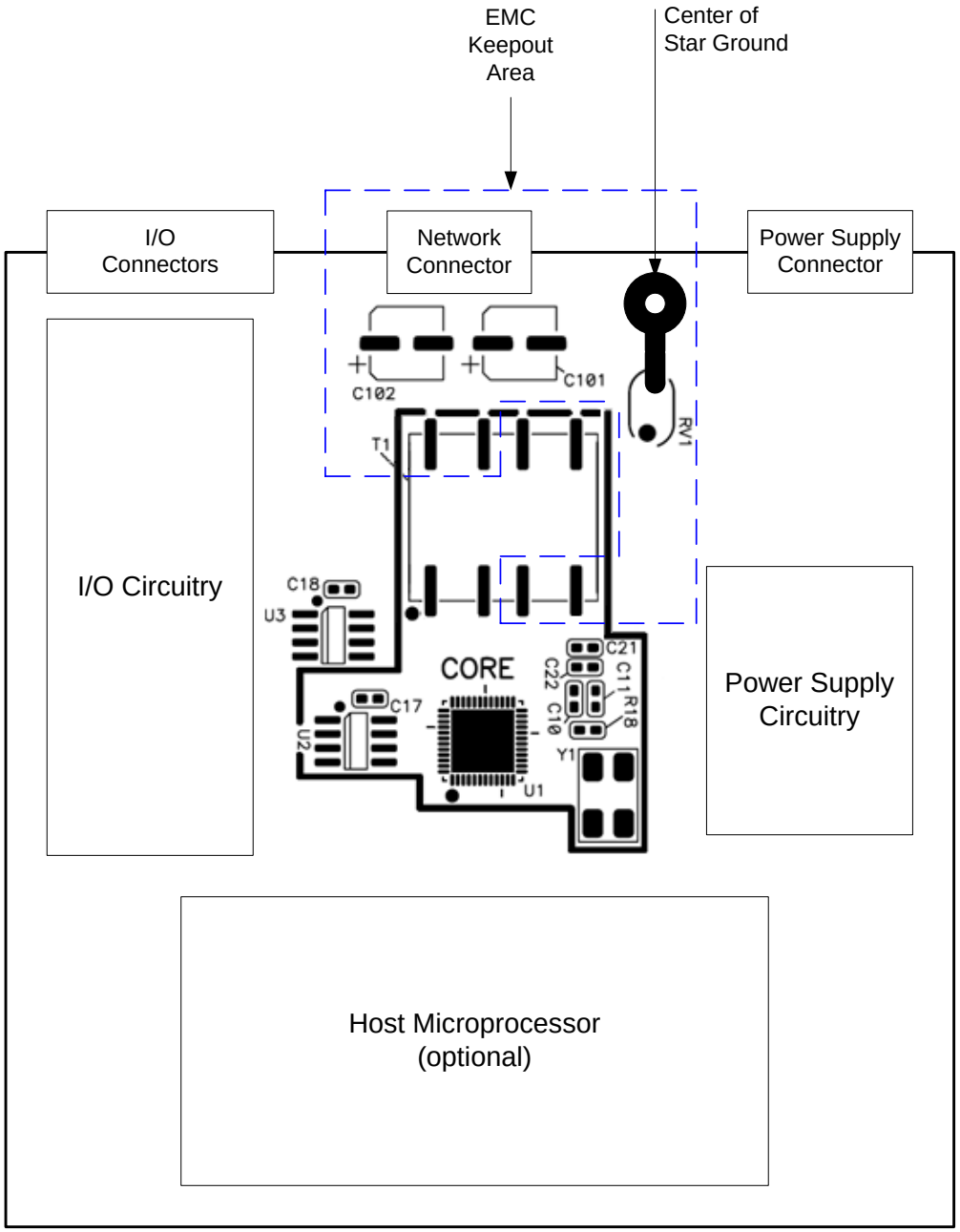


Figure 34. Example PCB Layout Design for an FT 5000 Smart Transceiver

For a development and test board, you can use a socket for the Neuron 5000 Processor or FT 5000 Smart Transceiver, such as the 48LQ50S17070 open-top dual latch QFN socket from Plastronics Socket Company, Inc., or the S-MLF-00-048-A1 open-top QFN/MLF socket from Emulation Technology, Inc.

Using a Series 5000 Chip with a Host Microprocessor

An FT 5000 Smart Transceiver or a Neuron 5000 Processor is designed to function as standalone microcontroller running a Neuron C application for a LONWORKS device. However, some LONWORKS devices run applications that require more memory, I/O, or processing capabilities, than a single Smart Transceiver or Neuron 5000 Processor can provide. For such applications, the device can use two processor chips working together:

- An Echelon Smart Transceiver or Neuron 5000 Processor
- A microprocessor, microcontroller, or embedded processor in a field-programmable gate array (FPGA) device

Compared to the single-chip device, the Smart Transceiver or Neuron 5000 Processor implements only a subset of the LonTalk protocol layers. The host processor implements the remaining layers and runs the device's application program. The Smart Transceiver and the host processor communicate with each other through a link-layer interface.

For Series 5000 Chips, Echelon provides the LonTalk Platform for ShortStack Micro Servers solution for creating host-based LONWORKS devices. The ShortStack Micro Server is firmware that runs on a Series 5000 Chip. The Micro Server implements layers 1 through 5 (and part of layer 6) of the ISO/IEC 14908 protocol, including the physical interface for the LONWORKS communications channel. A ShortStack Micro Server requires a host processor to implement the remaining layers (layers 6 and 7) of the protocol. The ShortStack development tools also allow you to create a custom Micro Server, which you can load into a Series 5000 Chip.

For ShortStack device development, you use the C programming language. You use the Echelon LonTalk Interface Developer utility to create the application framework. Your application uses an ANSI C API, the Echelon LonTalk Compact API, to manage communications with the ShortStack Micro Server and devices on the LONWORKS network.

ShortStack Device

The ShortStack Micro Server uses the IO0-IO11 pins with a *serial I/O model*, which defines a half-duplex asynchronous or synchronous serial interface. The serial I/O interface can use either the Serial Communications Interface (SCI) or the Serial Peripheral Interface (SPI).

The hardware interface for a ShortStack Micro Server is comprised of the serial communications interface, the pin assignments and characteristics for the Series 5000 Chip, and the pin assignments and characteristics for the host microprocessor or microcontroller.

See the *ShortStack User's Guide* (078-0365-01B) for more information about designing a ShortStack device.

The ShortStack SCI Interface

A ShortStack Micro Server on a Series 5000 Chip has 12 I/O pins that control the configuration of the Micro Server and provide the interface to the host processor. The IO3 input pin selects the serial interface: SCI or SPI. The serial interface also determines the usage of the other I/O pins. **Table 27** on page 82 summarizes these pin assignments for the SCI interface.

Recommendation: If your host processor can support both the SCI and SPI interfaces, use the SCI interface because it is typically faster and easier to implement, both in hardware and software.

Table 27. ShortStack Micro Server Pin Assignments for the SCI Interface

Series 5000 Chip Pin	Signal Name	Direction
IO0	CTS~	Output
IO1	HRDY~	Input
IO2	N/A	No connection
IO3	SPI/SCI~	Input (tie to GND for SCI)
IO4	RTS~	Input
IO5	Serial Bit Rate Bit 0 (SBRB0; LSB)	Input
IO6	Serial Bit Rate Bit 1 (SBRB1; MSB)	Input
IO7	N/A	No connection
IO8	RXD	Input
IO9	N/A	No connection
IO10	TXD	Output
IO11	N/A	No connection

Notes:

- Signal direction is from the point of view of the Smart Transceiver (Micro Server).
- N/A = Not applicable.

The SCI communications interface shown in **Figure 35** on page 83 is implemented with the following inputs and outputs:

- Interface Selector (SPI/SCI~): Tied to GND to specify the SCI interface.
- Request to Send (RTS~): When asserted, indicates that the host processor has data to send. The serial driver asserts this signal low if the CTS~ signal is deasserted (high), and waits for the Micro Server to assert CTS~.
- Clear to Send (CTS~): When asserted, informs the host processor that Micro Server is ready to receive data from the serial driver. Set by the Micro Server after the host has asserted RTS~. The Micro Server keeps CTS~ asserted until it receives the expected number of bytes. The host must deassert RTS~ after the CTS~ acknowledgement has been received, and must start transmitting the related data with minimal delay (under 25 ms for an 80 MHz Series 5000 Micro Server).

- Host Ready (HRDY~): When deasserted, indicates that the host processor is temporarily not able to accept data transfers from the Micro Server. This signal is optional; if your application does not use this signal, you must tie it low so that it is continually asserted (to specify that the host is always ready to accept data transfers). Typical host applications deassert the HRDY~ signal in the following situations:
    - During power-up and initialization following a reset (until the serial driver is ready to receive data from the Micro Server)
    - When enqueuing received data, following a completed uplink transfer
- Receive Data (RXD): Transfers data from the host processor to the Micro Server.
- Transmit Data (TXD): Transfers data from the Micro Server to the host processor.
- Serial Bit Rate Bit 0 (SBRB0) and Serial Bit Rate Bit 1 (SBRB1): Together set the communications bit rate.

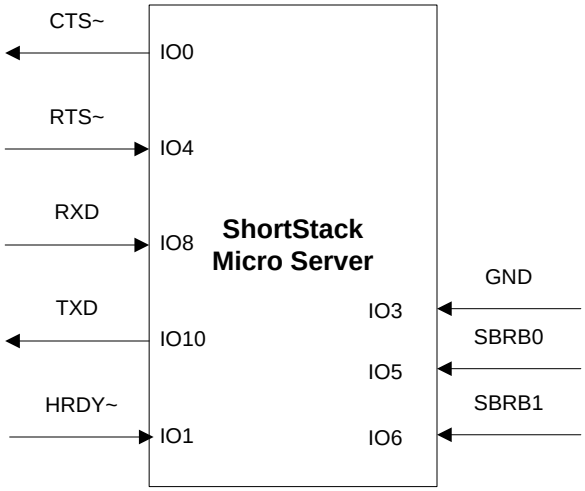


Figure 35. ShortStack SCI Communications Interface

The ShortStack SPI Interface

A ShortStack Micro Server on a Series 5000 Chip has 12 I/O pins that control the configuration of the Micro Server and provide the interface to the host processor. The IO3 input pin selects the serial interface: SCI or SPI. The serial interface also determines the usage of the other I/O pins. **Table 28** summarizes these pin assignments for the SPI interface.

Table 28. ShortStack Micro Server Pin Assignments for an SPI Interface

Series 5000 Chip Pin	Signal Name	Direction
IO0	R/W~	Output
IO1	SCLK	Output
IO2	SS~	Output
IO3	SPI/SCI~	Input (tie to V_{DD} for SPI)

Series 5000 Chip Pin	Signal Name	Direction
IO4	TREQ~	Input
IO5	Serial Bit Rate Bit 0 (SBRB0; LSB)	Input
IO6	Serial Bit Rate Bit 1 (SBRB1; MSB)	Input
IO7	MOSI	Output
IO8	MISO	Input
IO9	N/A	No connection
IO10	HRDY~	Input
IO11	N/A	No connection

Notes:

- Signal direction is from the point of view of the Smart Transceiver (Micro Server).
- N/A = Not applicable.

The SPI communications interface shown in **Figure 36** on page 85 is implemented with the following inputs and outputs:

- Interface Selector (SPI/SCI~): Tied to V_{DD} to specify the SPI interface.
- Host Ready (HRDY~): When deasserted, indicates that the host processor is temporarily not able to accept any data transfers from the Micro Server. This signal is optional; if your application does not use this signal, you must tie it low so that it is continually asserted (to specify that the host is always ready to accept data transfers). Typical host applications deassert the HRDY~ signal in the following situations:
    - During power-up and initialization following a reset (until the serial driver is ready to receive data from the Micro Server)
    - When enqueuing received data, following a completed uplink transfer
- Master Input Slave Output (MISO): Transmits control and data bytes from the host to the Micro Server. Data is presented at the falling clock edge, and sampled at the rising edge, MSB first, 8 bit.
- Master Output Slave Input (MOSI): Transmits control and data bytes from the Micro Server to the host. Data is presented at the falling clock edge, and sampled at the rising edge, MSB first, 8 bit.
- Serial Clock (SCLK): Provides a clock signal for all data transfers. Data is presented at the falling clock edge, and sampled at the rising edge.
- Slave Select (SS~): When asserted, re-synchronizes the interface by resetting the state of the host SPI interface in case of bit misalignment. This signal can be used to drive an (active-low) Enable signal on the host's SPI interface, when necessary.

- Transmit Request (TREQ~): When asserted, indicates that the host processor is ready to send a byte. The host asserts this signal low and waits for the Micro Server to assert the R/W~ pin.
- Read/Write (R/W~): Indicates which direction is active during a byte transfer (low indicates write). The R/W~ pin is low during a transfer from the Micro Server to the host (MOSI); the R/W~ pin is high during a transfer from the host to the Micro Server (MISO).
- Serial Bit Rate Bit 0 (SBRB0) and Serial Bit Rate Bit 1 (SBRB1): Together set the communications bit rate.

The ShortStack SPI interface supports only one host processor on the bus; it does not support any other SPI devices or microprocessors on the bus.

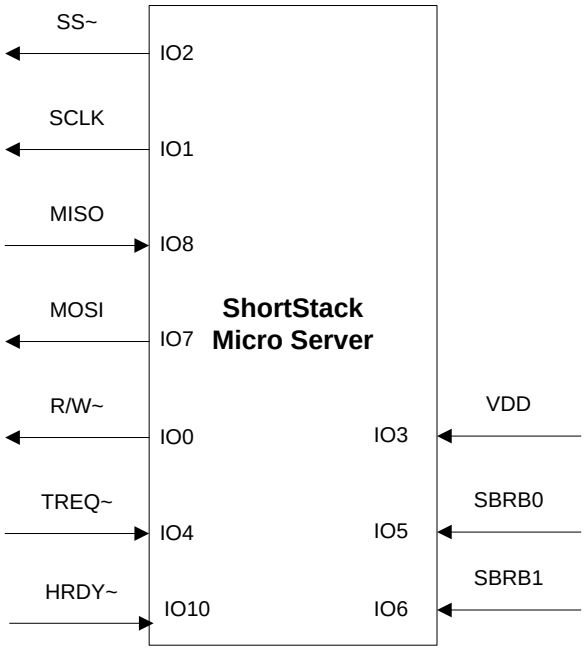


Figure 36. ShortStack SPI Communications Interface

4

Design and Test for Electromagnetic Compatibility

This chapter describes electromagnetic compatibility design considerations for Series 5000 devices and the tests that you perform to ensure immunity.

Overview

A product that is designed for electromagnetic compatibility (EMC) must be able to pass rigorous tests for immunity to external interference and demonstrate low electromagnetic interference (EMI) emissions. If the product will be sold in the European Union (EU), the product must demonstrate appropriate EMC levels to pass European Conformité Européene[4] (CE) Marking tests. Even if the product will not be sold in the EU, immunity testing helps you to design a better, more robust product.

Echelon has performed immunity tests for CE Marking on Series 5000 devices, and has also performed additional tests to ensure immunity and low emissions. Specifically, Echelon has performed the following immunity tests:

- Electrostatic discharge (ESD) testing (both air and contact discharge) for compliance with Comité Européen de Normalisation[5] (CEN), standard EN 61000-4-2
- Radiated radio frequency (RF) immunity testing for compliance with CEN standard EN 61000-4-3
- Burst testing for compliance with CEN standard EN 61000-4-4
- Surge testing for compliance with CEN standard EN 61000-4-5
- Conducted RF Immunity testing for compliance with CEN standard EN 61000-4-6

Summary and Testing Results on page 99 summarizes the results of Echelon's testing for Series 5000 devices.

You need to perform your own immunity testing for Series 5000 devices that you design and build.

The test results for each of the CEN standard EN 61000-4-x tests are interpreted within the scope of the product's specifications and standard operating conditions. A product's test results fall into one of the following categories, which are referred to as "performance criteria":

1. Normal product performance within specified limits
2. Temporary degradation or loss of function, or performance, that is self-recoverable
3. Temporary degradation or loss of function, or performance, that requires operator intervention to reset the system
4. Degradation or loss of function that is not recoverable

For example, within a LONWORKS network, losing one network packet because of an ESD or surge hit likely meets category 1 because the Series 5000 chip resends network data that is not acknowledged as received.

For more information about the CEN standard tests and to purchase copies of the standards documents, go to the Information Handling Services (IHS) Global page: global.ihs.com.

[4] European Conformity

[5] European Committee for Standardization

Achieving High Immunity

Achieving good immunity to ESD and other types of network transients requires good layout of the power, ground, and other device circuitry. In general, an ESD current will return to Earth ground or to other nearby metal structures. The device's ground scheme must be able to pass this ESD current between the network connection and the device's external ground connection without generating significant voltage gradients across the device.

To achieve high immunity, ensure that your design conforms to the following general guidelines:

- Use a star-ground configuration for your device layout
- Limit entry points in the device for ESD current
- Provide ground guarding for switching power supply control loops
- Provide good decoupling for V_{DD33} and V_{DD18} inputs
- Maintain separation between digital circuitry and cabling for the network and power

In a star-ground configuration, the power supply, network coupling circuit, and any I/O circuitry are distributed on the PCB in the form of a star, with the respective connectors and any chassis ground connections forming the center of the star. The host microprocessor and other sensitive circuitry should be located away from the center of the star. The goal of the star-ground configuration is to conduct transients that enter the device on one cable out of the device through the other cables, with minimal disruption to other functional areas of the device. If the device has a metal chassis, ESD and other transients generally return to that chassis by way of the star-ground center point. If the device's logic ground is connected to this chassis ground, you should only connect it at this single point, with a short standoff, in the center of the star. Keep noisy digital lines (such as host microprocessor memory array lines) away from the metal enclosure walls. If a device is housed in a plastic enclosure and is powered with an isolating transformer, an explicit Earth ground or chassis ground might not be available. In this case, it is still important for the network connector and power supply connector to be located near the center of the star.

Switching power supply control loops can pick up radio-frequency (RF) noise and rectify it. RF immunity depends on limiting the pickup of such RF noise, so you need to provide sufficient ground guarding for the switching power supply control loops.

To provide good decoupling for V_{DD33} and V_{DD18} inputs, you should distribute V_{DD33} and V_{DD18} through low inductance traces and planes in the same manner as ground. All of the ground pins on an FT 5000 Smart Transceiver or Neuron 5000 Processor should be connected with either a ground plane (for PCBs with at least 4 layers) or a ground pad directly underneath the FT 5000 Smart Transceiver or Neuron 5000 Processor on the bottom of the board (for PCBs with 2 layers). Place one SMT decoupling capacitor per power pin between the FT 5000 Smart Transceiver or Neuron 5000 Processor and ground. Place each decoupling capacitor on the top side of the PCB, with the connection to its V_{DD33} or V_{DD18} pin as short as possible.

Maintaining separation between digital circuitry and cabling for the network and power limits RF crosstalk to any traces associated with the network or power supply (and any I/O lines that leave the device).

Electrostatic Discharge

Electronic systems in industrial and commercial environments frequently encounter electrostatic discharge (ESD). An ESD event is a momentary electric current that flows

between electrically charged objects at different voltage potentials (one of which can be ground). The most common form of ESD is an electric spark, but not all ESD hits are accompanied by a spark.

A reliable system design must consider the effects of ESD, and take steps to protect sensitive components. Static discharges occur frequently in low-humidity environments when human operators touch electronic equipment. Keyboards, connectors, and enclosures can also provide paths for static discharges to reach ESD-sensitive components. In addition, the European Community has adopted requirements for ESD testing.

There are two general approaches to minimizing the effects of ESD for an electronic product:

- Seal the product to prevent static discharges from reaching sensitive circuits inside the package.
- Design the grounding of the product so that ESD hits to user-accessible metal parts can be shunted around sensitive circuitry.

Because a LONWORKS network connector is likely to be user-accessible, it is generally not possible to seal Series 5000 devices completely. However, the product's package should be designed to minimize the possibility of an ESD hit arcing into the device's circuit board. If the product's package is made of plastic, then the PCB should be supported within the package so that unprotected circuitry on the PCB is not adjacent to any seams in the package. The PCB should not touch the plastic of an enclosure near a seam, because a static discharge can creep along the surface of the plastic, through the seam, and arc onto the PCB.

After an ESD hit arcs into the product, the current from the discharge flows through all possible paths back to Earth ground. The grounding of the PCB, and the protection of user-accessible circuitry, must allow these ESD return currents to flow back to Earth ground without disrupting normal circuit operation of the Series 5000 chip, its host microprocessor (if any), or other device circuitry. Generally, this means that you should ensure that the ESD currents are shunted to the center of a star ground configuration (as described in *Achieving High Immunity* on page 89), and then out to the product's chassis or Earth ground connection. If the device floats with respect to Earth ground, the ESD current can return capacitively to Earth by the network wire, the power supply wires, and the PCB ground plane.

Testing for ESD to comply with the EN 61000-4-2 ESD immunity test standard is performed on a metal test table using an ESD transient generator. Level 4 testing involves injecting up to ±8 kV contact discharges and up to ±15 kV air discharges into the product under test. Depending on the product design, you can inject the discharges at the network connector, power connector, or other user-accessible areas. During the test, the device should continue to operate normally, with occasional packet loss due to the ESD hits.

Electromagnetic Interference

The high-speed digital signals that are associated with microcontroller designs can generate unintentional electromagnetic interference (EMI). This interference is emitted by electrical circuits that carry rapidly changing signals that generate RF currents that can cause unwanted signals to be induced in other circuits. These unwanted signals can interrupt or degrade the effective performance of those other circuits.

Products that use an FT 5000 Smart Transceiver or Neuron 5000 Processor will generally need to demonstrate compliance with EMI limits enforced by various regulatory agencies. In the USA, the Federal Communications Commission (FCC) requires that industrial products comply with Title 47 of the Code of Federal Regulations (CFR) Part 15, Subpart A, and it requires that products which can be used in residential environments comply with Subpart

B. The European comité européen de normalisation electrotechnique[6] (CENELEC) EN 55022 standard and the international comité international spécial des perturbations radioélectriques[7] (CISPR) 22 standard both require similar compliance, and most countries throughout the world require compliance with similar regulations.

A typical Series 5000 device has several digital I/O signals that switch in the kHz to MHz range. These signals generate voltage noise near the signal traces, and also generate current noise in the signal traces and power supply traces. The goal of good device design is to keep this voltage and current noise from coupling out of the product's package. Thus, careful PCB layout can ensure that a Series 5000 device achieves the desired low level of EMI emissions.

It is important to minimize the leakage capacitance from circuit traces in the device to any external pieces of metal near the device, because this capacitance provides a path for the digital noise to couple out of the product's package. **Figure 37** shows the leakage capacitances to Earth ground from a device's logic ground ($C_{leak,GND}$) and from a digital signal line in the device ($C_{leak,SIGNAL}$).

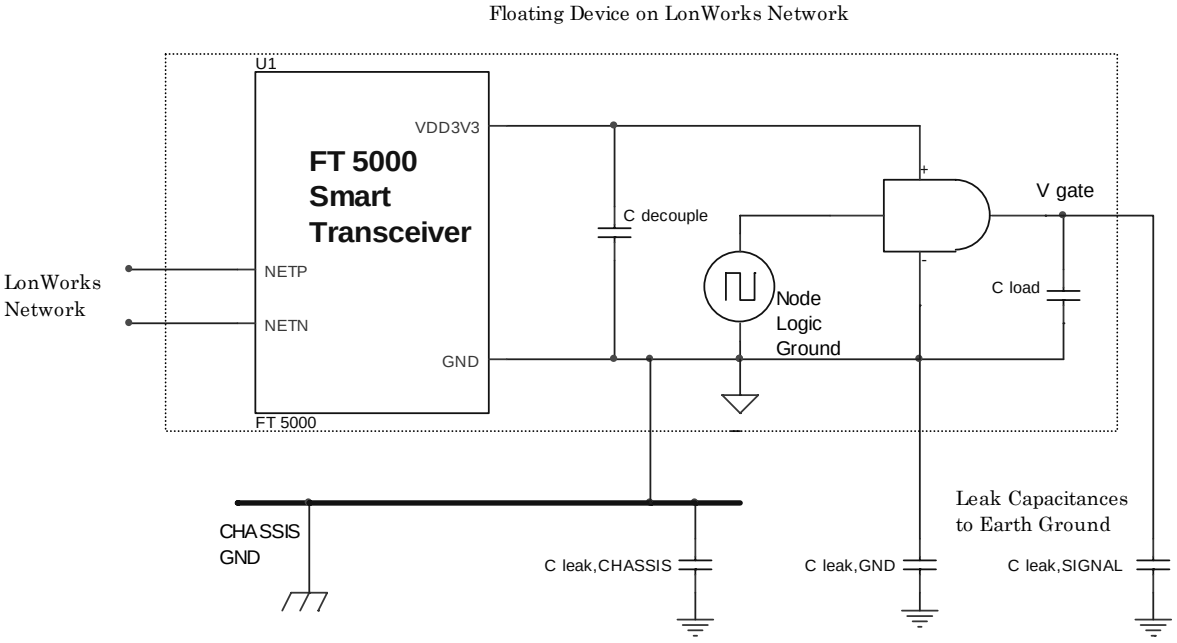


Figure 37. Parasitic Leakage Capacitances to Earth Ground

If the Series 5000 device is housed inside a metal chassis, that chassis likely has the largest leakage capacitance to other nearby pieces of metal. If the device is housed inside a plastic package, use PCB ground guarding to minimize $C_{leak,SIGNAL}$. Effective guarding of digital traces with logic ground reduces $C_{leak,SIGNAL}$ significantly, which reduces the level of common-mode RF currents driven onto the network cable.

For a device mounted near a piece of metal, especially metal that is Earth grounded, any leakage capacitance from fast signal lines to that external metal provides a path for RF currents to flow. When V_{gate} is pulled down to logic ground, the voltage of logic ground with respect to Earth ground increases slightly. When V_{gate} is pulled up to V_{DD33}, logic ground is pushed down slightly with respect to Earth ground.

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[6] European Committee for Electrotechnical Standardization

[7] International Special Committee on Radio Interference

As $C_{leak,SIGNAL}$ increases, a larger current flows during V_{gate} transitions, and more common-mode RF current couples onto the network twisted pair. This common-mode RF current can generate EMI in the 30-500 MHz frequency range, well in excess of CFR Part 15 Subpart B or CISPR 22 Class B levels, even when the capacitance of $C_{leak,SIGNAL}$ from a clock line to Earth ground is less than 1 pF. Thus, it is essential to guard clock lines (and keep them on the top side of the PCB, if possible) for meeting Subpart B limits.

By using 0.1 µF or 0.01 µF decoupling capacitors at each digital IC power pin, you can reduce V_{DD33} and logic ground noise. You can then use logic ground as a ground shield for other noisy digital signals and clock lines.

In addition, some amount of filtering might also be required on a Series 5000 device's power supply input, depending on the level of noise generated by the application circuitry. A good way to achieve this filtering is to place ferrite chokes in series with the power input traces adjacent to the power connector. **Figure 38** shows a typical power supply circuit illustrating the placement of these ferrite chokes.

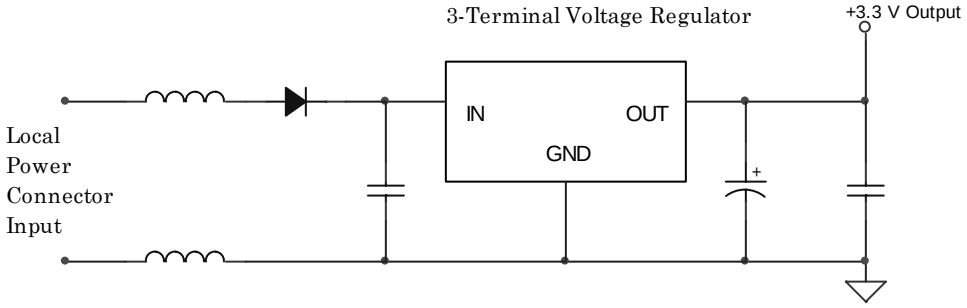


Figure 38. Power Supply Input Filtering Using Ferrite Chokes

Testing for EMI to comply with the CISPR 22 Radio Disturbance Characteristics test standard takes two forms:

- Radiated EMI testing checks for RF noise that radiates from network and power cables (or from inside the device)
- Conducted EMI testing checks for RF noise that radiates from the power supply connection to the AC mains

Compliance with the CISPR 22 Class A standard is required for industrial products, and compliance with the Class B standard is required for products that can be used in residential environments.

The following general rules and guidelines summarize EMI design considerations:

- The faster the system clock speed for a Series 5000 device, the higher the level of EMI.
- Better V_{DD3} decoupling quiets RF noise at the sources (the digital ICs), which lowers radiated EMI.
- A four-layer PCB generates less EMI than a two-layer PCB because the extra layers provide better V_{DD3} decoupling and more effective logic ground guarding.

Radiated and Conducted Immunity

The EN 61000-4-3 RF Susceptibility and EN 61000-4-6 Conducted RF Immunity tests ensure that a device's operation is not impaired by strong electromagnetic fields, such as those generated near cellular phones and portable radios.

The EN 61000-4-3 RF Susceptibility test is generally performed in an RF-shielded anechoic chamber with high-power transmitter-driven antennas aimed at the equipment under test (EUT). During the EN 61000-4-3 RF Susceptibility test, the RF signal generator is set to an amplitude modulation (AM) depth of 80% at 1 kHz, and the frequency is slowly swept from 30 MHz to 1 GHz. With this condition, there are three levels of testing:

- Level 1 subjects the EUT to a 1 V/m field strength
- Level 2, which represents a moderate electromagnetic radiation environment, subjects the EUT to a 3 V/m field strength
- Level 3, which represents a severe electromagnetic radiation environment, subjects the EUT to a 10 V/m field strength

During the EN 61000-4-6 Conducted RF Immunity test, the RF signal generator is set to an AM depth of 80% at 1 kHz, and the frequency is slowly swept from 150 kHz to 80 MHz. With this condition, there are three levels of testing:

- Level 1 injects a common-mode voltage on the EUT's network cable of 1 V_{RMS} (5 V_{P-P} including the 80% AM)
- Level 2, which represents a light industrial environment, injects a common-mode voltage on the EUT's network cable of 3 V_{RMS} (15.3 V_{P-P} including the 80% AM)
- Level 3, which represents a harsh industrial environment, injects a common-mode voltage on the EUT's network cable of 10 V_{RMS} (50.9 V_{P-P} including the 80% AM)

For twisted-pair networks, the preferred test method is the Current Injection method, also called the Bulk Current Injection (BCI) method. A current clamp injects common-mode noise onto the twisted-pair communication cable, and both the auxiliary equipment and the EUT experience similar common-mode noise at their network connections. Even when this wiring passes through a coupling-decoupling network, the RF noise that is present during the test can disrupt wired communication between the auxiliary equipment and an external control PC. Thus, the auxiliary equipment should provide a visual indication of a pass/fail result during the test, rather than requiring a wired connection to a computer to monitor the result.

Figure 39 on page 94 shows a typical setup for EN 61000-4-6 testing of a Series 5000 device with unshielded twisted-pair (UTP) network wire.

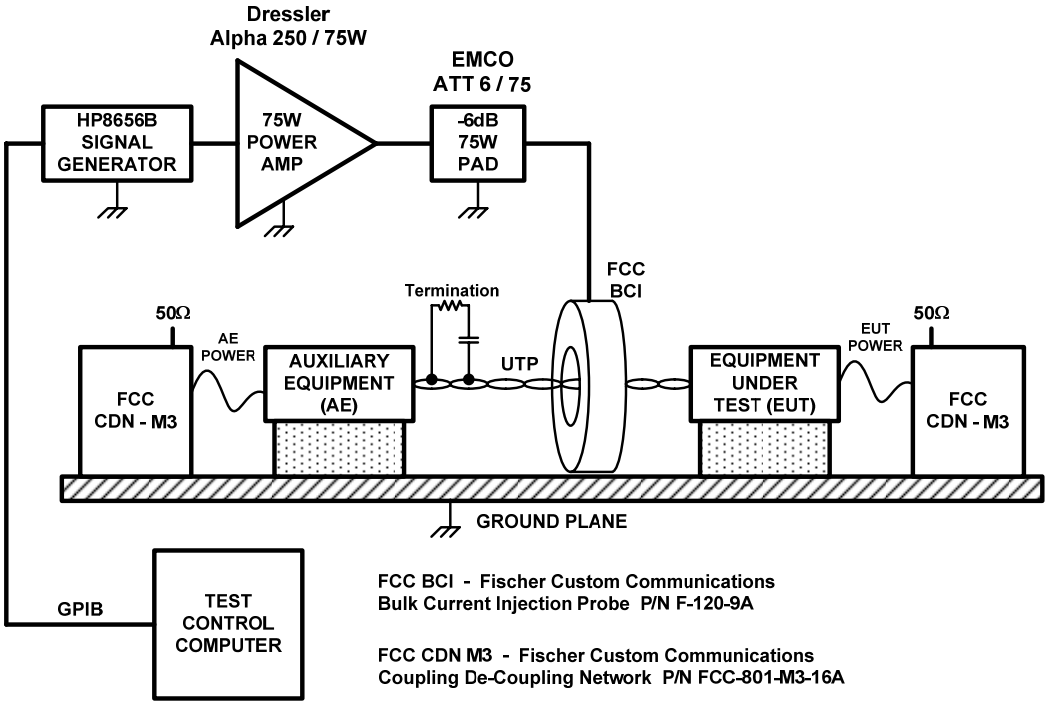


Figure 39. Typical EN 61000-4-6 Test Setup for Unshielded Twisted-Pair (UTP) Wires

For the EN 61000-4-6 tests, the EUT is placed on a 10 cm high, non-conducting support on top of a metal ground plane. If the chassis of the EUT is connected to Earth ground in typical installations, for the test it should be connected directly to the metal ground plane with a short wire. If the EUT is left floating in normal use, there should be no connection between the EUT and Earth ground for the EN 61000-4-6 tests.

Power connections for the auxiliary equipment and EUT should be routed through suitable decoupling devices, such as non-driven M3 "coupling-decoupling" network (CDN) devices. During the network immunity tests, any I/O lines that come out of the auxiliary equipment or the EUT should also pass through a decoupling network. The objective of the BCI current clamp is to drive the large common- mode noise signal into the network cable of the EUT. The M3 CDNs ensure that the power supply inputs to the auxiliary equipment and EUT are not an RF return path.

For shielded twisted-pair (STP) networks, the BCI current clamp injects common-mode noise into the STP cable. The cable shield should be connected to Earth ground with a parallel resistor and capacitor as shown in **Figure 40** on page 95. The resistor is generally 470 kΩ, 0.25 W, 5%. The capacitor is generally 0.1 μF, 10%, metal polyester, with a voltage rating of 100 VDC or higher.

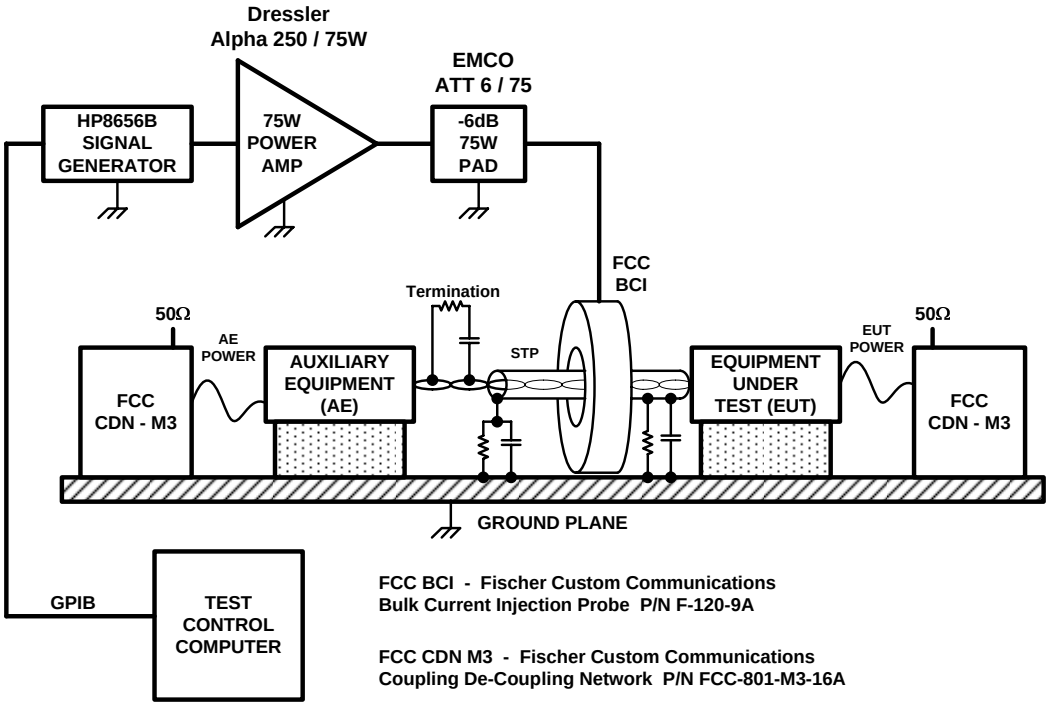


Figure 40. Typical EN 61000-4-6 Test Setup for Shielded Twisted-Pair (STP) Wires

Surge and Burst

For the purposes of EMC testing, a surge is a transient overvoltage of several kV with a rise time that is measured in microseconds or nanoseconds, and with a duration that is measured in microseconds. Compared with fast transient bursts and ESD, surges are relatively slow, but also long lived.

A surge is created by a switching event or insulation fault in the AC power distribution network, or by the switching of a reactive load (such as an electric motor). A surge can also be caused by lightning, but EN 61000-4-5 only indirectly addresses the effects of lightning.

EN 61000-4-5 Surge testing is performed on a non-conducting table using specialized surge generation equipment. The surges are injected directly into the network wiring (in a common-mode fashion) or into the power supply cable through a coupling circuit. During the test, the device should continue to operate normally, with occasional packet loss due to the surges.

There are three levels of network testing that are relevant to Series 5000 devices:

- Level 2 conductively couples a ±1 kV surge into the network
- Level 3 conductively couples a ±2 kV surge into the network
- Level "X" conductively couples a user-defined surge voltage into the network

EN 61000-4-4 Burst testing of the network cable is performed on a non-conducting table, with 1 meter of the network cable clamped in a high-voltage burst generation apparatus. The test capacitively injects high voltage bursts of noise into the network cable. The test injects three bursts onto the network cable each second. During the test, the device should continue to operate normally, with occasional packet loss due to the bursts.

There are two levels of network testing that are relevant to Series 5000 devices:

- Level 3, which represents a typical industrial environment, injects ±1 kV bursts continuously for 60 seconds
- Level 4 which represents a severe industrial environment, injects ±2 kV bursts continuously for 60 seconds

In addition, burst testing is performed on the power supply input cable. For Series 5000 devices, the following levels of power supply input testing are relevant:

- Level 3, which represents a typical industrial environment, injects ±2 kV bursts continuously for 60 seconds
- Level 4 which represents a severe industrial environment, injects ±4 kV bursts continuously for 60 seconds

Lightning Protection

Protection against lightning is required when designing control networks that run outside of buildings.

Building Entrance Protection

Echelon recommends using shielded twisted-pair wire for all networks, or portions of networks, that are run outside of buildings or grounded structures. The shield, as well as the two network lines, should be connected to Earth ground through Data Line Lightning/Surge arresters at each building entry point. This connection conducts excessive energy surges or lightning strike energy directly to Earth and prevents their entry inside the building through the network shield or data line conductors. Therefore, three arresters should be used at each building entrance for shielded twisted-pair wiring.

Network Line Protection

The arresters used on the network data lines must be of the Gas Discharge type. The intrinsically low capacitance to ground of these devices, typically less than 5 pF, minimizes the corruption of any data signals. Due to their low capacitance construction, the use of Gas Discharge devices does not alter the maximum number of devices allowed per network segment.

Important: MOV and TVS protection devices must not be used on the network data lines because of their much higher capacitance (>200 pF) and potentially poor differential capacitance matching. These devices can corrupt, and possibly prevent, network communication between devices.

Shield Protection

Gas Discharge, MOV, or TVS devices can be used for the **shield-to-ground** protection. MOV and TVS devices should not be used to protect the network data lines.

Suggested Gas Discharge Arresters

Three-electrode device configurations are suggested for the data network lines, because they require the use of only one physical device to protect both lines. The network lines should be connected to the two outside ends of the arrester, while the middle terminal must be

connected to a stable Earth ground. Alternatively, two each of two-electrode configurations can be used (contact manufacturer for details). **Table 29** provides a list of three-electrode Gas Discharge device manufacturers.

Table 29. Manufactures of Suggested Gas Discharge Arresters

Vendor and Configuration	Series	Voltage
Sankosha, 3 Electrode www.sankosha-usa.com/arresters.asp?id=2	3H or 3P	90 VDC
Citel, 3 Electrode www.citelprotection.com/citel/gas_cover.htm	BT, BTR, or BTS	90 VDC
Littelfuse, 3 Electrode www.littelfuse.com/series/PMT8.html	PMT8	90 VDC

Figure 41 shows a typical outdoor twisted pair network in which Gas Discharge arresters have been incorporated.

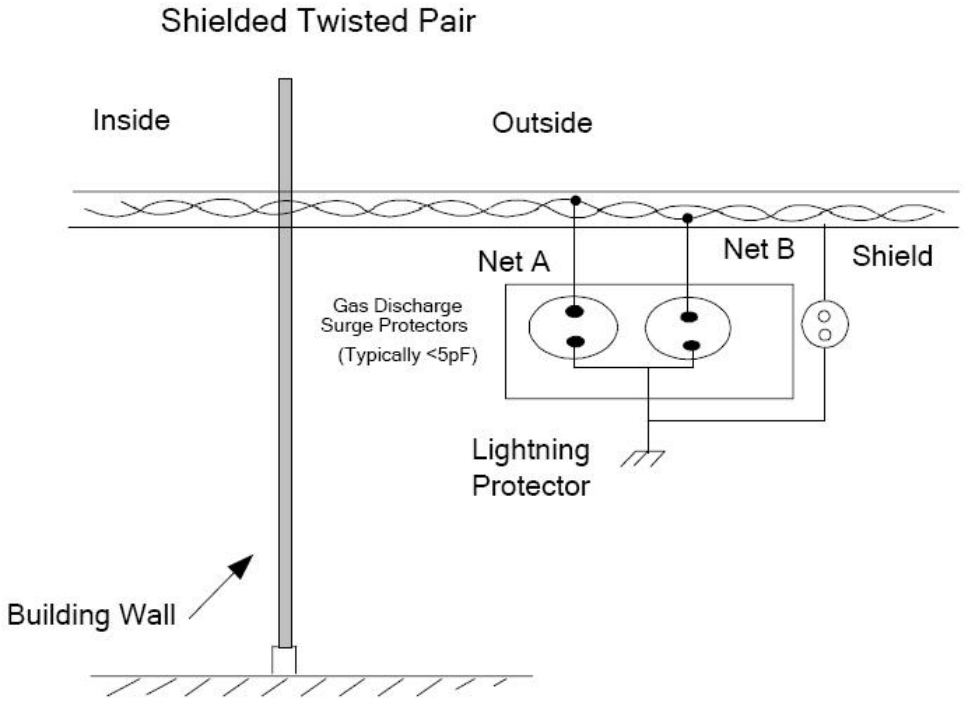


Figure 41. Network and Shield Lightning Protection

When the network data line extends outside of a building or grounded structure, **every** FT 5000 Smart Transceiver or Neuron 5000 Processor device on the network segment, whether located indoors or outdoors, must be equipped with surge protection circuitry. Additionally, protection devices must be added to the network at every point where the network cable exits the building or structure.

Avoiding Magnetic Field Interference

All transformer-based transceivers are vulnerable to stray magnetic fields that can interfere with the transformer coupling. In most environments, stray magnetic field noise is not a concern for FT 5000 Smart Transceivers or Neuron 5000 Processors with external transceivers. However, high frequency external magnetic fields can couple sufficient energy into the transceiver to cause erratic network performance or, in some cases, cause data traffic to cease.

One possible source of stray magnetic fields is a DC-DC switching power supply, or regulator, using unshielded switching inductors located in close proximity to the transceiver. To minimize magnetic coupling into the transceiver, the switching magnetics of power supplies should be kept at least 7.5 cm (3 inches) from the FT 5000 Smart Transceiver or Neuron 5000 Processor with external transceiver. Otherwise, noise induced into the receiver could affect communications.

If you suspect magnetic field interference, you should measure the level of noise at the FT 5000 Smart Transceiver or Neuron 5000 Processor with external transceiver. You can measure the noise induced by a switching power supply by using an oscilloscope with differential probes having at least 5 V common-mode range with 50 dB of common-mode rejection to measure the voltage between the Series 5000 chip's NETP and NETN pins during an interval when there is no packet activity. You can also identify the source of the magnetic noise by moving the suspected source away from the FT 5000 Smart Transceiver or Neuron 5000 Processor with external transceiver by connecting it to at least 15 cm twisted-pair wires and monitoring the noise at the NETP and NETN pins.

The noise between the NETP and NETN pins should be less than 15 mV peak-to-peak differential. For noise that is magnetically coupled from a switching power supply, the noise will be synchronous with the power supply switching frequency. The worst case occurs when the coupled noise is between 10 kHz and 300 kHz, the center of the network data communication band. If the noise is greater than 15 mV peak-to-peak, you should take steps to reduce the coupling effect. The easiest solution is to provide more distance between the power supply and the FT 5000 Smart Transceiver or Neuron 5000 Processor with external transceiver.

For noisy power converters, shielded inductors can provide a solution to magnetic field interference. In the commonly used buck DC-DC converter, a shielded inductor can be used instead of an open-slug inductor to significantly lower the amount of stray magnetic field generated by the DC-DC converter. For example, Taiyo Yuden's LHFP-series inductor can be used instead of their LHL-series, and TDK's FS-series inductor can be used instead of their EL or ELF-series. In transformer-based DC-DC converters, the power supply designer should take care to choose a transformer style that generates minimum external stray magnetic fields. For example, a pot-core DC-DC transformer will generally produce less stray magnetic field than will an E-E core transformer, and the stray fields that it does generate are vertical when they go through the plane of the PCB. A common way to minimize magnetic fields emitted from power supply transformers is to wrap a "shorted-turn" of copper tape around the transformer in the same direction as the transformer winding.

In addition to power supplies, other noise sources can include DC motor controllers and industrial ovens or heaters. For these noise sources, shielding the emitting device is often the most effective approach to solving magnetic field interference problems.

Summary and Testing Results

Table 30 summarizes the results of the immunity and RF testing for a typical LONWORKS application based on an FT 5000 Smart Transceiver with the FT-X3 Communications Transformer. EMC testing results for the Neuron 5000 Processor depend on the specific network transceiver used.

Table 30. Immunity and EMI Results

Test	FT 5000 Smart Transceiver with FT-X3 Communications Transformer
EN 61000-4-2 ESD	15 kV Air 8 kV Contact (Level 4)
EN 61000-4-3 Radiated RF	10 V/m (Level 3)
EN 61000-4-4 Network Burst	2 kV (Level 4)
EN 61000-4-5 Network Surge	2 kV or 6 kV (depends on clamping diodes used; see **Table 23** on page 56) (Level 3)
EN 61000-4-6 Conducted RF	10 V_{RMS} (Level 3)
CISPR 22 Radiated EMI	Class B
CISPR 22 Conducted EMI	Class B

5

Network Cabling and Connections for FT Devices

This chapter describes the network connections and cable types supported for FT devices.

Network Connection

For a TP/FT-10 channel, the network connection (from the NETP and NETN pins) is polarity insensitive. Therefore, either of the two twisted pair wires can be connected to either of these network connections.

For any of the supported cable types, the average temperature of the wire must not exceed +55 °C, although individual segments of wire can be as hot as +85 °C.

As a general rule, TP/FT-10 network channel communication cables should be separated from high voltage power cables. Follow local electrical codes with regard to cable placement.

Network Topology Overview

The TP/FT-10 network is designed to support free topology wiring, and can accommodate bus, star, loop, or any combination of these topologies. Series 5000 devices can be located at any point along the network wiring. This capability simplifies system installation, and makes it easy to add devices if the network needs to be expanded. **Figure 42** through **Figure 46** on page 104 present five different network topologies. The actual termination circuit varies by application.

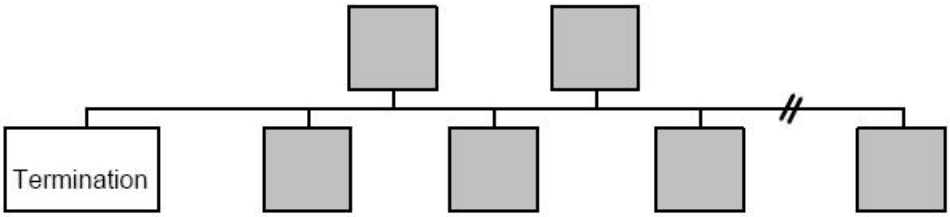


Figure 42. Singly Terminated Bus Topology

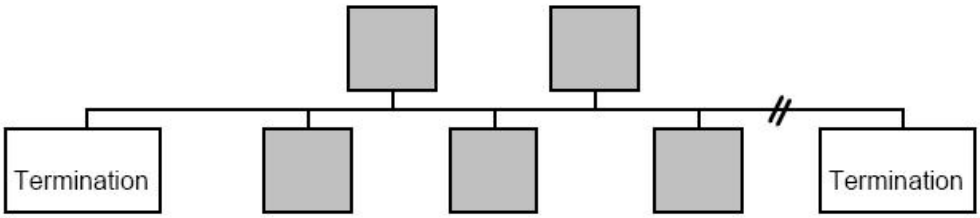


Figure 43. Doubly Terminated Bus Topology

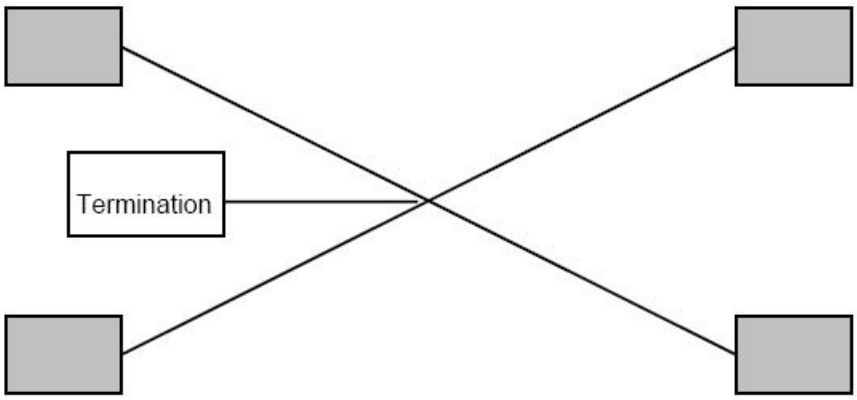


Figure 44. Star Topology

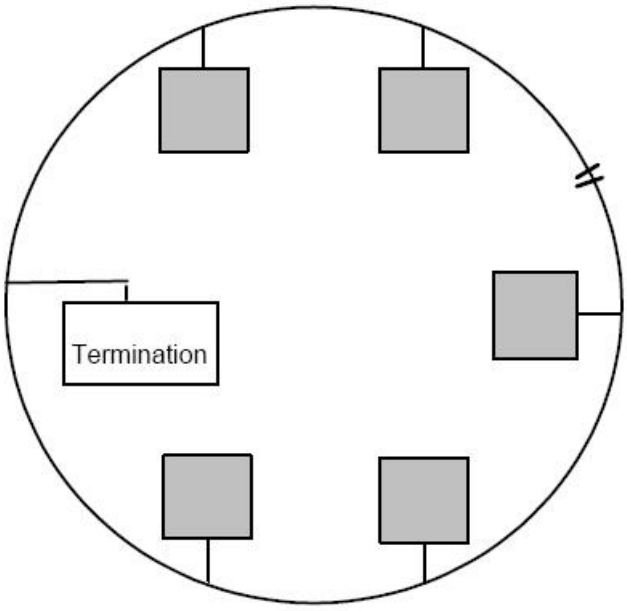


Figure 45. Loop, or Ring, Topology

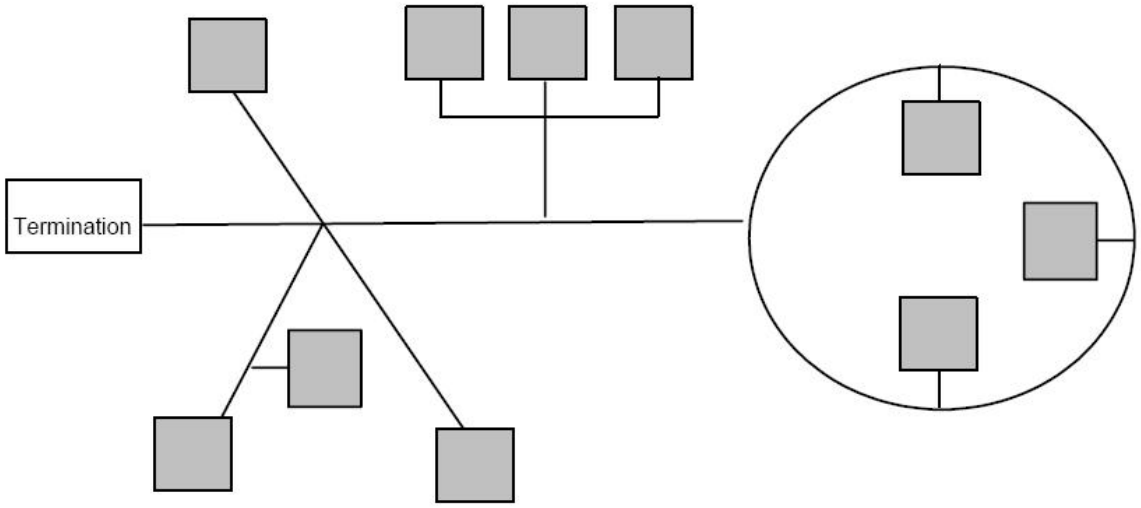


Figure 46. Mixed Topology

In the event that the limits for the number of transceivers or total wire distance are exceeded, then one FTT physical layer repeater (PLR) can be added to interconnect two segments and double the overall system capability. FTT-10A Transceivers are used to make physical layer repeaters. See the *FTT-10A Free Topology Transceiver User's Guide* for more info about PLRs.

System Performance and Cable Selection

Echelon has qualified the following types of cable types for use with TP/FT-10 channels:

- A generic American wire gauge (AWG) 16 (1.3 mm diameter) plenum-rated twisted-pair cable (similar to Belden® 85102 2-conductor wire)
- A generic American wire gauge (AWG) 16 (1.3 mm diameter) standard twisted-pair cable (similar to Belden 8471 1-Pair wire)
- National Electrical Manufacturers Association (NEMA) Type 4 cable (this cable is *not* equivalent to TIA Category 4 cable)
- AWG 24 (0.511 mm) ANSI/TIA/EIA-568-B.2-2001 Category 5 or Category 6 twisted-pair wire
- An EN 50441 telecommunications cable, such as J-Y(ST)Y

Based on the cost, performance, and availability of these different cable types, system designers can choose the most appropriate cable for their application.

Appendix B, *Qualified TP/FT-10 Cable Specifications*, on page 137, lists the electrical specifications for these cables. The *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks* engineering bulletin (005-0023-01) provides a list of cable vendors for each type of supported cable. This bulletin is available from the Echelon Web site (www.echelon.com). These cables have been qualified by Echelon in a generic form, and are available from vendors in a number of variations, including shielded, unshielded, plenum jacketing, and non-plenum jacketing. Additionally, Echelon has qualified two 16 AWG (1.3 mm) Belden cables, and one cable used in specific applications in the European market (type J-Y(ST)Y cable).

TP/FT-10 channels must meet the system specifications and transmission specifications described in the following sections. When you create documentation and installation

procedures for TP/FT-10 channels, be sure to include the TP/FT-10 system specifications and, based upon the cable used, the appropriate transmission distance specifications. Incorporating these specifications can ensure a smoother installation, and provide a resource for the installer who must troubleshoot the installation.

Note: The following specifications apply to a single network segment. You can combine multiple segments by using FTT-10A based physical layer repeaters to increase the number of devices and distance as described in the *FTT-10A Free Topology Transceiver User's Guide*.

System Specifications

Each network segment can include up to 64 FT-X3 (or FT X1 or FT-X2) Transformers and FT Smart Transceivers.

You can use LPT-11 transceivers on network segments with FTT-10A transceivers and FT Smart Transceivers, but they are subject to additional constraints, particularly on distance. See the *LONWORKS LPT-11 Link Power Transceiver User's Guide* for more information.

The average temperature of the wire must not exceed +55°C, although individual segments of wire may be as hot as +85°C.

As a general rule, the TP/FT-10 channel communication cables should be separated from high voltage power cables. Follow local electrical codes with regard to cable placement.

Transmission Distance Specifications

Table 31 and **Table 32** list the transmission distance specifications for the supported cable types.

Table 31. Doubly Terminated Bus Topology Specifications

Cable Type	Maximum Bus Length (Meters)
Belden 85102	2700
Belden 8471	2700
NEMA Type 4, 22 AWG	1400
J-Y(ST)Y 2x2x0.8	900
ANSI/TIA/EIA Category 5 or 6	900

A doubly-terminated bus can have stubs of up to 3 meters from the bus to each device.

Table 32. Free Topology Specifications

Cable Type	Maximum Device-to-Device Distance (Meters)	Maximum Total Wire Length (Meters)
Belden 85102	500	500
Belden 8471	400	500
NEMA Type 4, 22 AWG	400	500

Cable Type	Maximum Device-to-Device Distance (Meters)	Maximum Total Wire Length (Meters)
J-Y(ST)Y 2x2x0.8	320	500
ANSI/TIA/EIA Category 5 / 6	250	450

The free topology transmission distance specification includes two components that must both be met for proper system operation. The distance from each transceiver to all other transceivers and to the termination (including the LPI-10 termination, if used) must not exceed the *maximum device-to-device distance*. If multiple paths exist, for example, in a loop topology, then the longest path should be used for calculations. The *maximum total wire length* is the total length of wire within a segment.

Cable Termination and Shield Grounding

TP/FT-10 network segments require termination for proper data transmission performance. The type of terminator varies depending on whether shielded or unshielded cable is used. Free Topology and bus topology networks also differ in their termination requirements. The following sections describe the various terminators and termination procedures.

Free Topology Network Segment

For a Free Topology segment, only one termination is required; it can be placed anywhere on the Free Topology segment. There are two choices for the termination:

- RC circuit, with Ra = 52.3 Ω ±1%, 1/8 W
- LPI-10 Link Power Interface, with jumper at the "1 CPLR" setting

Figure 47 shows the RC circuit for twisted-pair termination.

Doubly Terminated Bus Topology Segment

For a doubly terminated bus topology, two terminations are required: one at each end of the bus. There are two choices for each termination:

- RC circuit, with Ra = 105 Ω ±1%, 1/8 W
- LPI-10 Link Power Interface, with jumper at the "2 CPLR" setting

Only one LPI-10 interface is supported per segment. The LPI-10 contains the two required terminators. The other terminator must be an RC-type.

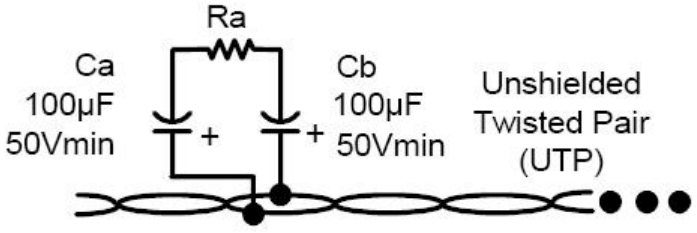


Figure 47. Twisted-Pair Termination

Ca and Cb are typically aluminum-electrolytic type for improved longevity in the presence of ESD. Be sure to observe their polarity.

Grounding Shielded Twisted Pair Cable

When using shielded twisted-pair cable, terminate the twisted pair *and* ground the cable shield, as shown in **Figure 48**.

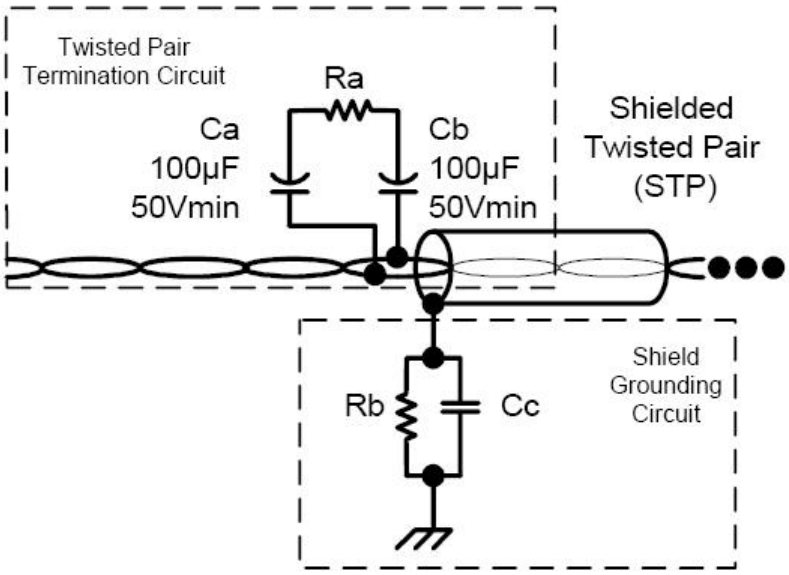


Figure 48. Shielded Twisted-Pair Termination and Grounding

Use the termination described in *Free Topology Network Segment* on page 106 or in *Doubly Terminated Bus Topology Segment* on page 106. The cable shield should be grounded using a capacitor to tie the shield to earth ground, and a large-value resistor to bleed off any static charge on the shield.

Tie the shield to earth ground through a capacitor, instead of using a direct connection, to avoid DC and 50/60 Hz ground paths from being formed through the shield. Typical values for Rb and Cc are:

- Cc = 0.1 µF, 10%, Metalized Polyester, ≥ 100V
- Rb = 470 kΩ, 1/4 W, ±5%

The cable shield should be grounded at least once per segment, and preferably at each device. Grounding the shield at every device assists in suppressing 50/60 Hz standing waves.

6

Input/Output Interfaces for the Series 5000

This chapter provides an overview of the I/O models that are available for Series 5000 devices.

See the *I/O Model Reference for Smart Transceivers and Neuron Chips* for more information about the available I/O models.

Overview

Echelon's Neuron Chips and Smart Transceivers connect to application-specific external hardware through 11 or 12 I/O pins, named IO0-IO11. You can configure these pins to provide flexible input and output (I/O) functions with minimal external circuitry. These functions are described as *I/O models*.

The Neuron C programming language allows the application programmer to declare *I/O objects* that use one or more I/O pins. An I/O object is a software instance of an I/O model, and provides programmable access to an I/O driver for a specified on-chip I/O hardware configuration and a specified input or output waveform definition. Programs can then refer to most of these objects through **io_in()** and **io_out()** system calls to perform the actual input or output function during execution of the program. Because events are associated with changes in input values, the task scheduler can execute associated application code when these changes occur.

There are many different I/O models available for use with the Neuron Chips and Smart Transceivers. Most I/O models are available in system images by default. If an I/O model is required by an application, but is not included in the default system image, the development tool links the appropriate models into available memory space. For FT 3120, PL 3120, and PL 3170 Smart Transceiver designs, this linkage means that internal EEPROM space must be used for the additional model. For FT 3150 or PL 3150 Smart Transceiver designs, the model is added to an external flash or EEPROM region beyond the 16 KB space reserved for the system image. For Series 5000 device designs, the model is added to the application image.

Series 5000 chips also support application-specific interrupts, which can trigger on either or both edges, or on either level, for any of the I/O pins, regardless of any associated I/O object. See the *Neuron C Programmer's Guide* for more information about interrupts.

See the *I/O Model Reference for Smart Transceivers and Neuron Chips* for more information about the available I/O models and how to use them.

Two 16-Bit Timer/Counters

Two classes of I/O model use internal timer/counters. The timer/counters are implemented as a register that is writable by the application processor, a 16-bit counter, and a latch that is readable by the processor. The 16-bit registers are accessed 1 byte at a time. Series 5000 chips have two timer/counters, as shown in **Figure 49** on page 111:

- Timer/Counter 1, with input that is selectable among pins IO4 – IO7 and output to pin IO0
- Timer/Counter 2, with input from pin IO4 and output to pin IO1

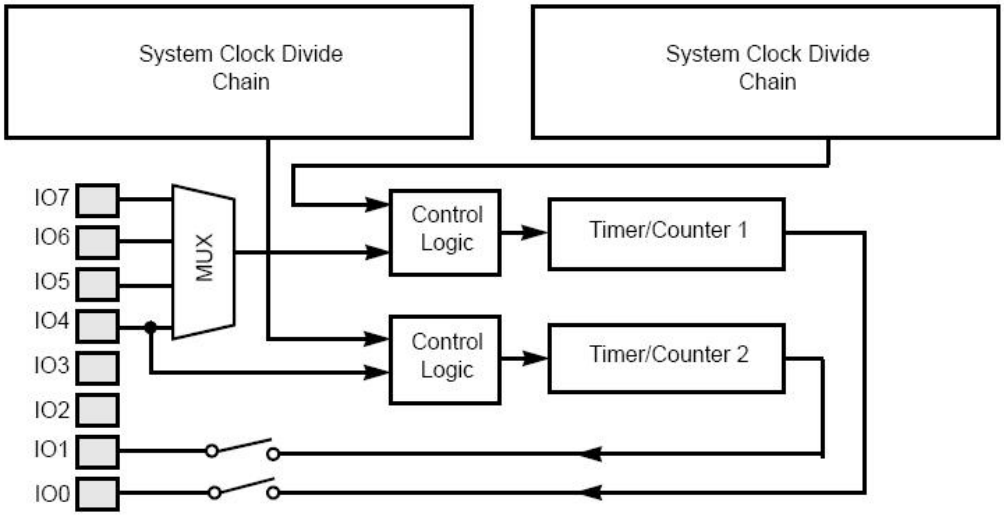


Figure 49. Timer/Counter Circuits

No I/O pins are dedicated to timer/counter functions. If, for example, Timer/Counter 1 is used for input signals only, then IO0 is available for other input or output functions. Clock and enable inputs for the timer/counters can be from external pins, or from scaled clocks derived from the system clock. The clock rates of the two timer/counters are independent of each other. External clock actions occur optionally on the rising edge, the falling edge, or both edges of the input.

Series 5000 chips also support up to one application-specific interrupt task per Timer/Counter unit. These interrupts are triggered by a condition selected through the choice of I/O object that uses the Timer/Counter unit; see the *Neuron C Programmer's Guide* for more information about timer/counter interrupts.

See the *I/O Model Reference for Smart Transceivers and Neuron Chips* for more information about how to use the timer/counters.

Summary of the Available I/O Objects

Many I/O models are available for Neuron Chips and Smart Transceivers. Certain I/O models are available only for specific chip types, but most are available to all Neuron Chips and Smart Transceivers. The I/O models are grouped into the following categories:

- *Direct I/O Models* are based on a logic level at the I/O pins; none of the Neuron Chip or Smart Transceiver hardware's timer/counters are used in conjunction with these I/O models. These models can be used in multiple, overlapping combinations within the same Neuron Chip or Smart Transceiver. Direct I/O models include the following types:

Input Model Types	*Output Model Types*
bit	**bit**
byte	**byte**
leveldetect	**nibble**
nibble	**touch**
touch	

- *Timer/Counter I/O Models* use a timer/counter circuit in the Neuron Chip or Smart Transceiver. Each Neuron Chip and each Smart Transceiver has two timer/counter

circuits: One whose input can be multiplexed, and one with a dedicated input. Timer/counter I/O models include the following types:

Input Model Types	*Output Model Types*
dualslope	**edgedivide**
edgelog	**frequency**
infrared	**infrared_pattern**
ontime	**oneshot**
period	**pulsecount**
pulsecount	**pulsewidth**
quadrature	**stretchedtriac**
totalcount	**triac**
	triggeredcount

- *Serial I/O Models* are used for transferring data serially over a pin or a set of pins. The **neurowire**, **i2c**, **magcard**, **magcard_bitstream**, **magtrack1**, and **serial** I/O models are mutually exclusive within a single Neuron Chip or Smart Transceiver. Both the input and output versions of a serial I/O model can coexist within a single Neuron Chip or Smart Transceiver. Serial I/O models include the following types:

Serial Input Model Types	*Serial Output Model Types*
bitshift	**bitshift**
magcard	**serial**
magcard_bitstream	
magtrack1	
serial	
wiegand	

Serial Input/Output Model Types
i2c
neurowire
sci
spi

- *Parallel I/O Models* are used for high-speed bidirectional I/O. I/O models within this group use all of the Neuron Chip or Smart Transceiver I/O pins. The parallel I/O models include the following types:

Parallel Input/Output Model Types
muxbus
parallel

Table 33 through **Table 37** on page 115 list the available I/O models within each category. **Figure 50** on page 118 summarizes the pin configuration for each of the I/O models. A single device can use various I/O models of different types simultaneously.

Table 33. Summary of the Direct I/O Models

I/O Model	Applicable I/O Pins	Total Pins per Object	Input/Output Value
Bit Input[1]	IO0 – IO11	1	0, 1 binary data
Bit Output[1]	IO0 – IO11	1	0, 1 binary data

I/O Model	Applicable I/O Pins	Total Pins per Object	Input/Output Value
Byte Input	IO0 – IO7	8	0 – 255 binary data
Byte Output	IO0 – IO7	8	0 – 255 binary data
Leveldetect Input	IO0 – IO7	1	Logic 0 level detected
Nibble Input	Any adjacent four in IO0 – IO7	4	0 – 15 binary data
Nibble Output	Any adjacent four in IO0 – IO7	4	0 – 15 binary data
Touch I/O	IO0 – IO7	1	Up to 2048 bits of input or output bits

Notes:

1. The IO11 pin for this I/O model is available only for the following device types: PL 3120-E4, PL 3150, PL 3170, FT 5000, and Neuron 5000.

Table 34. Summary of the Parallel I/O Models

I/O Model	Applicable I/O Pins	Total Pins per Object	Input/Output Value
Muxbus I/O	IO0 – IO10	11	Parallel bidirectional port using multiplexed addressing
Parallel I/O[1]	IO0 – IO11	12	Parallel bidirectional handshaking port

Notes:

1. The IO11 pin for this I/O model is available only for the following device types: FT 5000 and Neuron 5000.

Table 35. Summary of the Serial I/O Models

I/O Model	Applicable I/O Pins	Total Pins per Object	Input/Output Value
Bitshift Input	Any adjacent pair (except IO7 + IO8 & IO10 + IO11)	2	Up to 16 bits of clocked data

I/O Model	Applicable I/O Pins	Total Pins per Object	Input/Output Value
Bitshift Output	Any adjacent pair (except IO7 + IO8 & IO10 + IO11)	2	Up to 16 bits of clocked data
I²C	IO8 + IO9 or IO0 + IO1	2	Up to 255 bytes of bidirectional serial data
Magcard Bitstream	IO8 + IO9 + (one of IO0 – IO7)	2 or 3	Unprocessed serial data stream from a magnetic card reader
Magcard Input	IO8 + IO9 + (one of IO0 – IO7)	2 or 3	Encoded ISO7811 track 2 data stream from a magnetic card reader
Magtrack1	IO8 + IO9 + (one of IO0 – IO7)	2 or 3	Encoded ISO3554 track 1 data stream from a magnetic card reader
Neurowire I/O	IO8 + IO9 + IO10 + (one of IO0 – IO7)	4	Up to 256 bits of bidirectional serial data
SCI (UART)[1]	IO8 + IO10	2	Up to 255 bytes input and 255 bytes output
Serial Input	IO8	1	8-bit characters
Serial Output	IO10	1	8-bit characters
SPI	IO8 + IO9 + IO10 + (IO7)	3 or 4	Up to 255 byes of bidirectional data
Wiegand Input	Any adjacent pair in IO0 – IO7	2	Encoded data stream from Wiegand card reader

Notes:

1. The SCI (UART) model is available only for the following device types: PL 3120-E4, PL 3150, PL 3170, FT 5000, and Neuron 5000.

Table 36. Summary of the Timer/Counter Input Models

I/O Model	Applicable I/O Pins	Total Pins per Object	Input/Output Value
Dualslope Input	IO0, IO1 + (one of IO4 – IO7)	2	Comparator output of the dualslope converter logic

I/O Model	Applicable I/O Pins	Total Pins per Object	Input/Output Value
Edgelog Input	IO4	1	A stream of input transitions
Infrared Input	IO4 – IO7	1	Encoded data stream from an infrared demodulator
Ontime Input	IO4 – IO7	1	Pulse width of 0.2 µs – 1.678 s
Period Input	IO4 – IO7	1	Signal period of 0.2 µs – 1.678 s
Pulsecount Input	IO4 – IO7	1	0 – 65,535 input edges during 0.839 s
Quadrature Input	IO4 + IO5, IO6 + IO7	2	± 16,383 binary Gray code transitions
Totalcount Input	IO4 – IO7	1	0 – 65,535 input edges

Table 37. Summary of the Timer/Counter Output Models

I/O Model	Applicable I/O Pins	Total Pins per Object	Input/Output Value
Edgedivide Output	IO0, IO1 + (one of IO4 – IO7)	2	Output frequency is the input frequency divided by a user-specified number
Frequency Output	IO0, IO1	1	Square wave of 0.3 Hz to 2.5 MHz
Infrared Pattern Output	IO0, IO1	1	Series of timed repeating square wave output signals
Oneshot Output	IO0, IO1	1	Pulse of duration 0.2 µs to 1.678 s
Pulsecount Output	IO0, IO1	1	0 – 65,535 pulses
Pulsewidth Output	IO0, IO1	1	0 – 100% duty cycle pulse train
Stretched Triac Output[1]	IO0, IO1 + (one of IO4 – IO7)	2	Delay of output pulse with respect to input edge
Triac Output[2]	IO0, IO1 + (one of IO4 – IO7)	2	Delay of output pulse with respect to input edge

I/O Model	Applicable I/O Pins	Total Pins per Object	Input/Output Value
Triggered-Count Output	IO0, IO1 + (one of IO4 – IO7)	2	Output pulse controlled by counting input edges

Notes:

1. The Stretched Triac Output model is available only for the following device types: FT 5000 and Neuron 5000.
2. Dual-edge triggering is not available for the following device types: Neuron 3150, FT 3150, or PL 3150.

Neuron Chips and Smart Transceivers have two 16-bit timer/counters on-chip. The input to timer/counter 1, also called the *multiplexed timer/counter,* is selectable among pins IO4 – IO7, through a programmable multiplexer and its output can be connected to pin IO0. The input to timer/counter 2, also called the *dedicated timer/counter,* can be connected to pin IO4 and its output to pin IO1.

The timer/counters are implemented as a 16-bit load register writable by the CPU, a 16-bit counter, and a 16-bit latch readable by the CPU. The load register and latch are accessed a byte at a time. No I/O pins are dedicated to timer/counter functions. If, for example, timer/counter 1 is used for input signals only, then IO0 is available for other input or output functions. Timer/counter clock and enable inputs can be from external pins, or from scaled clocks derived from the system clock; the clock rates of the two timer/counters are independent of each other. External clock actions occur optionally on the rising edge, the falling edge, or both rising and falling edges of the input.

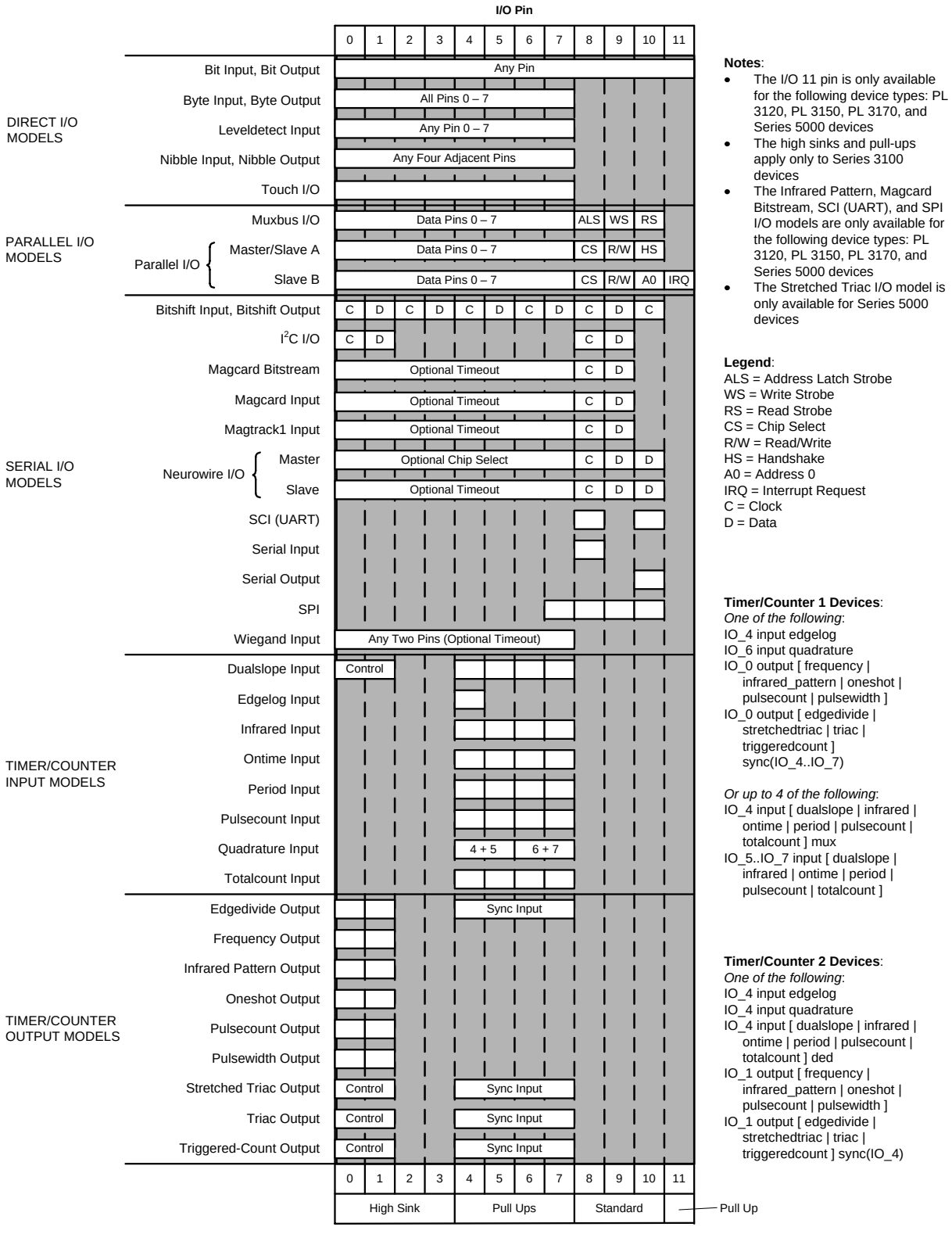
For Series 5000 devices, many of the timer/counter I/O models can also trigger interrupt tasks, which can provide minimum application latency for I/O events that are related to the timer/counter models. See the *Neuron C Programmer's Guide* for more information about defining and using interrupts for Series 5000 devices.

Multiple timer/counter input objects can be declared on different pins within a single application. By calling the **io_select()** function, the application can use the first timer/counter to implement up to four different input objects. If a timer/counter is configured to implement one of the output models, or is configured as a quadrature input object, then it can not be reassigned to another timer/counter object in the same application program.

The following guidelines for declaring I/O object types apply to the I/O models shown in **Figure 50** on page 118:

- Up to 16 I/O objects can be declared.
- Timer/counter 1 can be multiplexed for up to four input objects.
- The **neurowire**, **i2c**, **magcard**, **magcard_bitstream**, **magtrack1**, and **serial** I/O models are mutually exclusive. One or more of a single type of these I/O models can be declared in one program.
- Because the **parallel** and **muxbus** I/O models require all I/O pins for some Neuron Chips and Smart Transceivers, no other object types can be declared when either of these objects is declared. You can declare the IO11 pin as a **bit** input or output in addition to the **parallel** or **muxbus** object for the following device types: PL 3120-E4, PL 3150, or PL 3170. For Series 5000 devices, you can also declare the IO11 pin as a **bit** input or output in addition to the **parallel** (master or slave A mode) or **muxbus** object; the IO11 pin serves as an IRQ pin for the **parallel** (slave B mode) object.

- Direct I/O object types (such as **bit**, **nibble**, **byte**) can be declared in any combination. Timer/counter, **serial**, and **neurowire** I/O object declarations override the pin directions of any overlaying direct I/O object types.
- The **quadrature** and **dualslope** input objects cannot be multiplexed with other input objects on timer/counter 1. The **edgelog** input uses both timer/counters and is exclusive of any other timer/counter objects.
- The **bitshift** I/O objects cannot be declared on the same I/O pins as timer/counter objects. Direct I/O objects can be overlaid with **bitshift** I/O objects. Two adjacent **bitshift** I/O objects cannot share any I/O pins.



Notes:

- The I/O 11 pin is only available for the following device types: PL 3120, PL 3150, PL 3170, and Series 5000 devices
- The high sinks and pull-ups apply only to Series 3100 devices
- The Infrared Pattern, Magcard Bitstream, SCI (UART), and SPI I/O models are only available for the following device types: PL 3120, PL 3150, PL 3170, and Series 5000 devices
- The Stretched Triac I/O model is only available for Series 5000 devices

Legend:
ALS = Address Latch Strobe
WS = Write Strobe
RS = Read Strobe
CS = Chip Select
R/W = Read/Write
HS = Handshake
A0 = Address 0
IRQ = Interrupt Request
C = Clock
D = Data

Timer/Counter 1 Devices:
One of the following:
IO_4 input edgelog
IO_6 input quadrature
IO_0 output [frequency | infrared_pattern | oneshot | pulsecount | pulsewidth]
IO_0 output [edgedivide | stretchedtriac | triac | triggeredcount] sync(IO_4..IO_7)

Or up to 4 of the following:
IO_4 input [dualslope | infrared | ontime | period | pulsecount | totalcount] mux
IO_5..IO_7 input [dualslope | infrared | ontime | period | pulsecount | totalcount]

Timer/Counter 2 Devices:
One of the following:
IO_4 input edgelog
IO_4 input quadrature
IO_4 input [dualslope | infrared | ontime | period | pulsecount | totalcount] ded
IO_1 output [frequency | infrared_pattern | oneshot | pulsecount | pulsewidth]
IO_1 output [edgedivide | stretchedtriac | triac | triggeredcount] sync(IO_4)

Figure 50. Pin Configuration Summary for the I/O Models

Example: The following I/O object types can be combined for a Neuron Chip or Smart Transceiver:

- 1 **parallel** I/O object type (on **IO_0**..**IO10**)

  OR

- 1 **muxbus** I/O object type (on **IO_0**..**IO10**)

  OR

- A combination of any or all of the other I/O models *A* through *E* shown in **Table 38**:

Table 38. Example I/O Model Combinations

A	B	C	D	E
1 to 4 timer/counter inputs (multiplexed on **IO_4**, **IO_5**, **IO_6**, **IO_7**), including **quadrature** input on **IO_6** OR 1 timer/counter output (on **IO_0**)	1 timer/counter input (on **IO_4**), including **quadrature** input on **IO_4** OR 1 timer/counter output (on **IO_1**)	1 **neurowire** I/O object (on **IO_8**, **IO_9**, **IO_10**) and 1 of **IO_0** ... **IO_7** OR 1 serial I/O object type (on **IO_8**, **IO_10**)	Any direct I/O object type on any pin (**IO_0** through **IO_10**)	A bit I/O object on **IO_11**

Hardware Considerations

For a description of the electrical characteristics of the I/O pins, see *Characteristics of the Digital Pins* on page 45 or the appropriate Series 3100 or Series 5000 device data sheet. Pins that are configured as outputs can also be read as inputs, returning the value that was last written to the pin. In addition, an application program can optionally specify the initial values of digital outputs.

For Series 3100 devices, pins IO4 – IO7 and IO11 have optional pull-up current sources that act as pull-up resistors. You use a Neuron C compiler directive (**#pragma enable_io_pullups**) to enable these pull-ups. Also for Series 3100 devices, pins IO0 – IO3 have high current-sink capability (20 mA); the other pins have standard current-sink capability.

For Series 3100 FT Smart Transceivers, the I/O pull-ups are enabled during the stack initialization and built-in self-test (BIST) task (see the *FT 3120 / FT 3150 Smart Transceiver Data Book* for more information about the stack initialization and BIST task). However, for Series 3100 PL Smart Transceivers, the I/O pull-ups are not enabled during the stack initialization and BIST task.

Recommendation: For Series 3100 PL Smart Transceivers (especially for devices with energy storage power supplies), you must ensure that I/O pins that are not used by the application

are tied high or low on the PC board, or are left unconnected and configured as a bit output by the application in order to prevent unnecessary power consumption. See the *PL 3120 / PL 3150 / PL 3170 Power Line Smart Transceiver Data Book* for more information.

For Series 5000 devices, the I/O pins do not have configurable pull-ups or high current-sink capability. If your I/O circuitry requires pull-up resistors, you must add them to the hardware design for the device. The I/O pins on a Series 5000 device have an 8 mA current source and sink capability. If your I/O circuitry has higher current requirements, you can add external driver circuitry (for example, using a Fairchild Semiconductor® 74AC245/74ACT245 Octal Bidirectional Transceiver or 74VHC245/74VHCT245 Octal Buffer/Line Driver).

In addition, the Series 5000 device pins are all 3.3 V pins: the input pins are 5 V tolerant, and the output pins are CMOS compatible. Series 3100 device pins are all 5 V pins.

For both Series 3100 and Series 5000 devices, pins IO0 – IO7 have low-level detect latches.

Because the I/O pins are controlled by system firmware, the timing for reading or writing an I/O pin includes latency that can vary by I/O model and even vary by I/O pin. All inputs are software sampled during processing for the Neuron C **when** statement. In general, the latency scales inversely with the system clock rate.

To maintain and provide consistent behavior for external events, and to prevent setup and hold metastability, all I/O pins, when configured as simple inputs, are passed through a hardware synchronization block, shown in **Figure 51**, that is sampled by the internal system clock.

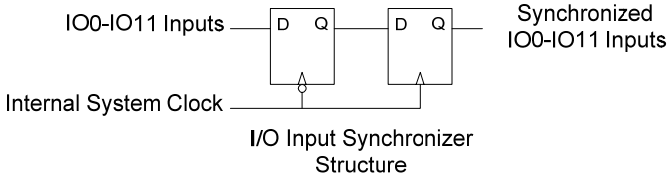


Figure 51. Synchronization Block

I/O pins used for other functions do not have this synchronization requirement.

For Series 3100 devices, the sample rate is always the input clock divided by two (for example, for a 10 MHz input clock, the sample rate is 5 MHz). For a signal to be reliably synchronized with a 10 MHz input clock, it must be at least 220 ns in duration; see **Figure 52**.

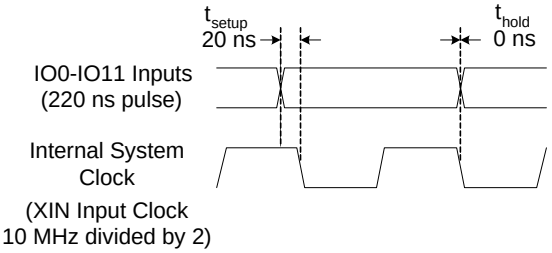


Figure 52. Synchronization of External Signals for Series 3100 Devices

For Series 5000 devices, the sample rate is equivalent to the system clock rate. For a signal to be reliably synchronized with an 80 MHz system clock, it must be at least 17.5 ns in duration; see **Figure 53** on page 121.

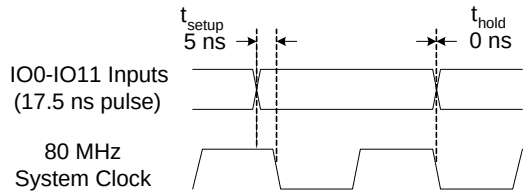


Figure 53. Synchronization of External Signals for Series 5000 Devices

Any event that lasts longer than 220 ns (for a Series 3100 device at 10 MHz) or 17.5 ns (for a Series 5000 device at 80 MHz) is synchronized by hardware, but there can be latency in software sampling, which can result in a delay in detecting the event. If the state changes at a faster rate than software sampling can process, the interim changes are not detected.

The following exceptions apply to the use of the synchronization block:

- The chip select (CS~) input used in the slave B mode of the parallel I/O object recognizes rising edges asynchronously.
- The **leveldetect** input is latched by a flip-flop with a 200 ns clock (for Series 3100 devices) or a 12.5 ns clock (for Series 5000 devices). The level detect transition event is latched, but there is a delay in software detection.
- The SCI (UART) and SPI objects are buffered on byte boundaries by the hardware, and are transferred to memory using an interrupt.
- Events on the I/O pins for the input timer/counter functions are accurately measured, and a value returned to a register, regardless of the state of the application or interrupt processor within the Neuron Chip or Smart Transceiver. However, the application processor can be delayed in reading the register.

7

Programming Considerations

This chapter describes software tools for creating applications that run on Series 5000 devices.

Application Program Development

You can perform initial development and test for Neuron C applications using the Mini FX Evaluation Kit or the NodeBuilder FX Development Tool. You can also perform application debugging using the NodeBuilder Development Tool. See the *Mini FX User's Guide* and the *NodeBuilder FX User's Guide* for detailed instructions on developing, testing, and debugging applications.

For initial device development, you should use the FT 5000 EVB Evaluation Boards that are included with the Mini FX/FT Evaluation Kit or the NodeBuilder FX/FT Development Tool. These boards include sample applications that demonstrate simple Neuron C applications for an FT 5000 Smart Transceiver. See the *FT 5000 EVB Hardware Guide* for more information about the FT 5000 EVB Evaluation Boards.

Mini FX Evaluation Kit

Echelon's Mini FX Evaluation Kit is a tool for evaluating the development of control network applications with the ISO/IEC 14908-1 (ANSI/CEA-709.1 and EN14908) Control Network Protocol. You can use the Mini FX Evaluation Kit to develop a prototype or production control system that requires networking, particularly in the rapidly growing, price-sensitive mass markets of smart light switches, thermostats, and other simple devices and sensors. You can also use the Mini FX Evaluation Kit to evaluate the development of applications for such control networks using the LONWORKS platform.

The Mini FX Evaluation Kit (or later) is required to build applications for Series 5000 devices.

For more information about using the Mini FX Evaluation Kit, see the *Mini FX/FT Quick Start* and the *Mini FX User's Guide*.

NodeBuilder FX Development Tool

The NodeBuilder FX Development Tool is a hardware and software platform that is used to develop applications for Neuron Chips and Echelon Smart Transceivers. The NodeBuilder tool enables you to do the following tasks:

- View standard resource file definitions for SNVTs, SCPTs, and standard functional profiles.
- Create your own resource files with your UNVTs, UCPTs, and user functional profiles.
- Automatically generate Neuron C code that implements your device interface.
- Edit your Neuron C code to implement your device functionality.
- Compile and build your application, and download it to an FT 5000 EVB Evaluation Board or to your own devices.
- Test with prototype I/O hardware on the FT 5000 EVB Evaluation Board, use the FT 5000 EVB to prototype and test your own I/O hardware, or use your own custom device.
- Install your device into a LONWORKS network and test your device interoperating with other LONWORKS devices.
- Use the LNS Plug-in Framework to develop an LNS plug-in for your device.

- Test your LNS plug-in with the LonMaker Integration Tool to ensure that your device is easy to configure and install.

The NodeBuilder FX Development Tool (Service Release 1 or later) is required to build applications for Series 5000 devices.

For more information about using the NodeBuilder FX Development Tool, see the *NodeBuilder FX/FT Quick Start* and the *NodeBuilder FX User's Guide*.

Development Hardware Setup

You configure the NodeBuilder Development Tool to use the TP/FT-10 channel by using an LNS compatible network interface with a TP/FT-10 connection. For initial device development, use the FT 5000 Evaluation Board (BFT5000) device template to target the FT 5000 EVB Evaluation Board for the development environment or as the base template for your Series 5000 device. By default, the hardware template for the FT 5000 EVB platform uses an 80 MHz system clock. You can choose any of the available system clock rates for your device. See the *NodeBuilder FX User's Guide* for more information.

The NodeBuilder Device Template wizard runs during the creation of a new device template. This wizard provides an opportunity to select predefined hardware templates. At a later point in the development process, you can access the hardware template through the Development and Release folders of the project pane.

During initial device development, use the FT 5000 Evaluation Board hardware template. If this template was not selected in the NodeBuilder Device Template Wizard, you can access it by dragging the FT 5000 Evaluation Board icon from the Standard Templates folder located in the Hardware Templates folder to the device template Development folder for the device.

Release Hardware Setup

After you have developed, tested, and debugged the application on the FT 5000 EVB Evaluation Board, you must create a hardware template to match the final target hardware.

The NodeBuilder Development Tool does not include predefined hardware templates for general Series 5000 devices; you can use the FT 5000 Evaluation Board device template as a basis for any custom Neuron 5000 Processor or FT 5000 Smart Transceiver device.

During the initial process of creating a device in the NodeBuilder Development Tool, select this template in the NodeBuilder Device Template wizard. To access the template later, drag the FT 5000 Evaluation Board icon from Standard Templates folder into the Release folder for the device.

After you place the standard template icon in the User Templates folder, the NodeBuilder Hardware Template Properties window opens with the values of the selected standard template. Change the template's name and modify the template properties as follows:

- From the Hardware tab:
    - Specify the type of Series 5000 device (Neuron 5000 Processor or FT 5000 Smart Transceiver) from the **Neuron chip model** dropdown list box.
    - Specify the clock multiplier value from the **Clock multiplier** dropdown list box. This multiplier value specifies the system clock rate for the device.
- From the Memory tab:
    - Specify the starting and ending addresses for the non-volatile memory (external EEPROM and optional flash) in the **Extended non-volatile** fields.

Remember to subtract 2 KB (0x800) from the total memory size to account for the mandatory EEPROM memory.

- Specify the remaining memory for the RAM in the **Extended on-chip RAM** fields.
- **Example**: For a 32K EEPROM part, specify the starting address for the **Extended non-volatile** as 0x4000 and the ending address as 0xB7FF. Specify the starting address for the **Extended on-chip RAM** as 0xB800 (the ending address is always 0xE7FF). Thus, 30 KB of the EEPROM is shadowed to RAM, and the application has 12 KB for general RAM.

After you create the hardware template, drag the new hardware template to the device. Drag the newly created icon in the User Templates folder to the Release folder of the device template to complete the procedure.

You can update the user-defined hardware template at any time by double-clicking the template icon. Your new changes affect any projects opened and compiled using this template. A **Build All** might be required if you change a hardware template without making any other changes.

ShortStack FX Developer's Kit

You can use the ShortStack FX Developer's Kit to develop host-based LONWORKS devices that use the LonTalk Compact API and a ShortStack Micro Server.

A ShortStack Micro Server is a Series 3100 Smart Transceiver, an FT 5000 Smart Transceiver, or a Neuron 5000 Processor, with firmware that implements layers 2 to 5 (and part of layer 6) of the LonTalk protocol. The host processor implements the application layer (layer 7) and part of the presentation layer (layer 6).

The ShortStack firmware allows you to use almost any host processor for your device's application and I/O. The Smart Transceiver or Neuron 5000 Processor implements layers 2 to 5 (and part of layer 6) of the LonTalk protocol and provides the physical interface for the LONWORKS communications channel.

A simple serial communications interface provides communications between the ShortStack Micro Server and the host processor. Because a ShortStack Micro Server can work with any host processor, you must provide the serial driver implementation, although Echelon does provide the serial driver API and an example driver for a specific host processor. Currently, example drivers are available for an Atmel ARM7 microprocessor and an Altera Nios II embedded processor.

For ShortStack device development, you use the C programming language. You use the Echelon LonTalk Interface Developer utility to create the application framework. Your application uses an ANSI C API, the Echelon LonTalk Compact API, to manage communications with the ShortStack Micro Server and devices on the LONWORKS network.

See the *ShortStack FX User's Guide* (078-0365-01B) for more information about the ShortStack Developer's Kit.

A

Series 5000 Design Checklists

This appendix includes a set of checklists, including chip connections, power supplies, PCB layout, and network cabling. These checklists help you ensure that products that you design for the Series 5000 chip meet the specifications described in this manual.

You can copy and freely distribute the contents of this appendix.

Checklist 1: Series 5000 Chip Connections

This checklist applies to all Series 5000 chips, including FT 5000 Smart Transceivers and Neuron 5000 Processors.

Check When Complete	Item	Description
	CC1	The **VDD3V3** pins (8, 18, 29, 30, 41, and 42) are connected to V_{DD3} (+3.3 V), as described in *Pin Connections* on page 41.
	CC2	The **VDD1V8** pins (6, 16, and 44) are connected to the **VOUT1V8** pin (27) only, as described in *Pin Connections* on page 41. Do not connect an external 1.8 V source to any of the **VDD1V8** pins (6, 16, and 44). Connect these pins to the **VOUT1V8** pin (27) only. **Using an external 1.8 V source for the VDD1V8 pins voids the warranty for the chip, and can cause unpredictable and possibly irreparable results.**
	CC3	The **AVDD3V3** pin (31) are connected to analog V_{DD3} (if separate from digital V_{DD3}) or to +3.3 V, as described in *Pin Connections* on page 41.
	CC4	The chip's pad (pin 49) is connected to logic ground, as described in *Pin Connections* on page 41.
	CC5	The **AGND** pin (33) is connected to analog ground (if separate from logic ground) or to logic ground, as described in *Pin Connections* on page 41.
	CC6	Decoupling capacitors are placed between V_{DD3} and ground (0.1 µF 10% 16V X7R) for pins 6, 8, 16, 18, 27, 29, 30, 31, 41, and 44. Each capacitor is placed directly adjacent to a V_{DD3} pin, on the top layer of the PCB, with a short connection to ground, as described in *Pin Connections* on page 41.
	CC7	An additional decoupling capacitor is placed between V_{DD3} and ground (0.1 µF 10% 6.3V X7R) for the **VOUT1V8** pin (27). The capacitor is placed directly adjacent to the **VOUT1V8** pin, on the top layer of the PCB, with a short connection to ground, as described in *Pin Connections* on page 41.
	CC8	Unused I/O pins are pulled up to V_{DD3}, or pulled down to ground, with a 10 kΩ resistor.
	CC9	The crystal or oscillator is connected to the **XIN** and **XOUT** pins (23 and 24), is 10 MHz, is 18 pF parallel resonant, and meets the accuracy requirements described in *Clock Requirements* on page 63.

Check When Complete	Item	Description
	CC10	Capacitors (30 pF 5% 50V NPO) are placed at the **XIN** and **XOUT** pins (23 and 24), as described in *Clock Requirements* on page 63. Each capacitor is placed directly adjacent to the **XIN** and **XOUT** pins, on the top layer of the PCB, with a short connection to ground.
	CC11	A feedback resistor (1 MΩ) is added across the **XIN** and **XOUT** pins (23 and 24), as described in *Clock Requirements* on page 63.
	CC12	A series resistor (200 Ω) is added at the **XOUT** pin (24), as described in *Clock Requirements* on page 63.
	CC13	Other than the crystal, the capacitors, series resistor, and the feedback resistor, there are no other connections to the **XIN** pin. The **XOUT** pin can optionally drive a CMOS buffer, as described in *Clock Requirements* on page 63.
	CC14	The **VDDPLL** pin (25) is connected to the **VOUT1V8** pin (27) with an associated chip ferrite bead, as described in *Pin Connections* on page 41.
	CC15	The **GNDPLL** pin (26) is connected to GND with an associated chip ferrite bead, as described in *Pin Connections* on page 41.
	CC16	Stabilizing capacitors (0.01 µF 10% 50V X7R and 0.1 µF 10% 16V X7R) are added across the PLL pins (pins 25 and 26), as described in *Pin Connections* on page 41. Each capacitor is placed directly adjacent to the PLL pins, on the top layer of the PCB.
	CC17	The connections for the external memory parts meet the requirements specified in *External Serial Memory Interface* on page 24.
	CC18	The JTAG **TCK** pin (19) includes a pullup resistor (4.99 kΩ) to V_{DD3}, as described in *Pin Connections* on page 41.

Checklist 2: FT 5000 Smart Transceiver Connections

This checklist applies to FT 5000 Smart Transceivers.

Check When Complete	Item	Description
	FC1	All items in *Checklist 1: Series 5000 Chip Connections* on page 128 are complete.
	FC2	Environmental and electrical specifications are met, as described in the *FT 5000 Free Topology Smart Transceiver* data sheet.
	FC3	The FT-X3 Communications Transformer pins are connected as specified in *Transformer Electrical Connections* on page 145.
	FC4	The FT 5000 Smart Transceiver and the FT-X3 Communications Transformer are placed adjacent to one another on the same PCB.
	FC5	The connections for the **NETP** and **NETN** pins (34 and 32) match the requirements specified in *Connection for an FT 5000 Smart Transceiver* on page 56.
	FC6	The **CP4** pin (39) is connected to V_{DD3} through a 4.99 kΩ pullup resistor, as shown in *Connection for an FT 5000 Smart Transceiver* on page 56.

Checklist 3: Neuron 5000 Processor Connections

This checklist applies to Neuron 5000 Processors.

Check When Complete	Item	Description
	NC1	All items in *Checklist 1: Series 5000 Chip Connections* on page 128 are complete.
	NC2	Environmental and electrical specifications are met, as described in the *Neuron 5000 Processor* data sheet.
	NC3	The connections for the **CP0..CP4** pins (32, 34, 37, 38, and 39) match the requirements specified in *Connection for a Neuron 5000 Processor* on page 59.

Checklist 4: Power Supply

This checklist applies to all Series 5000 chips, including FT 5000 Smart Transceivers and Neuron 5000 Processors.

Check When Complete	Item	Description
	PS1	V_{DD3} = 3.3V ± 0.3V over the full device temperature range and device application current range (including any ripple).
	PS2	Any ripple on V_{DD3} is ≤ 50 mV_{p-p}, measured with a 20 MHz bandwidth.
	PS3	For host-based devices (ShortStack devices), the rise time of V_{DD3} at power-up meets the requirements of the host microprocessor (see the appropriate host microprocessor data sheet – the maximum allowable risetime is often listed).

Checklist 5: Device PCB Layout

This checklist applies to all Series 5000 chips, including FT 5000 Smart Transceivers and Neuron 5000 Processors.

Check When Complete	Item	Description
	LO1	Your design incorporates a "star ground" layout design, with the network connector, coupling circuit, power supply input, and externally-accessible I/Os all grouped near each other along one edge (or two adjacent edges) of the PCB.
	LO2	If your device has a metal enclosure, the enclosure is tied to the center of the star ground through a low inductance connection (optionally with a low-inductance DC blocking capacitor in series).
	LO3	For 4-layer PCBs, the internal ground plane is used to connect the center of the star ground out to the ground connections of the other functional blocks. For 2-layer PCBs, ground pours on the bottom and top layers are used to connect the center of the star ground out to the ground connections of the other functional blocks.
	LO5	For FT 5000 Smart Transceiver devices, the EMC keepout area shown in **Figure 34** on page 80 has no traces or planes in the area shown, except for the connections from the NETA and NETB traces through the coupling capacitors and into the communication transformer.
	LO6	There is a low-inductance ground path from the Series 5000 chip back to the center of the star ground, to ensure that ESD and surge transients clamped inside the Series 5000 chip have a good return path back off of the PCB without going through any sensitive circuitry.
	LO7	If the device has a host microprocessor or any other digital circuitry that could generate RF noise, that circuitry is kept away from the network cable, power cable, and any I/O cables.
	LO8	The leakage capacitance to external metal surfaces from high frequency circuit traces is controlled with guard traces.
	LO9	The FT-X3 Communications Transformer PCB layout matches **Figure 57** on page 146.

Checklist 6: Network Cabling and Termination

This checklist applies to FT 5000 Smart Transceivers.

Check When Complete	Item	Description
	NT1	The LONWORKS network uses one of the approved wire types described in Chapter 5, *Network Cabling and Connections for FT Devices*, on page 101.
	NT2	The LONWORKS network uses the appropriate termination, as described in *Cable Termination and Shield Grounding* on page 106.

Checklist 7: Device Programming

This checklist applies to all Series 5000 chips, including FT 5000 Smart Transceivers and Neuron 5000 Processors.

Check When Complete	Item	Description
	PG1	For FT 5000 Smart Transceivers, TP/FT-10 is used as the channel definition in the development tool. For Neuron 5000 Processors, the appropriate channel type is specified.
	PG2	The device's hardware template defines the appropriate clock multiplier for the Series 5000 chip's PLL to specify the system clock rate.

B

Qualified TP/FT-10 Cable Specifications

This appendix describes generic cable specifications for cables that Echelon has qualified to work with TP/FT-10 channels.

Introduction

This appendix documents generic cable specifications for cables that Echelon has qualified to work with TP/FT-10 channels. Specific vendors and their cables are cited only to highlight the variety of cable types available that meet these generic specifications; other vendors may also meet the required specifications.

Qualified Cables

Echelon has qualified five cable types that are available from a variety of different vendors. **Table 39** describes these cables.

Table 39. Qualified Cables

Cable Type	AWG	Diameter	Comment
TIA 568A Category 5 or Category 6 cable	24 AWG	0.5 mm	Widely available, and can be found as part of structured cabling systems, such as the CommScope® Inc. Systimax® Structured Connectivity Solutions (originally developed by AT&T® Bell Laboratories).
NEMA Type 4 cable	16 AWG	1.3 mm	Available with a broad range of options, including stranded or solid, 1 or 2 pairs per cable, shielded or unshielded, and plenum or PVC. See also *NEMA Type 4 Cable Specifications* on page 139.
Belden 8471 cable	16 AWG	1.3 mm	See *16 AWG (1.3 mm) "Generic" Cable Specifications* on page 141.
Belden 85102 cable	22 AWG	0.65 mm	See *16 AWG (1.3 mm) "Generic" Cable Specifications* on page 141.
J-Y(ST)Y 2x2x0.8 cable	20.4 AWG	0.8 mm	Available only in Europe. See the *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks* engineering bulletin (005-0023-01) for more information.

Notes:

- AWG: American wire gauge. See *ASTM B258 - 02(2008) Standard Specification for Standard Nominal Diameters and Cross-Sectional Areas of AWG Sizes of Solid Round Wires Used as Electrical Conductors* (www.astm.org/Standards/B258.htm) for a definition of the wire gauges.
- NEMA: National Electrical Manufacturers Association. www.nema.org
- TIA: Telecommunications Industry Association. www.tiaonline.org

The *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks* engineering bulletin (005-0023-01) provides a list of cable vendors for each cable type. This document is available from the Echelon website (www.echelon.com).

Category 5 and 6 Cable Specifications

The specification for the Telecommunications Industry Association *Commercial Building Telecommunications Cabling Standard* (ANSI/TIA/EIA-568-A-95) is available from Information Handling Services (IHS) at global.ihs.com.

NEMA Type 4 Cable Specifications

The Type 4 cable specification used by Echelon, and as originally defined by the National Electrical Manufacturers Association (NEMA), differs from the Category IV specification proposed by the Electronic Industries Association/Telecommunication Industry Association (EIA/TIA).

Table 40 through **Table 43** on page 141 list the Type 4 cable specifications. In the tables, specifications apply to shielded or unshielded 22 AWG (0.65 mm) cable, unless listed otherwise.

Table 40. General Specifications

Specification	Value
DC Resistance (ohms per 1000 feet at 20 °C) maximum for a single copper conductor regardless of whether it is solid or stranded and is or is not metal-coated	18 [for 22 AWG (0.65 mm) cable] 28.6 [for 24 AWG (0.5 mm) cable]
DC Resistance Unbalance (percent) maximum	5
Mutual Capacitance of a Pair (pF/foot) maximum	17
Pair-to-Ground Capacitance Unbalance (pF/1000 feet) maximum	1000

Table 41. Impedance Characteristics

Frequency	Impedance (Ohms)
772 kHz	102 ±15% (87-117)
1.0 MHz	100 ±15% (85-115)
4.0 MHz	100 ±15% (85-115)
8.0 MHz	100 ±15% (85-115)
10.0 MHz	100 ±15% (85-115)
16.0 MHz	100 ±15% (85-115)
20.0 MHz	100 ±15% (85-115)

Table 42. Attenuation (dB per 1000 feet at 20 °C) Maximums

Frequency	Attenuation (dB per 1000 feet at 20 °C)
772 kHz	4.5 [for 22 AWG (0.65 mm) cable] 5.7 [for 24 AWG (0.5 mm) cable]
1.0 MHz	5.5 [for 22 AWG (0.65 mm) cable] 6.5 [for 24 AWG (0.5 mm) cable]
4.0 MHz	11.0 [for 22 AWG (0.65 mm) cable] 13.0 [for 24 AWG (0.5 mm) cable]
8.0 MHz	15.0 [for 22 AWG (0.65 mm) cable] 19.0 [for 24 AWG (0.5 mm) cable]
10.0 MHz	17.0 [for 22 AWG (0.65 mm) cable] 22.0 [for 24 AWG (0.5 mm) cable]
16.0 MHz	22.0 [for 22 AWG (0.65 mm) cable] 27.0 [for 24 AWG (0.5 mm) cable]
20.0 MHz	24.0 [for 22 AWG (0.65 mm) cable] 31.0 [for 24 AWG (0.5 mm) cable]

Table 43. Worst-Pair Near-End Crosstalk (dB) Minimums

Specification	Value (dB)
772 kHz	58
1.0 MHz	56
4.0 MHz	47
8.0 MHz	42
10.0 MHz	41
16.0 MHz	38
20.0 MHz	36

Values in **Table 43** are shown for informational use only. The minimum near-end cross talk (NEXT) coupling loss for any pair combination at room temperature is to be greater than the value determined using the following formula for all frequencies in the range of 0.772 MHz to 20 MHz for a length of 1000 feet (305 m):

$$NEXT(F_{MHz}) > NEXT(0.772) - 15 * \log\left(\frac{F_{MHz}}{0.772}\right)$$

16 AWG (1.3 mm) "Generic" Cable Specifications

Table 44 and **Table 45** on page 142 describe the specifications for the 16 AWG (1.3 mm) generic cable qualified by Echelon for use with TP/FT-10 networks. The generic single twisted pair is stranded (19 x 29) with tinned copper.

The conditions listed in the tables are specified according to *ASTM D4566 - 05e1 Standard Test Methods for Electrical Performance Properties of Insulations and Jackets for Telecommunications Wire and Cable* (www.astm.org/Standards/D4566.htm).

Table 44. General Specifications

Specification	Minimum	Typical	Maximum	Condition
DC resistance, each conductor	14.0	14.7	15.5 Ω/km	20 °C
DC resistance, unbalance	—	—	5%	20 °C
Mutual capacitance	—	—	55.9 nF/km	—
Characteristic impedance	92	100	108	64 kHz to 1 MHz

Table 45. Attenuation and Propagation Delay Characteristics

Characteristic	Maximum	Condition
Attenuation 20 kHz 64 kHz 78 kHz 156 kHz 256 kHz 512 kHz 772 kHz 1000 kHz	 1.3 dB/km 1.9 dB/km 2.2 dB/km 3.0 dB/km 4.8 dB/km 8.1 dB/km 11.3 dB/km 13.7 dB/km	20 ºC
Propagation delay	5.6 ns/m	78 kHz

C

FT-X3 Communications Transformer

This appendix describes the FT-X3 Communications Transformer, including its pinout, electrical connections, and pad layout.

Transformer Pinout

Figure 54 shows the pinout for the FT-X3 Communications Transformer and the equivalent electrical schematic. The FT-X3 Communications Transformer is rotationally symmetric; thus, the package does not mark pin 1. The wiring connections shown in **Figure 54** are made on the PCB, as described in *Transformer Pad Layout* on page 146. **Table 46** lists the pin assignments for the FT-X3 Communications Transformer.

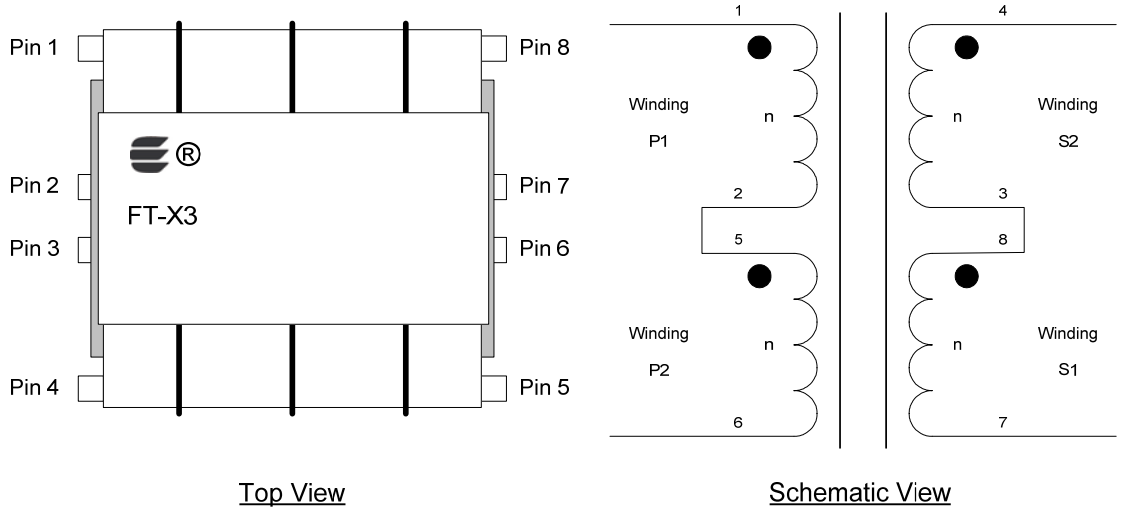


Figure 54. FT-X3 Communications Transformer Pinout Diagram and Schematic

Table 46. FT-X3 Communications Transformer Pin Assignments

Name	Pin Number	Description
NETP	1	NETP connection from FT 5000 Smart Transceiver
CTP1	2	Center tap for primary winding 1
CTS2	3	Center tap for secondary winding 2
NETA	4	NETA connection to LONWORKS network
CTP2	5	Center tap for primary winding 2
NETN	6	NETN connection from FT 5000 Smart Transceiver
NETB	7	NETB connection to LONWORKS network
CTS1	8	Center tap for secondary winding 1

Transformer Electrical Connections

Figure 55 shows the electrical connections for the FT-X3 Communications Transformer. The NETP and NETN signals represent connections to the FT 5000 Smart Transceiver NETP and NETN pins (32 and 34). The NETB and NETA ports represent the connections to the LONWORKS network, as shown in **Figure 56** on page 146.

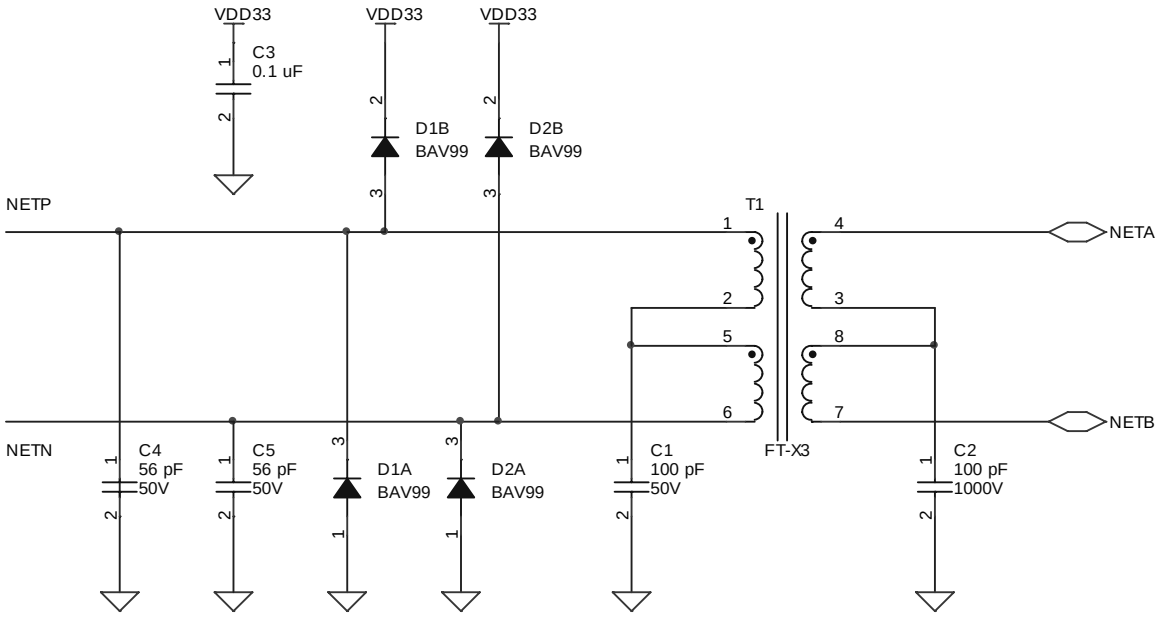


Figure 55. FT-X3 Electrical Connections

In the figure, the diodes D1 and D2 are ESD transient clamping diodes. Capacitors C1 and C2 are optional center-tap capacitors for the primary and secondary sides of the transformer. You can tune the values for C1 and C2 based on required EMC performance. Capacitor C3 provides decoupling for the ESD clamp diodes. Capacitors C4 and C5 provide common-mode noise immunity for compliance with EN61000-4-6 Level 3.

Note that the electrical connections for the FT-X3 Communications Transformer shown in **Figure 55** differ from the connections shown in the schematic for the FT 5000 Evaluation Board that is included with the NodeBuilder FX Development Tool and the Mini FX Evaluation Kit. The connections described in this data book (and also in the data sheet for the FT 5000 Smart Transceiver and FT-X3 Communications Transformer, 003-0457-01B) are the *preferred* connections for the FT-X3 Communications Transformer. Other electrical connections, such as those used for the FT 5000 EVB, are possible, but are not recommended for general use.

Figure 56 on page 146 shows the electrical connections for the FT network connector to the LONWORKS network.

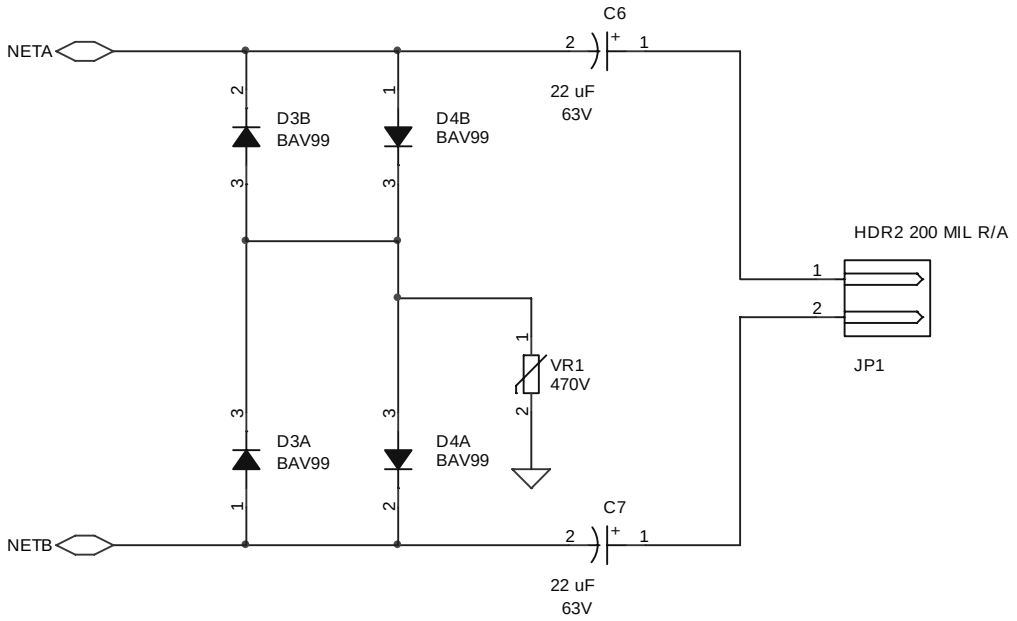


Figure 56. FT Network Electrical Connections

In the figure, the diodes D3 and D4 are differential network clamping diodes. Capacitors C6 and C7 are DC blocking capacitors, 22 µF, 63 V, polarized electrolytic aluminum. Varistor VR1 is 470 V, 5 mm. See *Connection for an FT 5000 Smart Transceiver* on page 56 for more information about the network connection.

Transformer Pad Layout

See the FT 5000 Free Topology Smart Transceiver data sheet (003-0457-01C) for a description of the pad layout for the FT-X3 Communications Transformer.

Figure 57 shows the recommended PCB trace layout for the FT-X3 Communications Transformer for a two-layer PCB.

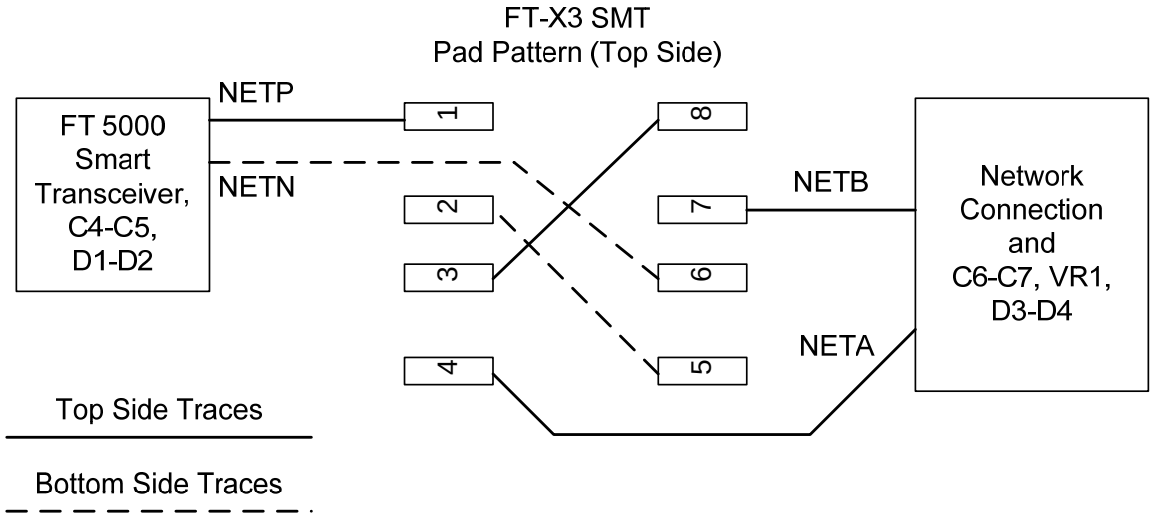


Figure 57. Recommended PCB Layout for FT-X3 Transformer

Notes for the figure:

- Maintain a minimum distance of 2 mm between a routed trace and any of the transformer pads or traces. This distance is especially important for the network pins (3, 4, 7, and 8) to maintain EMC compliance. The primary and secondary traces should be kept away from each other as much as possible.
- If you use center-tap capacitors, place them near pin 2 (Primary) and pin 8 (Secondary).
- Vias and other PCB features are not shown. Use standard practices for vias and trace widths.
- The component callout letters refer to the callouts used in **Figure 55** and **Figure 56**.

Recommendation: Add vias to the ends of each of the pin pad connections (just outside the SMT pad rectangles) to provide additional mechanical support for the transformer, as shown in **Figure 58**. The figure shows the pad trace extended to the via at each end, and slightly narrowed to distinguish the trace from the pad; use standard layout rules to determine the size and distances for the traces.

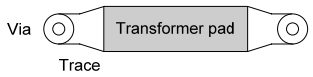


Figure 58. Adding Vias to the Transformer Pad Layout

D

Handling and Manufacturing Guidelines

This appendix describes guidelines for handling and manufacturing devices that use the Neuron 5000 Processor or FT 5000 Smart Transceiver, including soldering profiles and ESD handling guidelines.

Application Considerations

This section describes application considerations for design and manufacturing of LONWORKS devices.

Termination of Unused Pins

Because Series 5000 devices are CMOS devices, you must terminate all unused input pins, including undeclared or unconnected I/O pins that are configured as inputs and including three-state pins, to assure proper operation and reliability.

Figure 59 shows a CMOS inverter representative of circuitry found on CMOS input pins. When the input is logic zero, the P-channel transistor is *on* (conducts), and the N-channel transistor is *off*. When the input is a logic one, the P-channel transistor is *off*, and the N-channel transistor is *on*. These transistors are linear devices with relatively broad switch points. As the input transitions through the mid-supply region, there is a period of time when both transistors are conducting. With fast rise-time digital signals at the input, this period is very short. When the inverter is out of the linear region, there is very little current flow. This effect is the reason that the overall current drain of a CMOS device is directly proportional to the switching speed. Almost all the current consumption is by transistors passing through the linear region and charging and discharging of internal capacitances. If a pin is configured as an input or three-state, then the input can oscillate because of power supply noise or it can float to the mid-supply region, which can result in higher current consumption. Current design techniques have made latch-up due to floating input unlikely, but it is good design practice to terminate unused I/O pins that are not configured (high impedance) or are configured as inputs.

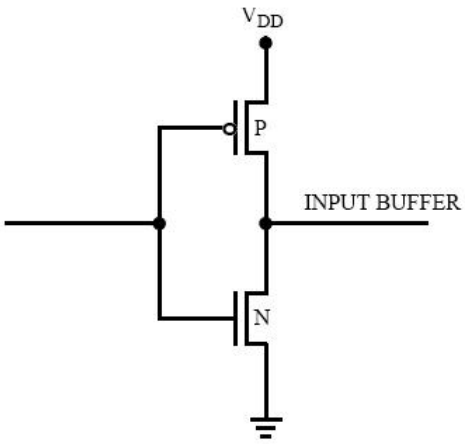


Figure 59. CMOS Inverter

The best method to terminate unused I/O pins is with an individual pull-up or pull-down resistor for each unused pin. Other, less desirable, methods include:

- Connecting unused input pins to each other and then to a common termination point. This cost- and space-effective method has the disadvantage of not allowing individual pin configuration later and has the possibility of contention if the pins are later declared as outputs.

- Connecting individual unused I/O pins directly to GND or to V_{DD}. This method is not recommended in case of software error and because of the possibility of output declaration to an opposing state.
- Declaring unused pins as outputs.

Thus, you should never connect a pin that is capable of being configured as an output to another such pin or directly to GND or to V_{DD}.

Avoidance of Damaging Conditions

All integrated circuit devices can be damaged or destroyed by exceeding specified voltage and environmental limits. These limits are conservative to ensure reliable operation within the conditions specified.

The maximum peak temperature for a Series 5000 chip is 260 ºC. See *Recommended Solder Profile* on page 154, and consult the data sheet of the solder manufacturer for recommendations on the optimum reflow profile. The actual reflow profile that you choose should consider these peak temperature limitations.

Most potentially destructive AC waveforms fall into one of two categories:

- High-voltage (10 kV to 25 kV), low-energy, spikes due to ESD discharge that usually last no longer than 100 ns. ESD modeling has shown that the human body can generate and discharge electrostatic voltages of up to 12 kV.
- Lower-voltage, higher energy, transients that can last for several hundred microseconds or more, that can be caused by capacitive coupling of lightning or by inductive load sources.

Different protection devices for these destructive waveforms must be implemented, depending on what is anticipated in the operating environment. Failure modes can be quantified and protective precautions taken to avoid product malfunction. This could be PC board layout-related or could involve the use of external protection devices. External protection is required for products that are subject to human contact or where interfaces to other equipment might be encountered. See Chapter 4, *Design and Test for Electromagnetic Compatibility*, on page 87, for more information about ESD protection.

Many factors, including ambient temperature and semiconductor lot-to-lot processing variations, can influence the effect of illegal conditions on a Series 5000 chip. The ground pins are internally connected to the substrate of the silicon die and are the reference point for all voltages. The Series 5000 chip functions for V_{DD} are connected to the positive supply pins. In limited temperature range environments, the device might operate over a wider V_{DD} ranges, with timing, drive, FT transceiver, and other specifications not met. There might also be some adverse effects on gate oxides from long-term exposures to V_{DD} greater than 3.3 V.

For Series 5000 chips, do not connect an external 1.8 V source to any of the **VDD1V8** pins (6, 16, and 44). Connect these pins to the **VOUT1V8** pin (27) only. **Using an external 1.8 V source voids the warranty for the chip, and can cause unpredictable and possibly irreparable results.**

Two additional damage mechanisms that are resident in CMOS chips include *zap* and *latch-up*:

- Zap refers to damage caused by exposure to very-high-voltage static electricity. This damage usually appears as breakdown of the relatively thin oxide layers, which

causes leakage or shorts. Often secondary damage occurs after an initial zap failure causes a short.

- Latch-up refers to a usually catastrophic condition that is caused by turning on a parasitic, bipolar, silicon-controlled rectifier (SCR). A latch-up is formed by N and P regions in the layout of the integrated circuit, which act as the collector, base, and emitter of parasitic transistors. Bulk resistance of silicon in the wells and substrate acts as resistors in the SCR circuit. Application of voltages to pins above V_{DD} + 0.3 V or below GND – 0.3 V, in conjunction with enough current to develop voltage drops across the parasitic resistors, can cause the SCR to turn on. After it is on, the SCR can be turned off only by removal of all power and applied voltages. The low on-impedance of the SCR circuit can overheat and destroy the chip.

Figure 60 shows the MOS circuitry for a digital input-only pin. The gates of the input buffer are very high impedance for all voltages that would ever be applied to the pin. Protection is implemented with a P-channel transistor that acts as a diode to V_{DD} and an N-channel transistor that acts as a diode to GND. Allowing a pin to float or be driven to a mid-supply level can result in both the N- and P-channel devices in the input buffer simultaneously being partially on, which can cause excess current and noise for the V_{DD}/GND power supply. If a digital input is driven above V_{DD}, the pseudo-diode will conduct, protecting the input. As the current is increased to high levels (100 mA), damage can result.

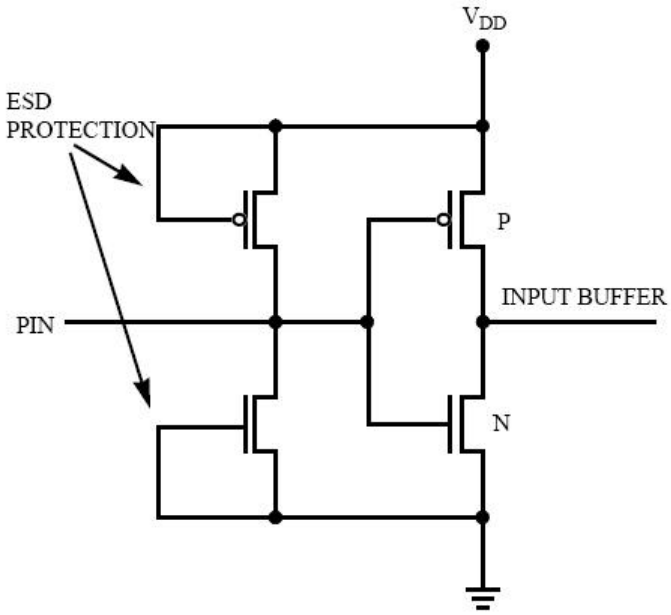


Figure 60. Digital Input

Figure 61 on page 153 shows the CMOS circuitry for a digital I/O pin.

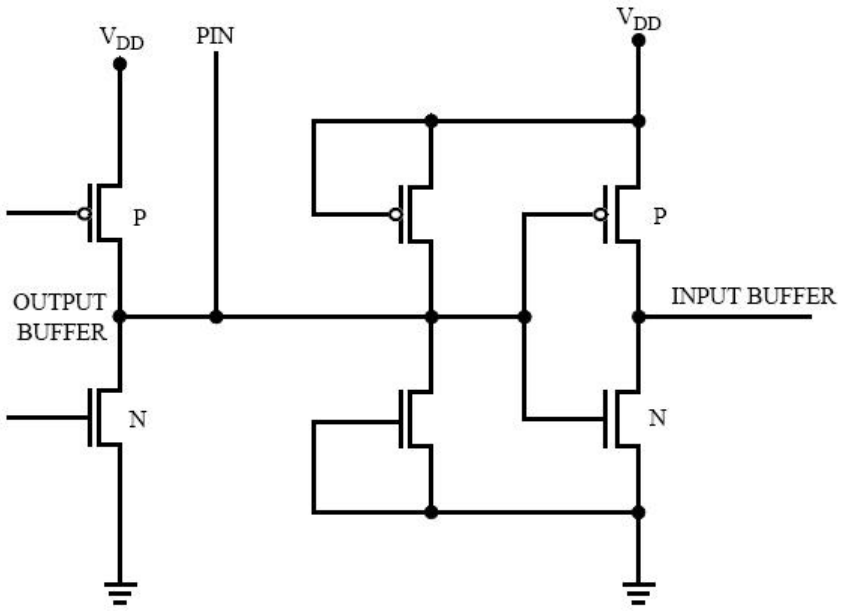


Figure 61. Digital I/O

Electrostatic Discharge Design Guidelines

There are many ways to deal with ESD, including:

- Divert or limit energy from points of contact to circuitry.
- Start with a series of electromagnetic interference (EMI) ferrites or resistors for high frequency filtering.
- Use diodes, transient voltage suppressors (such as, MOSorbs or transorbs) for high-speed clamping.
- Use capacitors to protect critical inputs.
- Use good power distribution.
- Use a separate, low-impedance, ESD ground path to divert energy from electronics (for example, the star-ground strategy described in Chapter 4, *Design and Test for Electromagnetic Compatibility*, on page 87).

Note: The impedance of a wire at 300 MHz is approximately 20 Ω/cm. Use a conductor with less than or equal to 3:1 length:width ratio.

Power Supply, Ground, and Noise Considerations

Some of the most important considerations for PCB layout concern how to manage noise. Noise can come from the power supply, from digital circuitry on the device, and from digital signals that couple to analog signals. Best practices for PCB layout methods to help prevent noise-induced problems include:

- Keep digital signals as far away from analog signals as possible.

- Use short, low-inductance, traces for the analog circuitry to reduce inductive, capacitive, and radio frequency (RF) noise sensitivities.
- Use short, low-inductance, traces for the digital circuitry to reduce inductive, capacitive, and radio frequency (RF) radiated noise.
- Connect bypass capacitors between the V_{DD} and GND pairs with minimal trace length. These capacitors help supply the instantaneous currents of the digital circuitry, in addition to decoupling the noise that can be generated by other sections of the device or by other circuitry on the power supply.
- Use short, wide, low-inductance, traces to connect all of the GND ground pins together. Depending on the application, a double-sided PCB with a ground plane under the device that connects all of the digital and analog GND pins together could be a good grounding method. A multilayer PCB with a ground plane that connects all of the digital and analog GND pins together would be the optimal ground configuration. These methods result in the lowest resistance and the lowest inductance in the ground circuit, which is important to reduce voltage spikes in the ground circuit resulting from the high-speed digital current spikes. Suppressing these voltage spikes on the integrated circuit is the reason for multiple GND leads.
- Use short, wide, low-inductance, traces to connect all of the V_{DD} power supply pins together. Depending on the application, a double-sided PCB with V_{DD} bypass capacitors to the ground plane under the device can complete the low-impedance coupling for the power supply. For a multilayer PCB with a power plane, connecting all of the digital and analog V_{DD} pins to the power plane would be the optimal power distribution method. The integrated circuit layout and packaging considerations for the 3.3 V_{DD} power circuit are essentially the same as for the ground circuit.

Decoupling Capacitors

To absorb switching spikes, which can introduce noise problems, the following CMOS devices should be bypassed with good quality 0.022 µF to 0.33 µF decoupling capacitors:

- Every device that drives a bus on which outputs switch simultaneously.
- All synchronous counters.
- Devices used as oscillator elements.
- Schmitt-trigger devices with slow input rise and fall times. The slower the rise and fall time, the larger the bypass capacitor. Lab experimentation is suggested.

Bypass capacitors should be distributed over the circuit board. In addition, boards could be decoupled with a 1 µF capacitor. You should also ensure low-impedance paths to and from logic devices in board layouts.

Board Soldering Considerations

This section describes PC board soldering considerations for design and manufacturing of Series 5000 devices.

Recommended Solder Profile

Follow the general guidelines described in IPC/JEDEC Standard J-STD-020D.1 when soldering Series 5000 chips to PCBs. This standard includes information for classification reflow profiles. All Series 5000 chips comply with the European Union Restriction of

Hazardous Substances (RoHS) Directive (2002/95/EC), thus their profiles use the lead-free assembly, with a peak temperature T_p of 260 ºC, and a solder profile as summarized in **Table 47**.

Soldering Surface Mount (SMT) Parts

Table 47 lists the maximum reflow temperature for surface mount (SMT) parts. In all cases, consult the solder manufacturer's data sheet for recommendations on optimum reflow profile. The actual reflow profile chosen should consider the peak temperature limitations.

Table 47. Peak Temperatures for Surface Mount Parts

Product	RoHS Compliant	Model Number	Peak Temperature
FT 5000 Free Topology Smart Transceiver	Yes	14235R	260 ºC
Neuron 5000 Processor	Yes	14305R	260 ºC
FT-X3 Communications Transformer	Yes	14255R	245 ºC

As measured according to the IPC/JEDEC Standard J-STD-020D.1, Series 5000 chips have a Level 3 Classification. The recommended soldering technique for Series 5000 chips is surface mount reflow. Soldering techniques that involve immersing the entire part are not recommended. Consult the solder manufacturer's datasheet for recommendations on optimum reflow profile.

Dry pack is a process that slowly bakes moisture from the surface mount technology package and seals it into a dry pack bag to shield the unit from moisture in the atmosphere. The exterior of the bag is marked with a label that indicates that the devices are moisture sensitive and is marked with the date that the bag was sealed (there is a one year shelf life for such devices).

There is a limited amount of time to use surface-mount devices after they are removed from the dry pack. Before surface mounting, packages should not be out of the dry pack longer than 168 hours at ≤ 60% relative humidity and ≤ 30 °C. If the units have not been shipped dry pack or have been unpacked for too long, then units must be baked at 125 °C for 12 hours prior to board soldering. If this is not done, some percentage of the units can exhibit destructive failures or latent failures after the soldering process.

General ESD Handling Guidelines

All complementary metal-oxide-semiconductor (CMOS) devices have an insulated gate that is subject to voltage breakdown. The high-impedance gates on the devices are protected by on-chip networks. However, these on-chip networks do not make the chip immune to ESD. Laboratory tests show that devices can fail after one very high voltage discharge. They can also fail due to the cumulative effect of several discharges of lower potential.

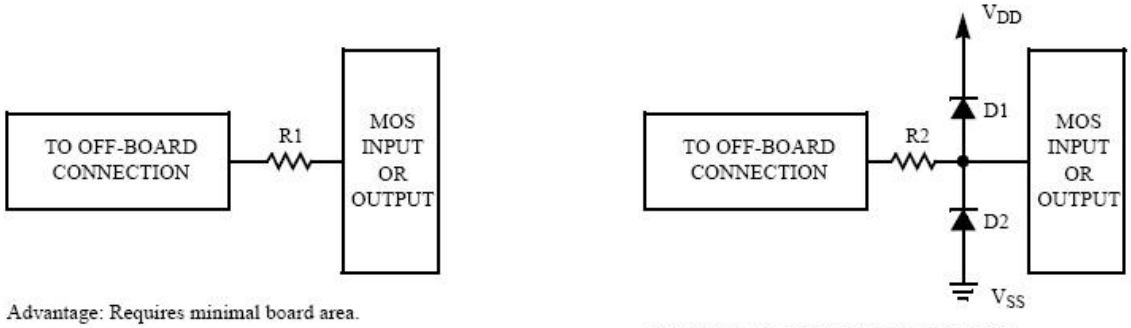
Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is shorted to V_{DD}, shorted to GND, or is open-circuited. As a result

of this damage, the device no longer functions. Less severe cases are more difficult to detect because they appear as intermittent failures or as degraded performance. Static damage can often increase leakage currents.

CMOS devices are not immune to large static voltage discharges that can be generated during handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4 kV – 15 kV range (depending on humidity, surface conditions, and so on). Therefore, you should observe the following general precautions:

1. Do not exceed the maximum ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or GND.
3. All low-impedance equipment (for example, pulse generators) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS devices is merely an extension of the device, and the same handling precautions apply. Contacting connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and is brought into contact with static-generating materials. For convenience, **Figure 62** on page 157 describes equations for added propagation delay and rise-time effects due to series-resistance size.
5. All CMOS devices should be stored or transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow," Styrofoam®, or plastic trays. Devices should be left in their original container until ready for use.
6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, because a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See **Figure 63** on page 158.
7. Nylon or other static-generating materials should not come in contact with CMOS circuits.
8. If automatic handling is being used, high levels of static electricity can be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines that come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers that use CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material, or soldered onto a PCB.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following precautions apply during wave-solder operations:
    a. The solder pot and conductive conveyor system of the wave-soldering machine must be grounded to an Earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an Earth ground.
    c. Operators must comply with precautions previously explained.

d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.



NOTE: These networks are useful for protecting the following:
a.digital inputs and outputs
b.analog inputs and outputs
c.three-state outputs
d.bidirectional (I/O) ports

Equation 1 – Propagation Delay vs. Series Resistance

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the input capacitance of the driven device in farads
k = 0.33 for the TTL input levels (switch point = 1.3 V)

Equation 2 – Rise Time vs. Series Resistance

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum rise time per data sheet in seconds
C = the board capacitance plus the input capacitance of the driven device in farads
k = 2.3 for other devices

Figure 62. Networks for Minimizing ESD and Reducing CMOS Latch-Up Susceptibility

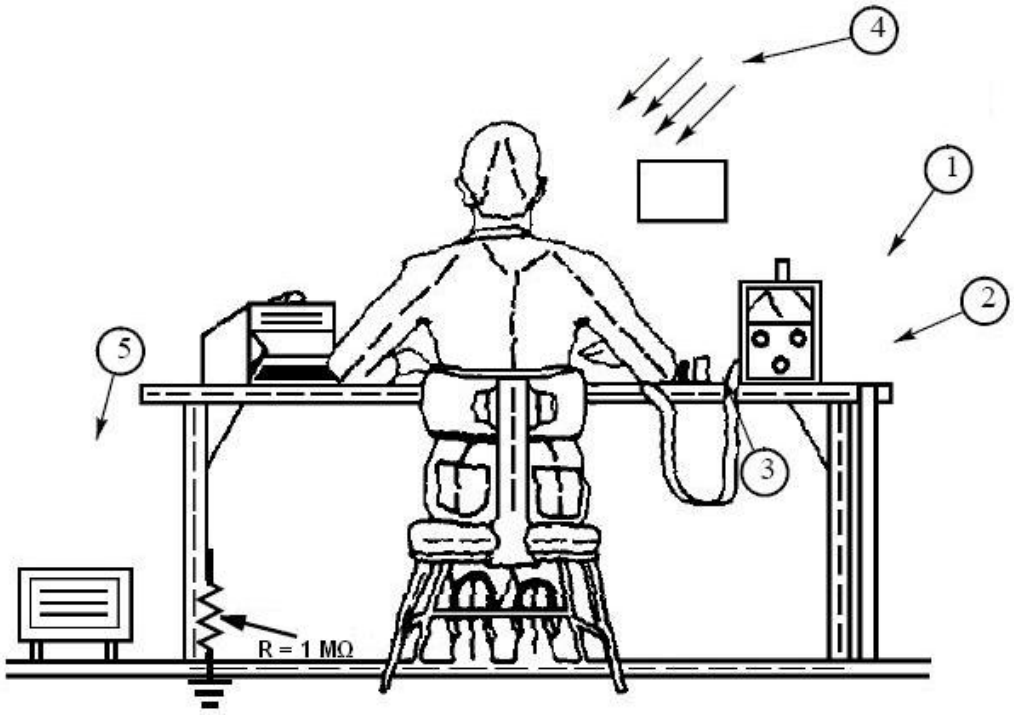


Figure 63. Typical Manufacturing Work Station

Notes for **Figure 63**:

1. 1/16-inch conductive sheet stock covering bench-top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer (ionized air blower directed at work). Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air, which causes the relative humidity inside a building to be less than outside humidity.

The following steps should be observed during board cleaning operation:

1. Vapor degreasers and baskets must be grounded to an Earth ground. Operators must likewise be grounded.
2. Brush or spray cleaning should not be used.
3. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
4. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
5. High-velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module. The use of static-detection meters for line surveillance is highly recommended.
6. The use of static-detection meters for line surveillance is highly recommended.

7. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
8. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
9. Double-check the equipment setup for proper polarity of voltage before conducting parametric or functional testing.
10. Do not recycle shipping rails. Continuous use causes deterioration of their antistatic coating.
11. Wrist straps and equipment logs should be maintained and audited on a regular basis. Wrist straps malfunction and the malfunction can go unnoticed. Also, equipment gets moved from time to time and grounds might not be reconnected properly.

Power Distribution and Decoupling Capacitors

Inductance in the power distribution creates noise during switching transients.

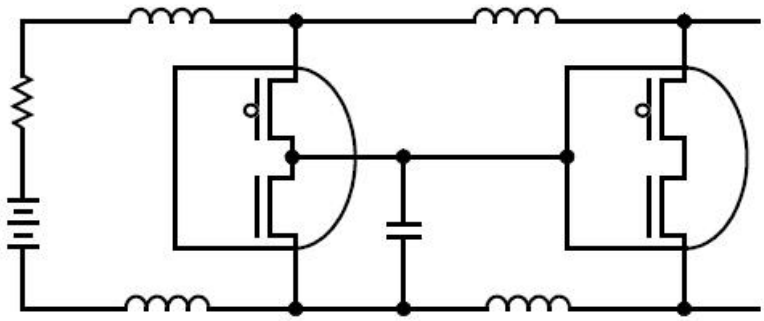


Figure 64. Inductance Creates Noise

For example, a 200 nH inductor with 25 mA and 5 ns surge characteristic can generate 1 V in noise:

$$V_{noise} = L\frac{dI}{dt}$$

If L = 200 nH, dI = 25 mA, dt = 5 ns, then V_{noise} = 200 nH * (25 mA / 5 ns) = 1 V.

Recommended Bypass Capacitor Placement

Proper decoupling is required to ensure proper operation of an FT 5000 Smart Transceiver or Neuron 5000 Processor. When you connect V_{DD} decoupling capacitors to Series 5000 chips, make the leads as short as possible. All V_{DD} pins must be tied to +3.3 V, and all GND pins to ground. Keep the crystal circuit close to the Series 5000 chip and isolated from communications lines.

Bypass capacitors should be 0.1 µF or 0.33 µF ceramic or dipped-mica capacitors, and should be placed as close to V_{DD33} pins as possible. V_{DD33} and GND loops should be avoided. Recommended configurations are:

- VDD3V3 pins: 8, 18, 29, 30, 31, 41
- VDD1V8 pins: 6, 16, 27, 44

Recommendation: Add an additional 1.0 µF (6.3 V, 10%, X7R) capacitor to pin 27 to provide extra protection and stability for the Series 5000 chip's internal voltage regulator.

Figure 65 shows suggested bypass capacitor placement and crystal circuit trace outlines. See *Pin Connections* on page 41 for additional information about placing these capacitors.

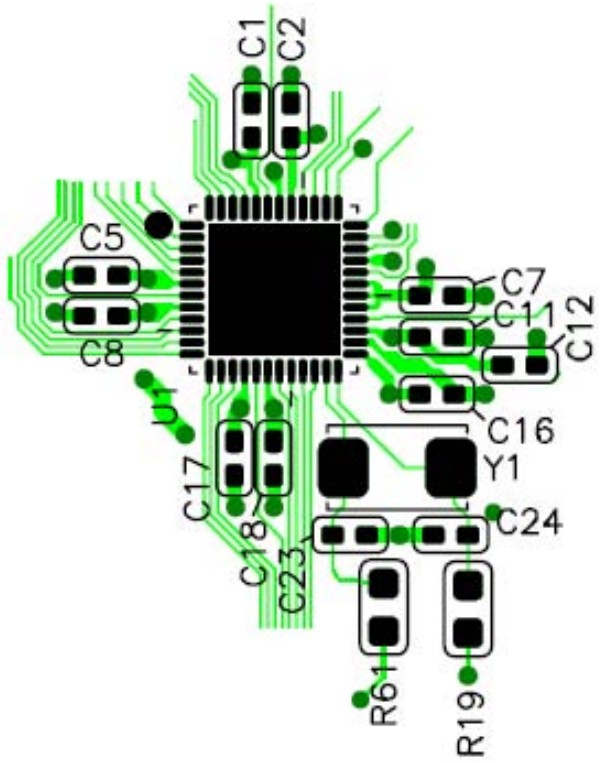


Figure 65. Minimum Recommended Capacitor Placement

The reference designators shown in the figure and the table are included as examples only.

Table 48. Parts Shown in the Figure

Reference	Part
C1	0.1 µF for pin 44 **VDD1V8**
C2	0.1 µF for pin 41 **VDD3V3** and pin 42 **VDD3V3**
C5	0.1 µF for pin 6 **VDD1V8**
C7	0.1 µF for pin 31 **AVDD3V3**, pin 30 **VDD3V3**, and pin 29 **VIN3V3**
C8	0.1 µF for pin 8 **VDD3V3**
C11	0.1 µF for pin 27 **VOUT1V8**

Reference	Part
C12	1.0 µF for pin 27 **VOUT1V8**
C16	0.01 µF across pins 25 and 26 (**VDDPLL** and **GNDPLL**)
C17	0.1 µF for pin 16 **VDD1V8**
C18	0.1 µF for pin 18 **VDD3V3**
C23	30 pF for pin 23 **XIN**
C24	30 pF for pin 24 **XOUT**
R19	200 Ω for pin 24 **XOUT**
R61	1 MΩ across pins 23 and 24 (**XIN** and **XOUT**)
Y1	External 10 MHz crystal

Key Layout Rules:

1. If possible, use 4-layer boards (or boards with more than four layers). Additional layers simplify the layout, and reduce noise-related and grounding problems.
2. For 2-layer boards, the four bypass capacitors must be close to the Series 5000 chip. V_{DD} and ground must use large traces to reduce inductance and noise.
3. On 2-layer boards, avoid running high-frequency digital signal traces under the crystal circuit or the communications port, on opposite sides of the board.
4. Ensure that power supply and ground traces are large enough to handle the peak surge switching currents. Otherwise, there can be power supply dips on the V_{DD} pins, which could cause errors in the checksum calculation, resulting in the Series 5000 chip's resetting.

E

Example Schematic

This appendix provides an example schematic for an FT 5000 Smart Transceiver, with associated non-volatile memory, communications transformer, and network connections.

Example Schematic

This appendix provides an example schematic for an FT 5000 Smart Transceiver. The example schematics are based on the FT 5000 Evaluation Board that is included with the NodeBuilder FX Development Tool and the Mini FX Evaluation Kit. The example schematic incorporates the design requirements that are described in the following sections:

- *External Serial Memory Interface* on page 24
- *Pin Connections* on page 41
- *Connection for an FT 5000 Smart Transceiver* on page 56
- *Clock Requirements* on page 63
- *Transformer Electrical Connections* on page 145

Basic Electrical Connections

Figure 66 shows the basic electrical connections for the FT 5000 Smart Transceiver.

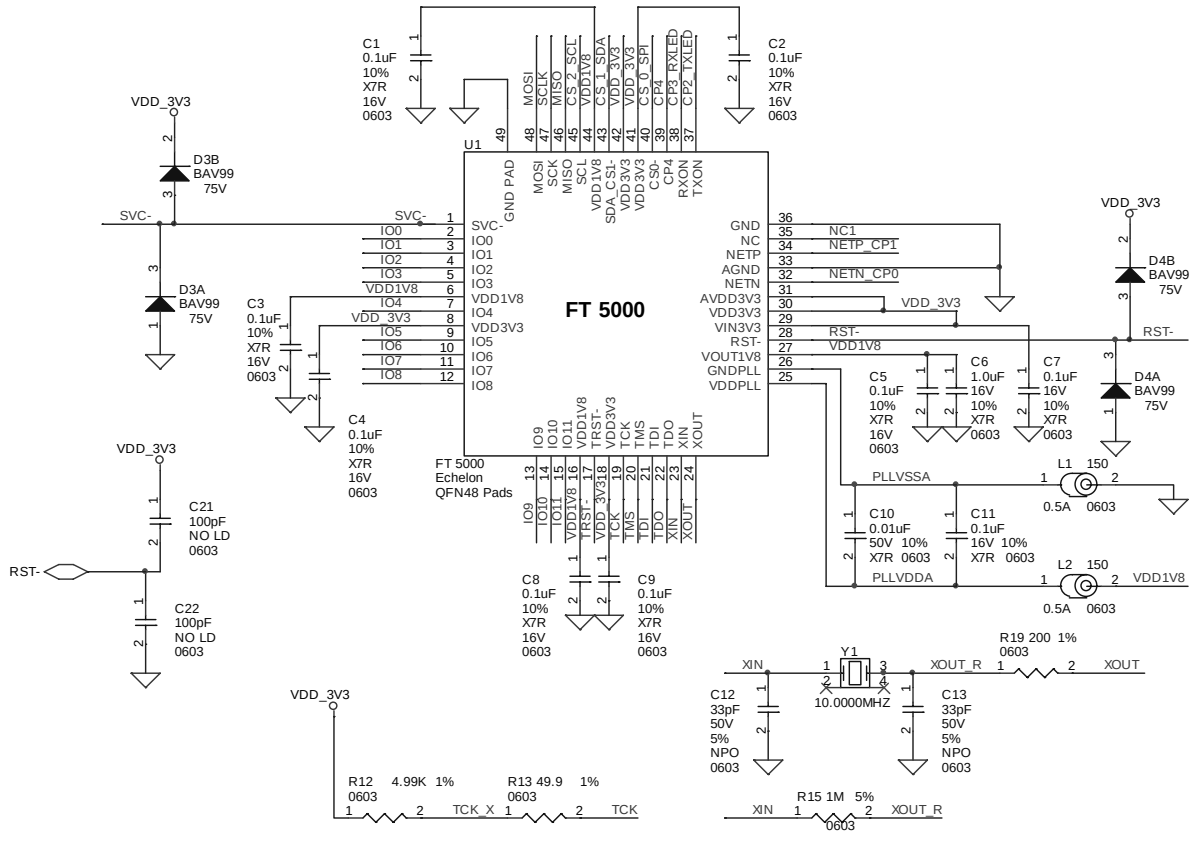


Figure 66. Basic Electrical Connections

Memory Interface Connections

Figure 67 shows the connections for the serial memory interface. The figure shows connections for both a serial EEPROM device and a flash memory device.

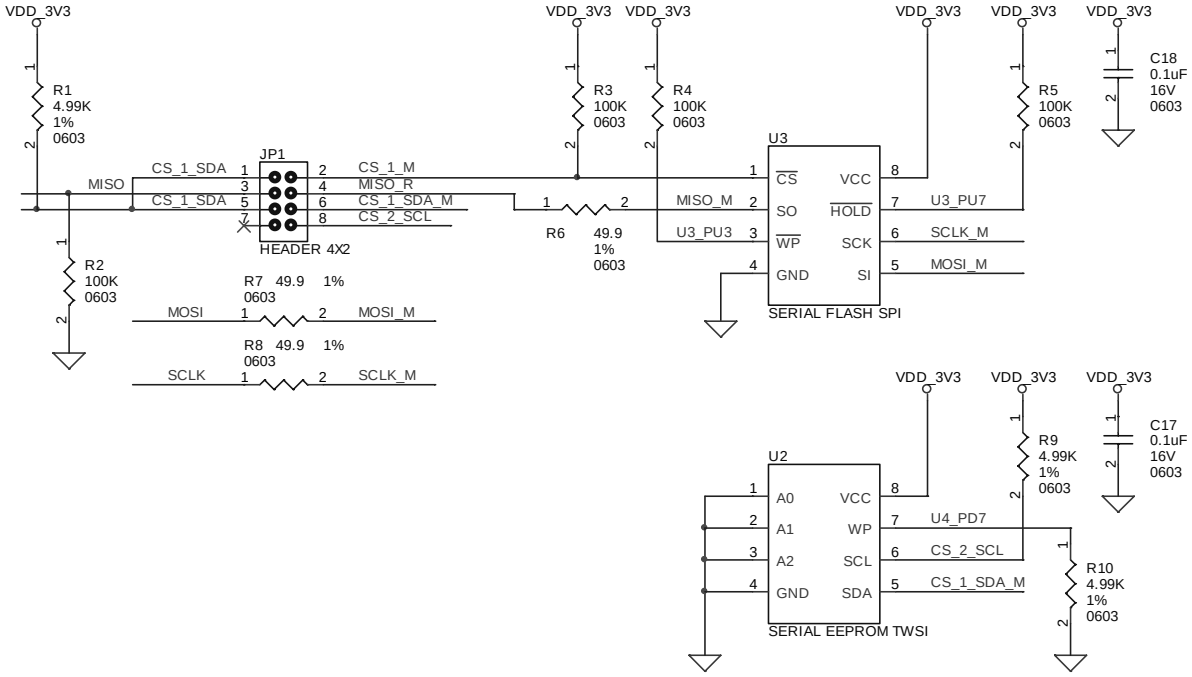


Figure 67. Memory Interface Connections

Transformer Connections

Figure 68 shows the connections for the communications transformer. The figure shows connections for both the FT-X2 Communication Transformer and the FT-X3 Communications Transformer. Your PCBA would include only an FT-X2 or an FT-X3.

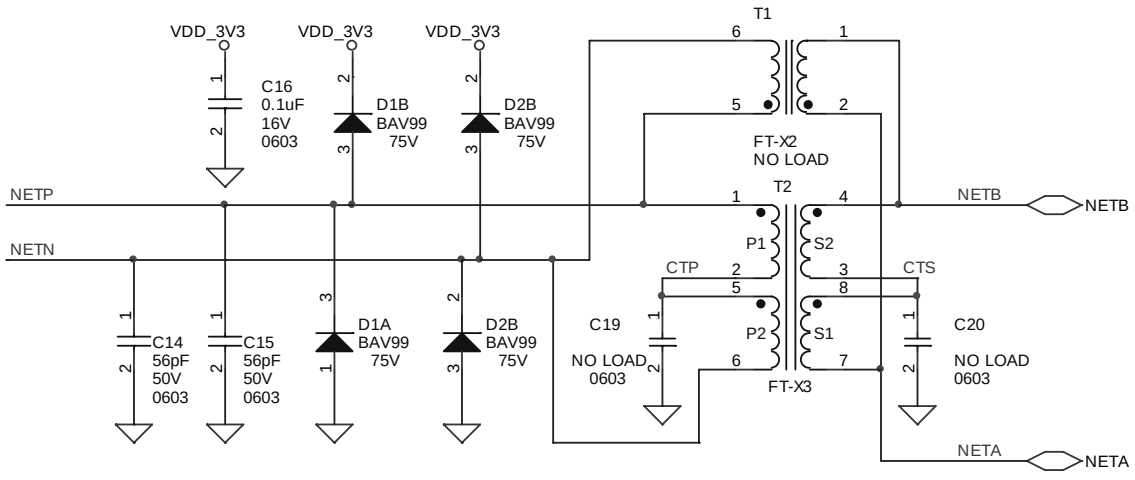


Figure 68. Transformer Connections

I/O and Network Connections

Figure 69 shows the basic I/O connections and the network connections. The figure does not show external I/O devices, and thus does not include pull-up or pull-down resistors for the IO0..IO11 signals.

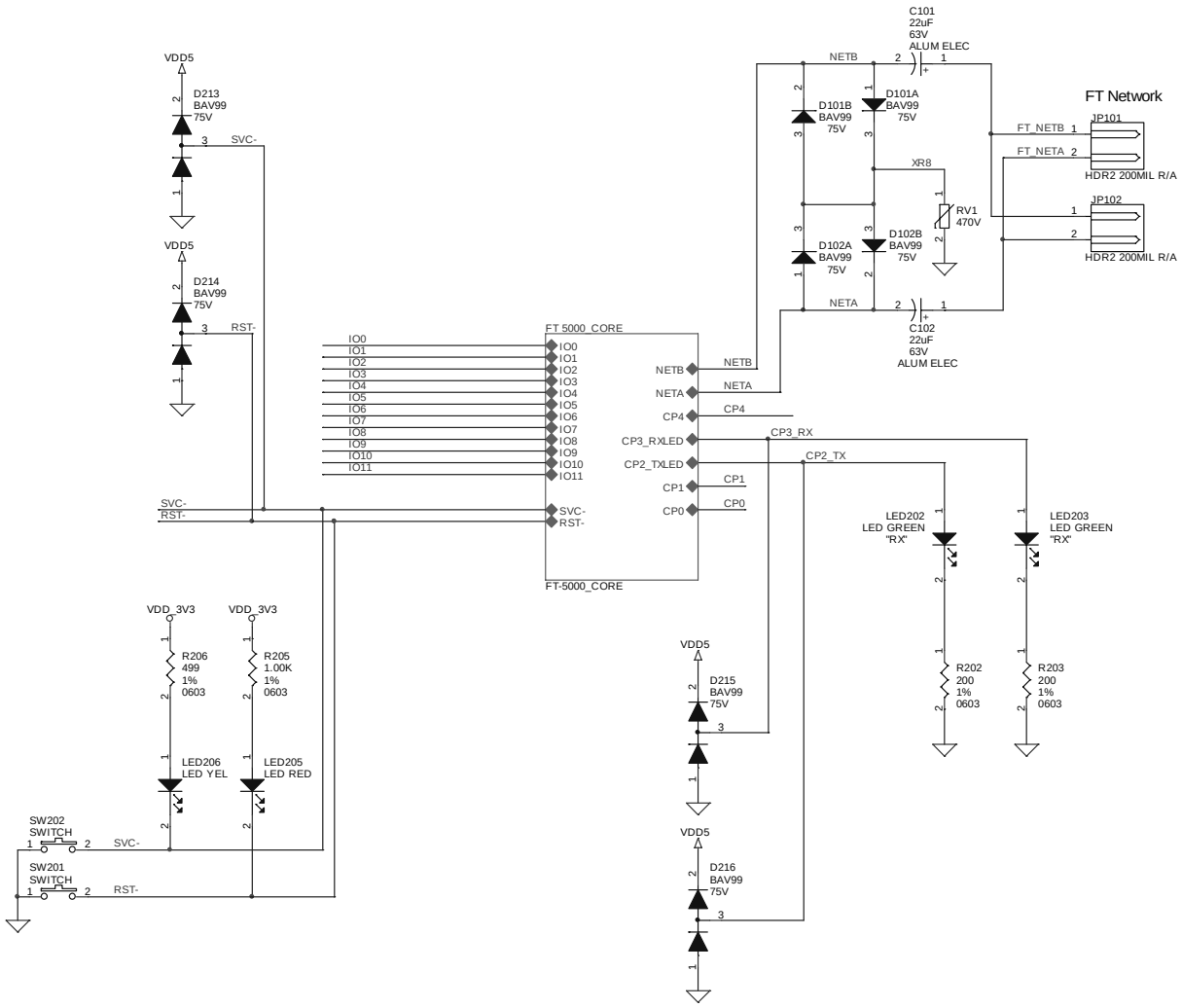


Figure 69. I/O and Network Connections

BOM for Example Schematic

Table 49 shows a partial bill of materials (BOM) for the example schematic shown in this appendix.

Table 49. Example BOM for Example Schematic

Reference Designator	Value
C10	0.01 µF
C12, C13	33 pF

Reference Designator	Value
C14, C15	56 pF
C19, C20, C21, C22	100 pF
C1, C2, C3, C4, C5, C7, C8, C9, C11, C16, C17, C18	0.1 µF
C6	1.0 µF
C101, C102	22 µF
D1, D2, D3, D4, D101, D102, D213, D214, D215, D216	BAV99
L1, L2	150 Ω
R6, R7, R8, R13	49.9 Ω
R18, R202, R203	200 Ω
R206	499 Ω
R205	1.00 kΩ
R1, R9, R10, R12	4.99 kΩ
R2, R3, R4, R5	100 kΩ
R15	1 MΩ
RV1	470 V
T2	Echelon FT-X3
T1	Echelon FT-X2 (not needed if FT-X3 is present)
U1	Echelon FT 5000 Smart Transceiver
U3	Atmel AT25F512B-SSH-B serial flash
U2	Atmel AT24C512BN-SH25-T serial EEPROM
Y1	10.0000 MHz

F

Vendor Contact Information

This appendix lists contact information for many of the product vendors mentioned in this manual.

Vendor Information

This appendix lists contact information for many of the product vendors mentioned in this manual. This information was current as of the publication of this manual. For most of the parts listed in this manual, Echelon does not require that you use these vendors, but has tested Series 5000 chips with products from the vendors listed.

Abracon Corporation

Headquarters

30332 Esperanza
Rancho Santa Margarita, CA 92688 USA
Phone: +1 949-546-8000
Fax: +1 949-546-8001

www.abracon.com

Atmel Corporation

Headquarters

2325 Orchard Parkway
San Jose, CA 95131 USA
Phone: +1 408-441-0311

www.atmel.com

Belden Inc.

Corporate

7733 Forsyth Boulevard, Suite 800
St. Louis, MO 63105 USA
Phone: +1 314-854-8000
Fax: +1 314-854-8001

www.belden.com

BPM Microsystems

Headquarters

5373 West Sam Houston Pkwy N, Suite 250
Houston, TX 77041 USA
Phone: +1 713-688-4600
Toll Free (US): 800-225-2102
Fax: +1 713-688-0920

www.bpmmicro.com

Citel Inc.

Headquarters

11381 Interchange Circle South
Miramar, FL 33025 USA
Phone: +1 954-430-6310
Toll Free (US): 800-248-3548
Fax: +1 954-430-7785

www.citelprotection.com

CommScope Inc.

Headquarters

1100 CommScope Place SE
Hickory, NC 28603 USA
Phone: +1 828-324-2200
Toll Free (US): 800-982-1708

www.commscope.com

Emulation Technology Inc.

Headquarters

2320 Walsh Avenue
Building H, Suite E
Santa Clara, CA 95051 USA
Toll Free (US): 800-ADAPTER (800-232-7837)

www.emulation.com

Fairchild Semiconductor Inc.

Headquarters

82 Running Hill Road
South Portland, ME 04106 USA
Phone: +1 207-775-8100
Toll Free (US): 800-341-0392

Corporate Offices

3001 Orchard Parkway
San Jose California 95134 USA
Phone: +1 408-822-2000

www.fairchildsemi.com

HiLo System Research Company Ltd.

Headquarters

4F, No. 18, Lane 76
Rueiguang Rd., Neihu Dist.
Taipei 11491, Taiwan
Phone: 886-2-8792-3301
Fax: 886-2-8792-3285

www.hilosystems.com.tw

Laird Technologies PLC

Headquarters

100 Pall Mall
London UK
SW1Y 5NQ

Phone: +44 (0)20 7468 4040
Fax: +44 (0)20 7839 2921

www.lairdtech.com

US Office

16401 Swingley Ridge Road
Suite 700
Chesterfield, MO 63017 USA
Phone: +1 636-898-6000
Fax: +1 636-898-6100

Littelfuse Inc.

Headquarters

8755 West Higgins Road Suite 500
Chicago IL 60631 USA
Phone: +1 773-628-1000
Fax: +1 847-391-0894

www.littelfuse.com

Numonyx BV

Headquarters

A-One Biz Center
Z.A. Vers la Piece
Rte de l'Etraz
1180 Rolle
Switzerland
Phone: +41.21.822.3700

www.numonyx.com

Americas Regional Sales Office

1900 Prairie City Road, FM3-N
Folsom, CA 95630 USA
Toll Free (US): 888-GO-NUMONYX

NXP Semiconductors BV

Headquarters

High Tech Campus 45
5656 AE Eindhoven
Netherlands
Phone: +31 40 27 29999
Fax: +31 40 27 43375

www.nxp.com

ON Semiconductor

Headquarters

5005 East McDowell Road
Phoenix, AZ 85008 USA
Phone: +1 602-244-6600
Toll Free (US): 888-743-7826

www.onsemi.com

Panasonic Corp.

Headquarters

1006 Oaza Kadoma
Kadoma, Osaka 571-8501
Japan
Phone: +81-6-6908-1121
Fax: +81-6-6908-2351

panasonic.co.jp/index3.html

US Office

1 Panasonic Way
Secaucus, New Jersey 07094 USA
Phone: +1 201-348-7000
Fax: +1 201-348-7016

panasonic.com

Plastronics Socket Company Inc.

Headquarters

2601 Texas Drive
Irving, Texas 75062 USA
Phone: +1 972-258-2580
Toll Free (US): 800-582-5822
Fax: +1 972-258-6771

www.plastronicsusa.com

Sankosha Corp.

Headquarters

4-3-8 Osaki
Shinagawa-ku, Tokyo 141
Japan
Phone: 81-3-3491-7181
Fax: 81-3-3494-7574

US Office

406 Amapola Avenue, Suite 135
Torrance, CA 90501 USA
Phone: +1 310-320-1661
Toll Free (US): 888-711-2436
Fax: +1 310-618-6869

www.sankosha-usa.com

Silicon Storage Technology Inc.

Headquarters

1171 Sonora Court
Sunnyvale, CA 94086 USA
Phone: +1 408-735-9110
Fax: +1 408-735-9036

www.sst.com

Taiyo Yuden Company Ltd.

Headquarters

Matsumura Bldg. 6-16-20 Ueno
Taito-Ku, Tokyo 110-0005
Japan
Phone: 81-3-3833-5441
Fax: 81-3-3835-4754

US Office

1930 North Thoreau Drive, Suite 190
Schaumburg, IL 60173 USA
Phone: +1 847-925-0888
Fax: +1 847-925-0899

www.t-yuden.com or www.yuden.co.jp/e/index.html

TDK Corp.

Headquarters

1-13-1, Nihonbashi, Chuo-ku
Tokyo, 103-8272
Japan

US Office

901 Franklin Avenue
P O Box 9302
Garden City, NY 11530-9302 USA
Phone: +1 516-535-2600
Fax: +1 516-294-8318

www.tdk.com

Total Phase Inc.

Headquarters

735 Palomar Avenue
Sunnyvale, CA 94085 USA
Phone: +1 408-850-6500

www.totalphase.com

Vishay Intertechnology Inc.

Headquarters

63 Lancaster Avenue
Malvern, PA 19355-2143 USA
Phone: +1 402-563-6866
Fax: +1 402-563-6296

www.vishay.com

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